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Asymmetric SRAM Memory Cell for Power Reduction

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Abstract: ***The main objective of this paper is to present the reasons for the preference of asymmetric SRAM cell over symmetric SRAM for cache memory applications. Since memory is main and consists a large part of systems, nearly fifty percent, reducing the power and delay in memories have become a hot burning issue. Almost half of the total CPU (central processing unit) dissipation is due to memory operations. SRAM memory is an essential building block for all processors and VLSI systems. Ideally, a SRAM cell should be fast and should dissipate low leakage power. Traditional SRAM cells are symmetrically composed of transistors with identical leakage and threshold characteristics, whereas asymmetric SRAM cell designs offer low leakage with little or no impact on latency.***

Keywords: SRAM, Low-leakage, Low-power, Dual-Vt.

1. Introduction

In recent years rapid growth is noticed in mobile, hand-held communication devices, battery operated devices that demand fast data transfer, larger memory capacity and low power consumption with minimum operational delays. A major part of any electronic system is the memory, on chip cache memories contributes a large fraction to the total power consumption of microprocessor, a cache is memory used to temporarily store the data.[1] As technology scales down into deep-submicron, leakage power is becoming a dominant source of power consumption. High-performance large-capacity Static Random Access Memories (SRAM) is an important component in the memory hierarchy of modern computing systems. SRAM design requires a balance between delay, area, and power consumption. The 6T SRAM (six transistors static random access memory) cells are the main choice for cache applications as the stability of the cell is best among all the cells, reducing the power dissipation in SRAM can significantly improve the power-efficiency, performance, reliability, and overall costs of the system. A SRAM (Static Random Access Memory) is designed to fill two purposes: to provide a direct interface with the CPU at speeds not attainable by DRAMs and to replace DRAMs in systems that require very low power consumption. In the first role, the SRAM serves as cache memory, interfacing between DRAMs and the CPU, The second driving force for SRAM technology is low power applications. Asymmetric technique has several main advantages over symmetric SRAMs as it reduces both active and standby leakage current including sub threshold and tunneling gate leakage components. Different methods are used for power reduction but Asymmetric SRAM works on the principle of dual-Vt it has no hardware or delay overheads and requires only a minor change in the SRAM design flow also has the ability to improve the static noise margin under process variations.

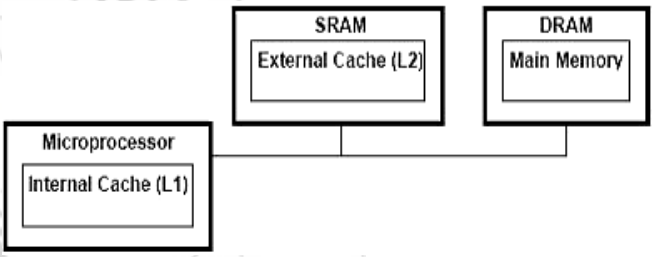

Figure 1: Memory configuration of CPU, SRAM and DRAM

2. Static Random-Access-Memory (SRAM)

It is a type of semiconductor memory that uses bistable latching circuitry to store each bit, it holds the stored value in Flip-Flop circuits as long as the power is on. The term static differentiates from dynamic RAM (DRAM), which must be periodically refreshed. SRAM is still volatile in the conventional sense that data is eventually lost when the memory is not powered. SRAM is more expensive and less dense than DRAM and is therefore not used for high and low-cost applications such as the main memory in personal computers. The Figure 2 shows a simple CMOS-SRAM cell which consists of two cross coupled inverters and two access transistors connecting the two inverters to the complementary-lines.[2]

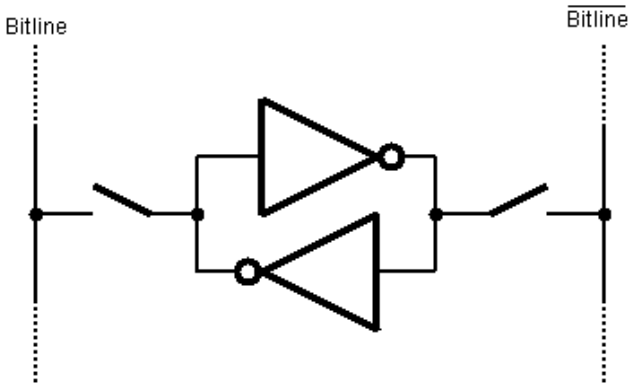

Figure 2: Basic SRAM cell

The Figure 2.1 shows a 6-transistor (6T) SRAM cell. In an SRAM cell, the pull-down NMOS transistors and the pass-transistors reside in the read path. The pull-up PMOS transistors and the pass-transistors, on the other hand, are in the write path. Traditionally all the cells used in an SRAM blocks are identical (i.e., the corresponding transistors have the same width, threshold voltage, and oxide thickness) that results in identical leakage characteristics for all cells.

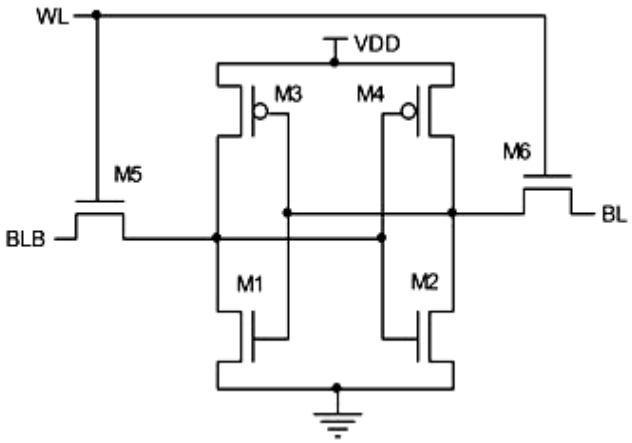

Figure 2.1.: 6T SRAM cell Structure

2.1 Access Time

It is the time delay or latency between a request to an electronic system, and the access being completed or the requested data returned. In telecommunication systems, access time is the delay between the start of an access attempt and successful access. Access time values are measured only on access attempts that result in successful access. In a computer, it is the time interval between the instant at which an instruction control unit initiates a call for data or a request to store data, and the instant at which delivery of the data is completed or the storage is started .This technique will minimize the total power dissipation of the cell.[4]

3. Asymmetric SRAM

Traditional high-performance SRAM cells uses six transistors of symmetric configuration with identical threshold voltage, the leakage can be reduced by the usage of dual-V*t* transistors which will result in reduced leakage while maintaining performance comparable to traditional cells. By varying the Width of the transistor we can change the threshold or switching voltage of the transistor. This technique is known as asymmetric or dual threshold voltage this technique will minimize the total power dissipation of the cell.[4]

3.1 Working of Asymmetric SRAM

Asymmetric SRAM cells reduce leakage while maintaining high performance based on the following approach: It selects a preferred state and weaken only those transistors necessary to drastically reduce leakage when the cell is in that state[1]. These cells exhibit asymmetric leakage and access behavior and this asymmetric access behavior can be exploited to maintain high performance while reducing the leakage. Asymmetric SRAM cell comprises of two inverters, i.e., (P2, N2) and (P1, N1), and two pass transistors, i.e., N3 and N4. In the inactive state, the word line (WL) is held low so that the two pass transistors are off isolating the cell from BL and BLB. During this stage, the bit lines are typically charged at V_{DD} (e.g., logic "1"). Cells spend most of their time in the inactive state. In this state, most of the leakage is dissipated by the transistors that are: 1) off and that 2) have a voltage differential across their drain and source. The value stored in the cell (i.e., the cell state) determines which transistors these are. When the cell is storing a "0," as in Fig. 1, the leaky transistors are P1, N4, and N2. If the cell was storing a "1," then transistors P2, N1, and N3 would dissipate leakage power. For read operation the W/L of N2 is greater than the W/L of N3. For write operation W/L of N4 is greater than W/L of P1 which is the CR ratio known as cell ratio should be (W/L) N2 > (W/L) N3.This ratio should be greater than 1. As we increase this ratio read stability of the cell increases. Similarly for Write operation $(W/L)_{N4} > (W/L)_{P1}$.This ratio is known as PR ratio (Pull Up ratio). It should also be greater than 1.As this ratio increases write stability of the cell increases.[4]

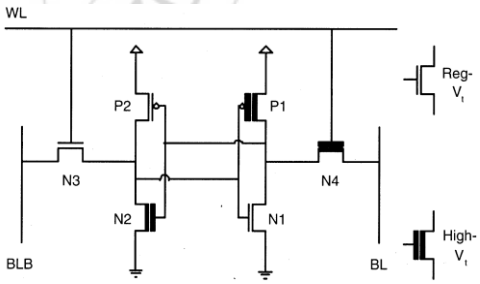

Figure 3: Basic asymmetric SRAM cell.

4. Sources of Power Dissipation

Power dissipation is an important constraint in a design as the leakage power will account for approximately 50% of the total chip power. There are two types of power dissipation

4.1 Dynamic Power Dissipation

Dynamic power dissipation is due to the charging and discharging capacitors, overturn of inverter and latch when the transistors in ON state Dynamic power dissipation is classified into two categories, namely short circuit power and power consumption during switching.

4.1.1. Short Circuit Power

If the input signals are having finite slopes which causes direct-path currents to flow through the gate for a short time during switching operation. For this short duration of time, there exists a direct path between VDD and GND and circuit consumes large amount of power which is termed as the short circuit power. [1]

4.1.2 Power Consumption During Switching

Charge is moved from Vdd to the output of the inverter, during and after input transaction, hereby pulling Vout to Vdd.

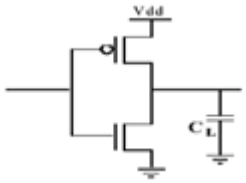

Figure 4: Dynamic power dissipation

Upon the opposite transition of the input, the PMOS transistor switches off and the NMOS transistor switches on.Now the charge stored on CL is moved to ground. This output capacitances consumed the power during switching is known as the dynamic power dissipation. It is the largest source of energy dissipation in CMOS circuits.

4.2 Static Power Dissipation

Traditionally, the static component of power consumption has been negligible in static CMOS. But as mentioned in the introduction, this is no longer the case. A number of Leakage mechanisms begin to gain significance. Most of these mechanisms are directly or indirectly due to the small device geometries.[1]

5. Need for ASRAM

LOW-POWER and high-stability have been the main themes of SRAM designs in the last decade [1]. The explosion of the portable electronic market constantly urges for less power-hungry architectures. Thus, many techniques have been employed to deliver this requirement such as scaling the supply voltage, using multi-threshold CMOS process to minimize the leakage

6. Advantages of Asymmetric SRAM Cell Over Symmetric Sram Cell

Asymmetric technique has several main advantages over previous techniques that are:

- Reduces both active and standby leakage current including sub threshold and tunneling gate leakage components.
- Has no hardware or delay overheads.
- Requires only a minor change in the SRAM design flow.
- Has the ability to improve the static noise margin under process variations.

(a) Irev is called reverse bias p-n junction leakage.

The asymmetric SRAM cell designs offer lower leakage power with little impact on latency. In asymmetric SRAM cells, selected transistors are “weakened” to reduce leakage current when the cell is storing a zero. Transistor weakening may be achieved by using higher voltage threshold transistors, by varying transistor geometries.

7. Conclusion

In recent years, power consumption has become a critical design concern for many VLSI systems. One can choose any method to reduce leakage depending upon requirements by changing the W/L of the Transistors. The asymmetric SRAM cell technique shows large reduction in leakage while retaining the cell information. Structure of the cell is identical to the 6T symmetric SRAM cell. The difference lies in the dual threshold voltages of the PMOS and NMOS transistors.

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