International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

FIR Interpolation Filter for Multi-Standard Digital Up Converter Using FPGA

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Abstract: ***This paper proposes an implementation of pulse shaping FIR interpolation filter for digital up converter. The designing of root raised cosine FIR filter for multistandard DUC for different standards is reduces the multiplications and additions per input samples and reduction in the power consumption has also been achieved. The 2-bit binary common sub-expression (BCS) elimination method is used to design the multipliers so that the delay can be minimized with increased speed and power performance parameters. The design could be validated for a standard wireless communication technology with specific incoming bit streams. The proposed design could be implemented using RTL Code and functional correctness is verified using a sophisticated Modelsim/ISIM Simulator tool.***

Keywords: Digital Up Converter, Software defined radio(SDR),Reconfigurable, Binary common sub-expression(BCS).

1. Introduction

Filters are the primary elements of all signal dealing out and electronic systems. In digital signal processing systems most widely used operations are FIR filtering. FIR filters are the primary component of the Digital Up converter. In telecommunication industry, Software defined radio concepts for various data transfer rates and high channel capacities.SDR [2] is a single device that supporting present as well as upcoming standard available in wireless communication systems. In an SDR system, within a single chip multiple standards can be realized by providing the channel select filter at the input level. To meet the specifications like different channel bandwidths, sampling rates, carrier-to noise ratios, and interference profiles one reconfigurable sample rate converter is required. Some pulse shaping filters are used in sample rate converter to reduce the undesired production of aliasing and interference effect to shape this baseband signal. Reconfigurable interpolators can be used in a next generation transceiver to realize a variable sample rate converter in order to support different data rates of different multiple standards in a single terminal.

Pulse-Shaping FIR interpolation filter for digital up converter has been proposed by several researchers toward designing a low-power, low-area, and low-complexity reconfigurable channel filter for data rate conversion in SDR system. A multiplier-less FIR interpolator has been proposed in [3] with smaller area usage and reduction in power by using the efficient look up tables (LUTs). This architecture is undesired because of its large ROM size. Area-delay-power efficient FIR filter by distributed arithmetic computation is presented by Meher [4]. In this implementation reduction in memory size leads to increase in the delay and area, this not suitable for SDR system.

In common sub-expression elimination (CSE) [5] technique, multiplication operations are performed by shift and add operation, and this technique defines critical path of the circuit. The constant multiplications (CM) [6] technique is useful in implementing the higher order filter design for reducing the hardware usage. A low complexity based binary CSE (BCSE) algorithm has been proposed in [7]. Constant shift multiplication based FIR filter design has been proposed in [8] involves use of adders in the multiplier block. This uses an additional area and power, and hardware usage makes design is not suitable for SDR system. From this literature low complexity multiplier by which more area and power can be reduced in designing the digital up converter (DUC) for SDR system. This disadvantage can be overcome by RRC filter architecture; this technique initially reduces the multiplications and additions per input samples and reduces the hardware and power consumption with designing of 2-bit BCS technique.

2. Problems in Designing the Root Raised Cosine Fir Filter and Solution

A. Problems in Designing the RRC FIR Filter

The hardware implementation of a reconfigurable RRC FIR interpolation filter has the following challenges. Implementation of the FIR interpolation filters with different lengths requires interpolation factor and roll-off factor. Selections of these parameters for designing the filters are the major challenge. The total number of multipliers and structural adders will linearly increase with the number of parameters for designing the filter. As the number of multipliers and structural adders increases, hence the problem of area and power consumptions increases for implementing the variable length higher order filter in a single architecture.

In recent communication technologies software defined radio is one of the advent technologies used. These technologies pose a major challenge in terms of area power and speed. FIR filter designing plays a major role in designing Digital up converter in defining speed and power of any communication system.

In BCSE technique, Proper choice of the length of the BCS is an important factor to avoid the inefficient utilization of hardware.

In BCSE technique, Proper use of BCS method to decrease the adders that maximizes the operating frequency of the filter is a challenge in the implementation of FIR filter for wireless communication standards. Propagation delay is another major tuning factor in defining the speed. The use of multipliers and adders with the conventional methods limits the speed and increases the power consumption of the system.

B. Solutions to the Problems

To solve the problems mentioned above proposed technique has the following steps.

1) The multiplexing technique can be used to decreasing the requirement of multipliers with control parameter (FTL_SEL) for designing the filter is to be selected depending on the roll-off factor.
2) Coefficients are generated in MATLAB. These obtained coefficients are passed through another set of multiplexers, with interpolation factor. This technique reduces the number of additions and multiplications per input samples.
3) 2-bit BCSE technique has been used other than 3-bit BCSE technique, to reduce the critical depth.This method gives a good propagation delay as compared with 3-bit BCSE based design.
4) In an FIR filter, the multiplication operation between inputs and coefficients can be written as

$$Y_1= x_1+2^{-1}x_1+2^{-2}x_1+\ldots\ldots\ldots +2^{-15}x_1 \quad (2)$$

In proposed architecture $x_2=x_1+2^{-1}x_1$ hence

$$Y_1= x_2+2^{-2}x_2+ 2^{-4}x_2+\ldots\ldots +2^{-14}x_2 \quad (3)$$

This technique helps to reducing the hardware usage as well as area requirement.

3. Architecture of the RRC Filter

The proposed architecture of FIR interpolation filter block diagram is shown in Fig.1. In this architecture, two parameters interpolation factor and roll-off factors are used. And the CLK is used to sample the output (RRCOUT), operates at a higher rate than others. The proposed architecture consists of different modules, like data generator (DG), coefficient generator (CG), coefficient selector (CS), and an accumulation unit.

A. DG Block

In order to generate the data values for RRC filter based on the Clock signal and also sample the input data DG block is used depending on the interpolation factor selection value. Here the filter taps are selected with different interpolation factor.

B. CG Block

In this block Multiplication between the obtained filterCoefficients from the MATLAB and the given inputs are performed. Coefficients are generated with Definite values of Roll-off factor, interpolation factor and sampling rate. Here the generated filter coefficients are 49-tap coefficients. Seven partial product outputs are generated and stored in different register blocks.

C. Coefficient Selector Block

The CS Block is used to direct the proper data to the addition block by using multiplexer units. Multiplexer unit will select appropriate generated coefficients from Dg block. Addition of generated partial product values are performed by 2-bit BCSE method.

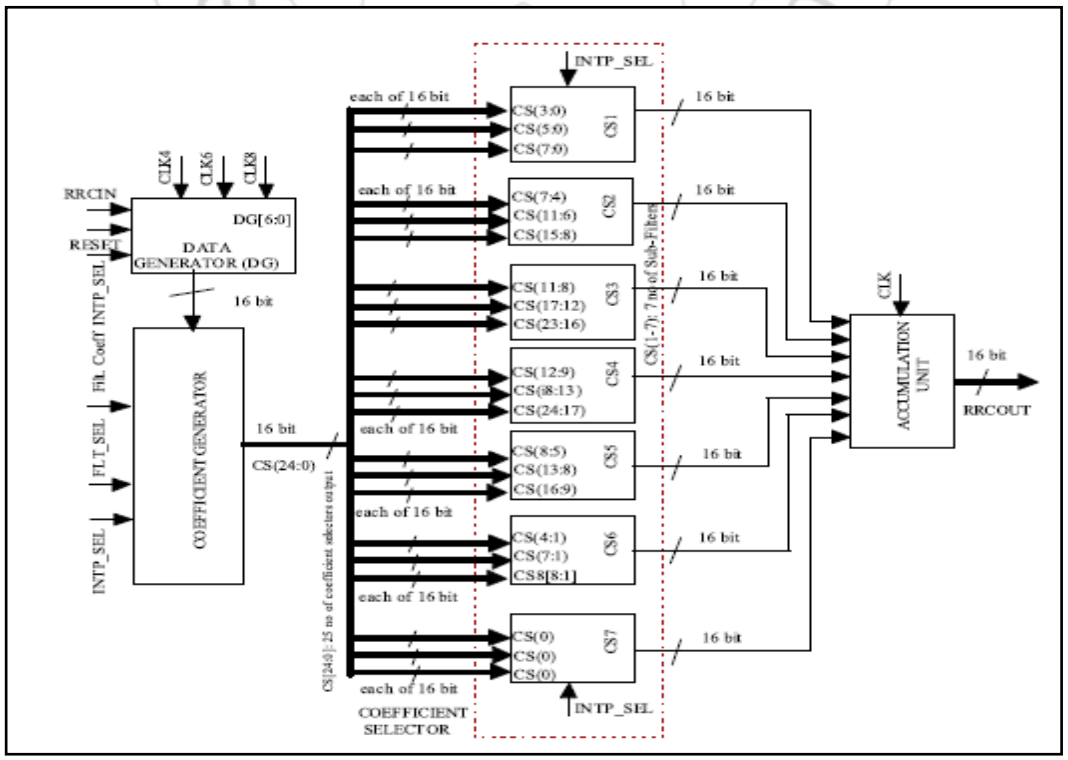

Figure 1: Proposed architecture of RRC filter

D. Accumulation Unit

This block has adders and registers blocks for addition and storing operation. The final output of RRC filter is generated in this block.

4. Results

The simulation results of the proposed RRC filter is as shown in Fig.2. First data_out signal is loaded by input value with enabling clock signal, then generated product values are added by using the 2-bit BCSE method, that is sum1=product1+product2, then

Sum1 value is added with product3 value. This method is continued to further steps. After that final rrc_out value is loaded with sum_out value.The chip scope results are matching with the simulation results so confirm that the implementation on FPGA is successful and the results are as per expectations. Fig.3 illustrates the chip scope results for proposed RRC filter module.

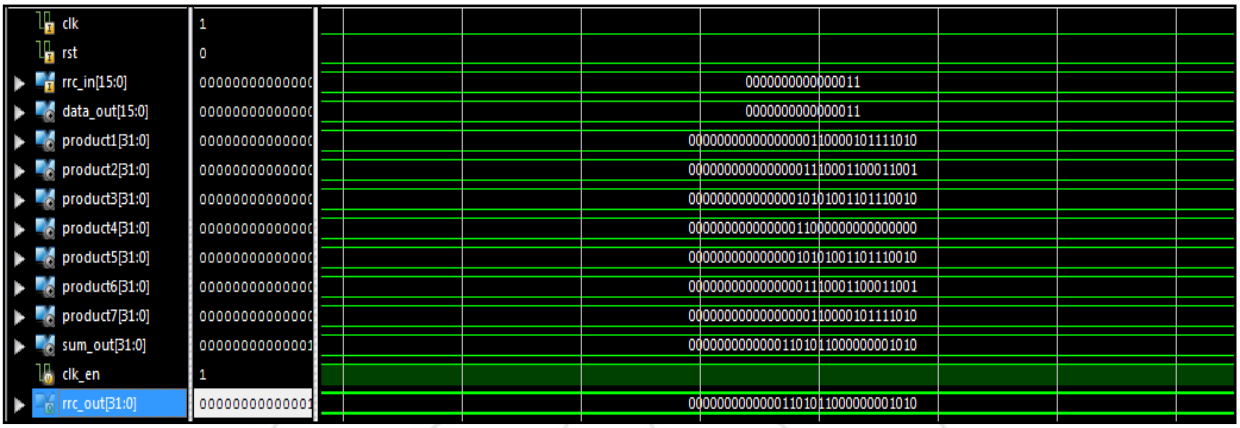

Figure 2: Simulation results of RRC filter

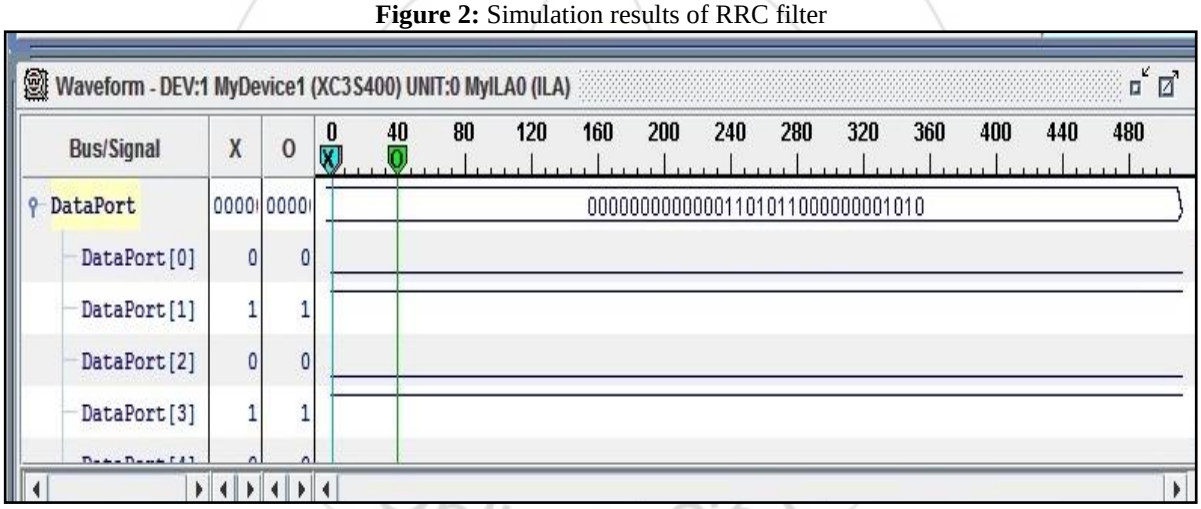

Figure 3: Xilinx Chip scope result of RRC filter

The RRC filter design has been implemented on XCS3S400 field-programmable gate array (FPGA) device using Xilinx ISE 14.5i EDA tool. Comparison has been done with 16- bit input and coefficients of 8-bit, 12-bit, and 16-bits of word length. Table 1: shows the tradeoff of area and delay product for a fair comparison.

Table 1: Comparisiom results of FIR filter in different techniques

Word length		8-bit	12-bit	16-bit	Area*delay Improvement (%)		
					8bit	12bit	16bit
GC	Proposed 2-bit BCSE method	167	281	345	23%	39%	49%
Delay (ns)		13.49	16.34	18.27			
GC	Constant shift multiplication method	2,878	3,532	3,771	62%	62%	63%
Delay		28.5	33.33	41.6			

The Table I shows the overall performance of the proposed design are 8%, 19%, 27% better than Xilinx multiplier core's performance and 62%,62%, and 63% better than 3-bit BCSE FIR filter architecture.

The synthesis results comparison of proposed architecture and Presented techniques in references shows in Table II. The synthesis result shows that the proposed technique has improvement in the LUT consumption, Gate Count and in speeds as compared with 3-bit BCSE method. The power estimation of RRC filter was 0.60W. In this Method RRC filter used less number of adders i.e. 6.

Table 2: Synthesis results comparision

References		Method used	Filter length	Max. freq.(MHz)	Slices (LUTs)	Gate Count
Proposed	Xc3s500e	2-bit BCSE	49 taps 16*17	73.54M	160	153
	Xc3s4000			66.4	249	232
	Xc3s400a			74.86	255	227

Xcs3000	3-bit BCSE	20 taps 16*17	64	1,601	23,878

The proposed design of 2-bit BCSE-based FIR filter consumes less power and high operating speed than earlier work reported on 3-bit BCSE based filter design.

5. Conclusion

This paper presents various problems occurred in designing the filter used in multistandard DUC, this is main component of SDR system. This offers the solutions to the problems and to make the filter is more efficient by reducing area and power with improvement in operating frequency. The proposed architecture is implemented on FPGA platform to validate the simulation results. This design can be enhanced with further reduction in area and power with better technique than BCSE-base design.

6. Acknowledgment

I am grateful to Mr. Yashwanth. N, Assistant Professor, Rajeev Institute of Technology, Hassan, for his constant guidance in completing the paper.

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