International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

High Efficiency Unity Power Factor Compact Fluorescent Lamp with Energy Conservation Dimmer for Commercial Applications

S. Sivaram

Abstract: ***This paper presentsunitypower factor single switch ballast for CFL with intensity controlled dimmer. The circuit topology comprises of single switch electronic ballast and an intensity controlled dimmer. This single switch is operated at ZVS and it carries only input current which leads to high efficiency. This circuit will operate in energy conservation mode during activation of Dimmer otherwise it operates in constant power mode. PSIM simulation results are provided which highlights the merits of proposed work.***

Keywords: compact fluorescent lamp, electronic ballast, Dimmer

1. Introduction

Energy is the most essential factors in people's life. Every day, people deal with the price of energy and think about saving of energy in their life. To save the energy, fluorescent lamps have been increasingly accepted in residential, industrial and commercial lighting applications.In commercial office applications, this lamp will glow continuously with constant intensity, which may leads to over illumination and energy loss.

The fluorescent lamp has negative resistance characteristics which lead to increase in current with decrease in lamp voltage. A lamp current stabilization element called ballast is required in order to provide sufficient voltage for proper lamp ignition and to stabilize lamp current once the lamp arc is established.

To provide a compact and lightweight solution for CFLs, high-frequency electronic ballasts operating at higher frequency than 25 kHz are more suitable than magnetic ballasts.For minimizing the cost, commercialCFL's normally do not include a power factor correction circuit in their ballasts. It consists of a diode rectifier and a self-driven half bridge parallel resonant inverter with a DC link capacitor.The major drawbackof this circuit is highly distorted line current and produces a large amount of unwanted harmonics, hence results in very poor power factor [1 – 4].

To improve the power factor, power factor correction circuit is introduced. The regulation of the PFC stage output DC voltage is achieved by controlling the duty cycle. However the circuit requires extra switching devices which increase the complexity size and cost of the device [5 – 11].

To reduce the number of MOSFETs required in the ballast power circuit, single-switch electronic ballasts were proposed in [12]–[17] by using the class-E resonant inverter. These electronic ballasts use only one switch to simultaneously achieve PFC while providing the lamp current stabilization at the inverter stage. The disadvantage of using the class-E resonant inverter is that the switch needs to suffer a high voltage stress of about 3–5 times of the input dc voltage [17].

On the other hand, in order to conserve energy or provide a comfortable lighting environment, dimming control is essential for the CFL electronic ballast. The formal incandescent dimmer cannot be used in CFL applications because of the ballast circuit which acts as a nonlinear load viewing from the supply. Therefore new methodology is required to perform dimming operation.

Different dimming technologies have been proposed; these methods can be categorized into phase-control [18] and frequency modulation [19]–[22]. These dimming technologies have to be operated under high-frequency condition, and hence, the wide-range dimming requirement is very difficult to achieve due to the acoustic-resonance limitations.

To limit this drawback, DC-link voltage regulation loop with feed-forward and feedback circuit was proposed [23]. The drawback of this circuit is it requires an EMI filter and the control circuit design is complex and also the voltage stress across the switch is high which reduces the efficiency and life time of the CFL.

This paper proposes a control scheme for high efficiency unity power factor single-switch electronic ballast that allows CFL to provide constant illumination for a wide range of input voltage at the lamp's full-power condition. On the other hand, during day time when the illumination is high, the intensity of the lamp is controlled by using a dimmer. When the dimmer is activated, the duty ratio is fixed to reduce the lamp illumination level. In the proposed design, the switching stress is reduced and hence the efficiency is increased.

2. Description About Proposed System

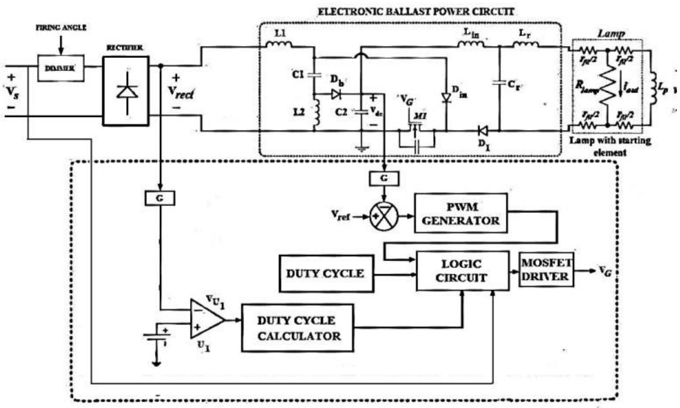

Figure 1: Proposed Dimmer controlled CFL

The completed ballast circuit with the proposed controller is shown in Fig. 1. The electronic ballast power circuit studied in this paper is a single-switch single-stage resonant inverter with SEPIC PFC.

A. Constant Lamp illuminationwith DC-Link Voltage Control

From the circuit it is clear that the dc-link capacitor (*Cd)*serves as the main energystorage element in the ballast circuit. The outputlamp poweris approximately equal to the DC-link power at the input of the inverter stage. Hence, by controlling the DC-link voltage *V*dc, output lamp power can be indirectly controlled, therebymaintaining almost constant light intensity at the output as theinput voltage fluctuates. Therefore this paper uses a DC voltage regulation loop which compares the DC link voltage with respect to the reference voltage and generates an error signal which is given to PWM generator. This generator will decide the duty ratio of the switch. Hence during line fluctuations the DC link voltage decreases and to maintain the constant DC voltage, the duty ratio increases. Thus by using this regulation loop constant illumination is maintained.

B. Proposed Controller with Dimmer operation.

During daylight condition, in commercial offices the lamp will glow with constant intensity. This will create over illumination which leads to energy loss. During over illumination, the energy can be conserved by using a dimmer which can be controlled by firing angle α. When α is varied (ie. $\alpha \geq \alpha_{min}$), the DC voltage regulation loop will get deactivated. The logic circuit will produce pulses with constant duty ratio and hence the DC link voltage varies with respect to firing angle of the dimmer. Therefore the illumination can be varied and controlled which leads to conservation of energy.

As α increase during dimming, it can be observed from Figure 4 that $V_{ripple2}$becomes less sinusoidal and can be described as consisting of two portions: a partly sinusoidal waveform and the discharge of the DC-link capacitor during the discontinuous period of the line voltage. The DC-link voltage during the discontinuous period of the line voltage can be obtained by noting that the DC-link capacitor must discharge its stored energy to the inverter side during this period.

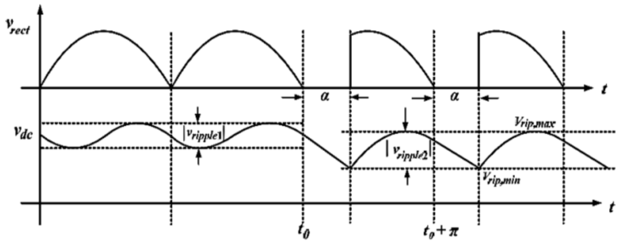

Figure 4: V_{ripple}during dimming

The firing angle α of the dimmer can be calculated by using duty cycle calculator which requires data's about the rectified DC voltage and the reference voltage. Depending upon the firing angle and the input supply voltage, the logic controller will decide whether to activate or deactivate the regulation loop. This is essential because the rectifier voltage will change during two cases: when input voltage varies and when dimmer is activated. When α is $\geq \alpha_{min}$, the controller will deactivate the regulation loop and generate gate pulses with constant duty ratio.

C. Design Specifications

The resonant circuit is designed based on the steady state lamp resistance. The formula is shown in (Eq. 1). Then the resonant circuit components are designed for the chosen *Q* value so that the proper lamp ignition voltage will be provided for the lamp start-up process. The switching frequency should be chosen to be below the corner frequency to ensure high voltage gain. At the same time, it should be above the resonant frequency to minimize the voltage and current stress of the switch.

$$R_{lamp} = \frac{P_{out}}{I_{out}^2} \quad (1)$$

$$L_r = \frac{QR_{lamp}}{2\pi f_0} \quad (2)$$

$$C_r = \frac{1}{(2\pi f_0)^2 L_r} \quad (3)$$

The corner frequency is chosen to be 90 kHz to minimize the resonant inductor size and the *Q* is chosen to be 0.9. The final values of *L*rand *Cr* are then calculated as shown in (Eq. 2) and (Eq. 3) respectively. The starting inductor for lamp ignition, *Lp*, is then selected to be 2.2*mH.* The switching frequency is chosen to be 70 kHz for this design.

3. Simulation Results and Performance

The performance of the proposed control circuit is validatedthrough PSIM simulation and the results are shown below.

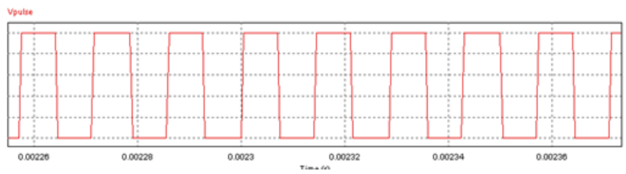

Figure 6: Gate Pulse

Figure 6 shows the gate pulse generated for MOSFET switch and the switching frequency is 70 KHz with duty cycle of 0.5.

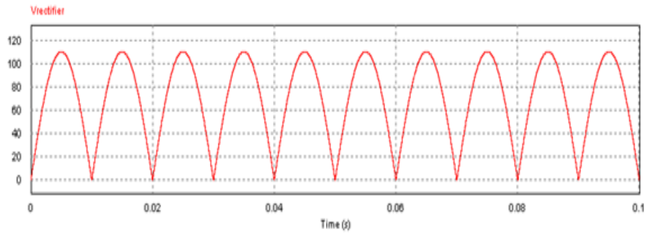

Figure 7: Rectifier Voltage

Figure 7shows the rectifier output voltage. The peak value is 110 V and the average DC voltage is 70 V.

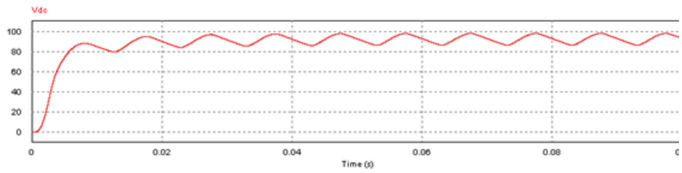

Figure 8: DC link voltage

Figure 8shows the DC link capacitor voltage. It is clear that Vripple is sinusoidal during normal operation and the average capacitor voltage is 90 V.

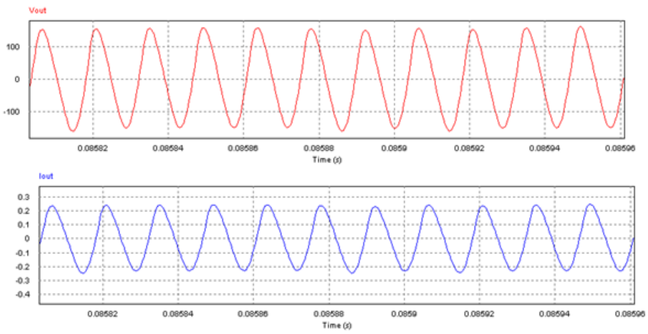

Figure 9: Output Voltage and Current waveforms

Figure 9shows the output voltage and current during steady state operation. The RMS voltage is 106 V and the RMS current is 0.17A.

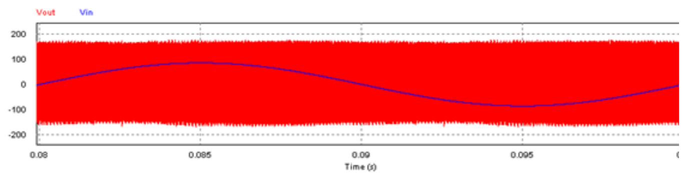

Figure 10: input voltage and output voltage

Figure 10shows the input and output voltage during transient operation. The input voltage given is 85 V and the RMS output voltage is 106 V. During line fluctuations from 85 V to 135 V, the constantoutput voltage is maintained by the help of regulation loop.

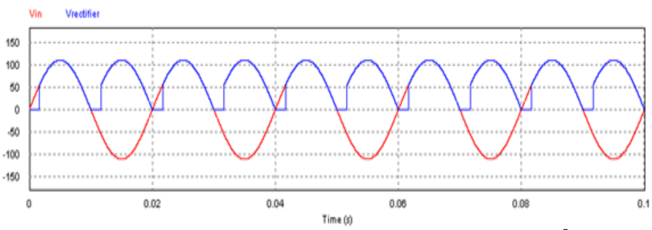

Figure 11: input and rectified voltage ($\alpha = 30^0$)

Figure 11shows the input and rectifier voltage during dimming operation. The firing angle given to the dimmer is $\alpha = 30^0$.

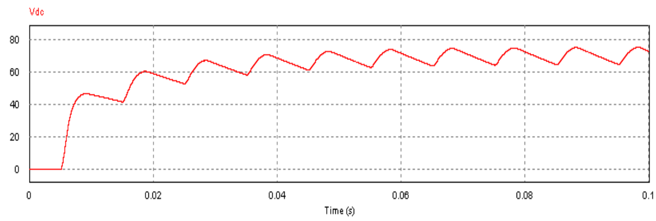

Figure 12: DC link voltage during Dimming

Figure 12shows the DC link capacitor voltage during dimming operation. As α increaseVripplebecomes lesssinusoidal and consist of two portions: a partly sinusoidal waveform continuous period andthe discharge of the DC-link capacitor during the discontinuous period of the line voltage.

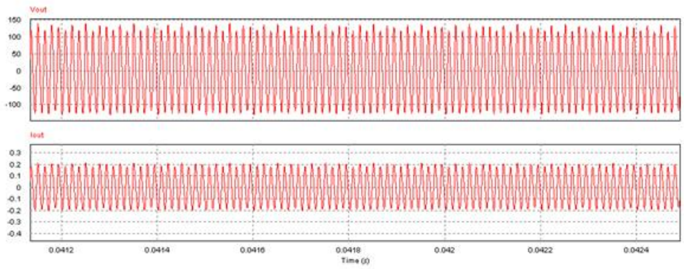

Figure 13: output voltage and current ($\alpha = 30^0$)

Figure 13shows the output voltage and current during dimming operation where firing angle $\alpha = 30^0$. The RMS voltage is 88 V and the RMS current is 0.14A.

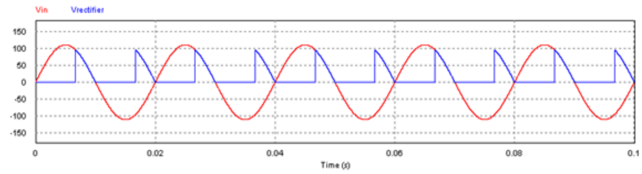

Figure 14: input and rectified voltage ($\alpha = 120^0$)

Figure 14shows the input and rectifier voltage during dimming operation. The firing angle given to the dimmer is $\alpha = 120^0$.

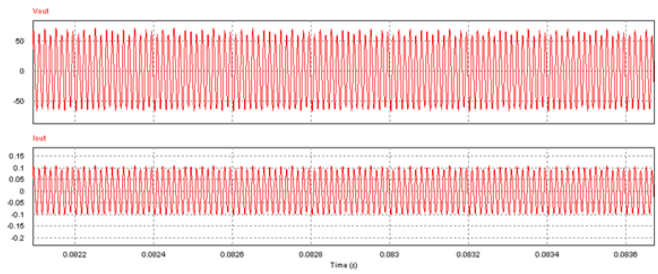

Figure 15: output voltage and current ($\alpha = 120^0$)

Figure 15shows the output voltage and current during dimming operation where firing angle $\alpha = 120^0$. The RMS voltage is 50 V and the RMS current is 0.07A.

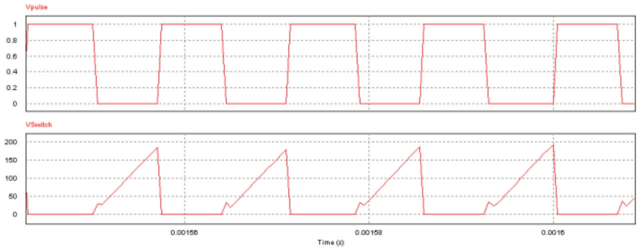

Figure 16: gate pulse and switch voltage

Figure 16shows the gate pulse and voltage across the switch. Switch transition is done with zero voltage switching and the voltage stress across the switch is also less.

Table 4: Energy Saved During Dimming Operation

Dimmer α	Time	V_{out} (RMS) V	I_{out} (RMS) A	P_{out} (RMS) W	Energy Saved W
0^0	6 pm – 8 am	106	0.17	18	-
30^0	8 am – 9 am	88	0.14	12.32	5.68
60^0	9 am – 10 am	71	0.13	9.23	8.77
90^0	10 am – 11 am	60	0.11	6.6	11.4
120^0	11 am – noon	50	0.07	3.5	14.5

4. Conclusion

A high efficiency unity power factor CFL with intensity controlled dimmer has been presented in this paper. During line fluctuations, the lamp is operated with voltage regulation loopmaintaining constant dc link voltage which realizes the constant lamp power. During dimmer activation, the regulation loop is deactivated and it will operate in energy conservation mode. The switch is operated at ZVS, which reduces the switching losses and increase the efficiency of the system. Simulation results have also beengiven to support the feasibility of the proposed work. Future works will include implementing a novel yet costeffectivecontroller design using fuzzy logic that will able to change the Vdc referenceaccording to the intensity of light in a room. Hence the energy can be conserved during over illumination.

References

[1] M. K. Kazimierczuk andW. Szaraniec, "Electronic ballast for fluorescent lamps," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 386–395, Oct. 1993.

[2] M. C. Cosby, Jr. and R. M. Nelms, "A resonant inverter for electronic ballast applications," *IEEE Trans. Ind. Electron.*, vol. 41, no. 4, pp. 418– 425, Aug. 1994.

[3] A. R. Seidel, F. E. Bisogno, and R. N. do Prado, "A design methodology for a self-oscillating electronic ballast," *IEEE Trans. Ind. Appl.*, vol. 43, no. 6, pp. 1524–1533, Nov./Dec. 2007.

[4] A. R. Seidel, F. E. Bisogno, T. B. Marchesan, and R.N. do Prado, "Designing a self-oscillating electronic ballast with bipolar transistor," in *Proc. 2002 Ind. Appl. Conf.*, pp. 1078–1083.

[5] F. J. Azcondo, F. J. Diaz, C. Branas, and R. Casanueva, "Microcontroller power mode stabilized power factor correction stage for high intensity discharge lamp electronic ballast," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 845–853, May 2007.

[6] J. M. Alonso, A. J. Calleja, E. Lopez, J. Ribas, and M. Rico-Secades, "A novel single-stage constant-wattage high-power-factor electronic ballast," *IEEE Trans. Ind. Electron.*, vol. 46, no. 6, pp. 1148–1158, Dec. 1999.

[7] J. M. Alonso, A. J. Calleja, F. J. Ferrero, E. Lopez, J. Ribas, and M. Rico- Secades, "Single-stage constant-wattage high-power-factor electronic ballast with dimming capability," in *Proc. IEEE Power Electron. Spec. Conf.*, 1998, pp. 2021–2027.

[8] C. S. Moo, T. F. Lin, and Y. C. Hsieh, "Single-stage high power factor electronic ballast for fluorescent lamps with constant power operation," *IEE Proc. Electr. Power Appl.*, vol. 148, no. 5, pp. 465–468, Sep. 2001.

[9] Y.-T. Huang, H.-C. Hsiao, Yi-Hua Liu, C.-R. Lee and L.-L. Lee, "A novel constant-power control for metal-halide lamp electronic ballasts with dimming capability," *IEEE Trans. Plasma Sci.*, vol. 38, no. 6, pp. 1482– 1488, Jun. 2010.

[10] C.-M. Huang, T.-J. Liang, R.-L. Lin and J.-F. Chen, "A novel constant power control circuit for hid electronic ballast," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 854–862, May 2007.

[11] R. De Oliveira Brioschi and J. L. F. Vieira, "High-power-factor electronic ballast with constant DC-link voltage," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1030–1037, Nov. 1998.

[12] A. Ekbote and D. S. Zinger, "Comparison of class E and half bridge inverters for use in electronic ballasts," in *Proc. 2006 Ind. Appl. Conf.(IAS)*, pp. 2198–2201.

[13] C. Lin and C. Chen, "A single-switch soft-switching electronic ballast with high input power factor," in *Proc. 1996 IEEE Int. Symp. Ind. Electron. (ISIE)*, pp. 697–702.

[14] M. Ponce, R. Vazquez, J. Arau, and D. Abud, "Class E amplifiers used as a high power factor electronic ballasts for fluorescent lamps in a single stage," in *Proc. 1998 Power Electron. Spec. Conf. (PESC)*, pp. 2009–2015.

[15] K. Jirasereeamornkul, M. K. Kazimierczuk, I. Boonyaroonate, and K. Chamnongthai, "Single-stage electronic ballast with class-E rectifieras power-factor corrector," *IEEE Trans. Circuits Syst. I: Regular Papers, [see also Circuits Syst. I: Fund. Theory Appl.]*, vol. 53, no. 1, pp. 139–148, Jan. 2006.

[16] A. S. de Morais, V. J. Farias, L. C. de Freitas, E. A. A. Coelho, and J. B. Vieira, Jr., "A high power factor ballast using a single switch withboth power stages integrated," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 524–531, Mar. 2006.

[17] E. Deng and S. Cuk, "Single switch, unity power factor, lamp ballasts," in *Proc. 1995 IEEE Appl. Power Electron. Conf. Expo.*, pp. 670–676.

[18] H. J. Chiu, H. M. Huang, Y. K. Lo, and C. H. Li, "High-frequency dimmable electronic ballast for HID lamps," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1452–1458, Sep. 2006.

[19] T. J. Ribarich, "Electronic dimmable ballast for high intensity discharge lamp," U.S. Patent 6 639 369, Oct. 28, 2003.

[20] S. Peters, M. Kettlitz, H. Schneidenbach, M. Wendt, and A. Kloss, "Dimming characteristics of metal-halide plasma lamps," *IEEE Trans. Plasma Sci.*, vol. 36, no. 4, pp. 1178–1179, Aug. 2008.

[21] W. Yan and S. Y. R. Hui, "An analysis into the dimming control and characteristic of discharge lamps," *IEEE*

Trans. Power Electron., vol. 20, no. 6, pp. 1432–1440, Nov. 2005.

[22] X. Cao, W. Yan, S. Y. R. Hui, and H. S. H. Chung, "Dimming control and characteristics of high-frequency operated metal halide lamps," *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 854–864, May 2004.

[23] John C. W. Lam, Praveen K. Jain, "A TRIAC Dimmable Single-Switch ElectronicBallast With Power Factor Correctionand Lamp Power Regulation," *IEEE Trans. Power Electron.*, vol. 29, no. 10, pp. 5472–5484, October 2014.