

A Review Study on High Speed Adder for Image Processing Applications

Parul Jaiswal¹, Rahul Gedam²

Abstract: *This paper is primarily deals the construction of 16 bit high speed on adder. The motivation behind the investigation is that an adder is a very basic building block of Arithmetic Logic Unit (ALU) and would be a limiting factor in performance of Central Processing Unit (CPU) . In this research article, we will present comparative analysis and study on existing 16 bit adder with some approximation technique which is used in arithmetic application. Here we discuss about the existing accurate and approximate architecture of different kind of adder. As we there is many application where accuracy can be tolerable by human eye. So there is no need of accurate design we can use approximate design for those kind of applications. This paper is implementing the existing design on Xilinx-14.2 and simulated is done on Modelsim.*

Keywords: FPGA, LUT, ALU, CPU, ASIC, APPROXIMATION

1. Introduction

There are two important challenges that the world of computing is facing. Currently, the first challenge is due to the increasingly ubiquitous nature of the present day portable electronics ranging from mobile phones to GPS-based navigation devices. Portability demands lower energy consumption without compromising on the functionality. Also, demand for low energy consuming, also referred to as green design, electronics [1] is gaining a lot of momentum.

According to the 2008 International Technology Roadmap for Semiconductors (ITRS) "Energy Consumption has become an increasingly important topic of public discussion in recent years because of global CO₂ emission .In general, the ITRS documents the impressive trends and, more importantly, sets aggressive targets for future electronics energy efficiency, for example, computational energy/operation (per logic and per memory-bit state changes). The most detailed targets relate directly to semiconductor materials, process and device technologies, which form the bases of integrated-circuit manufacturing and components, respectively." [2]

The core of every microprocessor, digital signal processor (DSP), and data processing application- specific integrated circuit (ASIC) is its data path. It is often the crucial circuit component if die area, power dissipation, and especially operation speed are of concern. At the core of data-path and addressing units in turn are arithmetic units, such as comparators, adders, and multipliers. Finally, the basic operation found in most arithmetic components is the binary addition. Besides of the simple addition of two numbers, adders are also used in more complex operations like multiplication and division. But also simpler operations like incrementing and magnitude comparison base on binary addition.

Therefore, binary addition is the most important arithmetic operation. It is also a very critical one if implemented in hardware because it involves an expensive carry-propagation step, the evaluation time of which is dependent on the operand word length. The efficient implementation of the addition operation in an integrated circuit is a key problem in VLSI design. Productivity in ASIC design is constantly

improved by the use of cell based design techniques — such as standard cells, gate arrays, and field programmable gate arrays (FPGA) — and by low- and high-level hardware synthesis. This asks for adder architectures which result in efficient cell-based circuit realizations which can easily be synthesized. Furthermore, they should provide enough flexibility in order to accommodate custom timing and area constraints as well as to allow the implementation of customized adders.

The second challenge is manufacturing reliable and predictable electronic devices. Moore's Law predicts that the number of transistors on a single die is going to increase at an exponential rate. This has been accomplished by decreasing the size of an individual transistor up to 20nm where particular layers such as the gate oxide layer are about 1.2 nm (equivalent to 5 atoms!). But engineering considerations on lithography have limitations of designing these tiny elements precisely which leads to hindrances like thermal noise, parametric variations and other device perturbations [3,4,5] which leads to unreliable computing. Again the 2008 ITRS report states as a long term challenge "Dealing with fluctuations and statistical process variations". Also the paper mentions that "Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control". [2]

These two challenges have competing requirements in the design of a VLSI system. A straightforward method of lowering the energy consumption is to lower the supply voltage of the circuit. But this would lead to transistors behaving unreliably because noise becomes a dominant factor. To ensure reliability, techniques such as redundancy and majority voting [6] can be used. However these techniques tremendously increase the energy consumption of the circuit. Thus conventional methods typically have contradictory results and do not offer a common solution to both energy consumption and reliable design.

The conventional electronic circuit design methodology utilizes three parameters in the tradeoff argument, the energy consumption of the circuit, the area occupied by the circuit and the speed at which the circuit is being operated. To face the challenges outlined previously, a radically new solution to introduce a new alternate dimension, the accuracy of the

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circuit, to the traditional design approach has been proposed recently. For the first time ever, Palem [7,8], showed that noise (or randomness) can be exploited as a resource for low energy but still obtain useful computation.

Currently there are three different techniques, applicable in different scenarios that use this novel fourth dimension in circuit design [9,10,11]. The first approach uses CMOS circuits that operate probabilistically due to noise [12]. The concept of a probabilistic CMOS switch (PCMS) was introduced where a PCMS inverter is correct with a probability parameter $p \ll 1$. The probabilistic inverter has been characterized in detail in terms of the relation between its energy consumption per switching and its probability of correctness. These probabilistic inverters were then used to design bigger probabilistic gates which switch correctly with a probability of correctness. This work was later extended to develop a probabilistic Boolean logic, because it was realized that conventional Boolean logic was no more valid in the universe where devices are probabilistic and not deterministic [13]. In probabilistic Boolean logic, the basic operators are defined with a probability of correctness, for example, an AND gate with a probability of correctness p is defined as \wedge_p . Further extending the foundational probabilistic Boolean logic, a probabilistic arithmetic was developed, where the operators are also defined with a probability of correctness, such as $+_p$.

2. Overview

Inexact circuit design is a design philosophy where the conventional constraint of requiring 100% accuracy in circuits is relaxed. Fundamentally, this philosophy adds a fourth dimension of accuracy to the current 3-dimensional circuit design space spanning around power consumption, area and delay. This methodology is applicable in the following two situations.

- The first situation is where the circuits are inherently "unreliable" and "probabilistic". Increasing parameter variations, noise susceptibility and decreasing process sizes are causing CMOS devices to be non-deterministic. To address these issues and precisely model the effect of these probabilistic circuit elements, the metric of accuracy needs to be introduced into the entire circuit design framework.
- The second situation is where the circuits themselves are not probabilistic in nature but are deterministic, but the application does not demand 100% accuracy. In such cases, relaxing the very rigid constraint of accuracy can be used to decrease energy consumption which is one of the leading challenges in current day circuit design. The first challenge in adopting an inexact circuit design methodology is to prove that circuits with less than 100% accuracy can still be used to perform useful computations in many applications which are energy constrained. There are two types of applications where inexact circuit design can be implemented. They are
- The first set of applications is where randomness is a required quality. For example, many encryption applications use pseudo-random number generators to produce random numbers. But if there was a circuit that

was inherently random then the extensive overhead of a pseudo-random number generator can be removed. That there are numerous such applications/algorithms which actually benefit from having a circuit which is inherently probabilistic. Some of the algorithms are Bayesian inference, Random neural networks, probabilistic cellular automata, and hyper-encryption.

- The second set of applications where accuracy can be relaxed is where a less than 100% correctness can be tolerated. This set primarily consists of traditional digital signal processing (DSP) applications whose output is consumed and judged by a human being. For example, consider a music player whose quality can be tuned based on how much battery power is left. In fact, many DSP algorithms are "approximate" in nature. The discrete Fourier transform, for example, represents the entire signal in the frequency spectrum with a few samples, thus introducing both quantization and sampling error. However, this still works because the human brain can interpret stimuli to the body's senses and obtain useful information even if they are not completely accurate.

There are many researchers provide a many types of Approximate ADDERS and Multipliers. In [13] the author proposed a new novel adder targeting to reduce the area and increase the speed of the circuit. The work is as shown in below first splitting the input operands into two parts: an accurate part that includes higher order bits and the inaccurate part that includes remaining lower order bits. Length of each part need not be equal and depends upon MAA's and AP's of application. The addition process starts from the joining point towards the two opposite directions simultaneously. Since the higher order bits play more important role than the lower order bits, normal addition method is applied for accurate part to preserve its correctness.

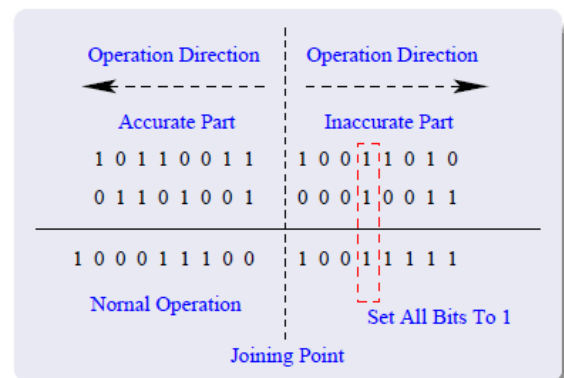


Figure 1: Error Tolerant Adder Type I (ETAI)

For inaccurate part no carry signal will be generated or taken in at any bit position to eliminate the carry propagation path. To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted:

- Check every bit position from left to right,
- If both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position,
- If both input bits are "1", the checking process stopped and from this bit onwards, all sum bits to the right are set to "1".

By eliminating the carry propagation path in the inaccurate part and simultaneously performing addition in two separate parts, the overall delay and power is reduced. But the accuracy of the ETA-I is poor for small input numbers. In ETA-I the AP's are strong function of input range and degrades as input range decrease, but AP's are 100% for large input range.

3. Error-Tolerant Adder

To solve small number addition problem, ETA-II[14] was proposed by Zhu. ETA-II splits the entire carry propagation path into a number of short paths and completes the carry propagations in these short paths concurrently. The below figure shows the architecture and approach

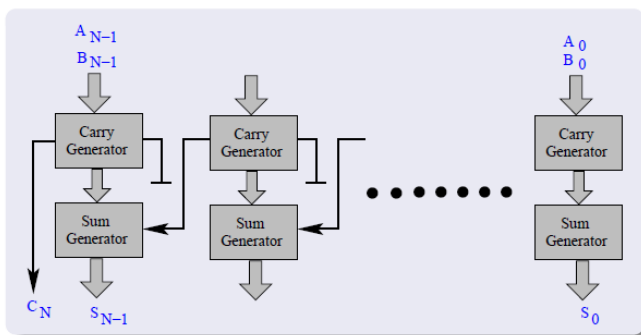


Figure 2: Block diagram of Type II ETA (ETAII)

In binary addition, worst-case happens when the carry signals are generated at the LSBs and propagates along the carry chain to the MSBs. If this worst case happens, tremendous amount of time and power will be consumed. As the worst case seldom happens, hence for most of the cases, this carry signal can be determined by just considering several input bits on the right of the current bit position. In ETA-II[14], an N - bit adder is divided into M blocks ($M \geq 2$). Each block contains N/M bits and consists of two separate circuitries – Carry Generator and Sum Generator. The carry generator creates the carry-out signal and does not take carry-in signal from previous block and, hence the carry propagation only exists between two neighboring blocks. The longest carry propagation path of ETA-II is $2N/M$ and, hence worst-case delay of ETA-II is only $2/M$ times of the conventional adder. The accuracy of ETA-II for large input operands is degraded than ETA-I. The degraded accuracy for large input may still restrict ETA-II use.

In modified ETA-II [14] design, the higher order bits should be more accurate than the lower order bits. In modified structure, the first three carry generators are cascaded together to generate the carry signals. In this way, the carry signal for the highest block is generated by the preceding 12 bits and the carry signal for the others block is generated by the preceding 8 bits.

The approximate designs have difficulty of detecting and correcting errors, since they are designed for error-acceptable applications with target accuracy. In some applications, however, more accurate or totally accurate results are required under certain conditions, e.g., image processing in security cameras. In contexts where the required accuracy changes during runtime, the accuracy of results should be

configurable to maximize the benefit of approximate operations. Figure illustrates how power benefits can be achieved with an accuracy-configurable design.

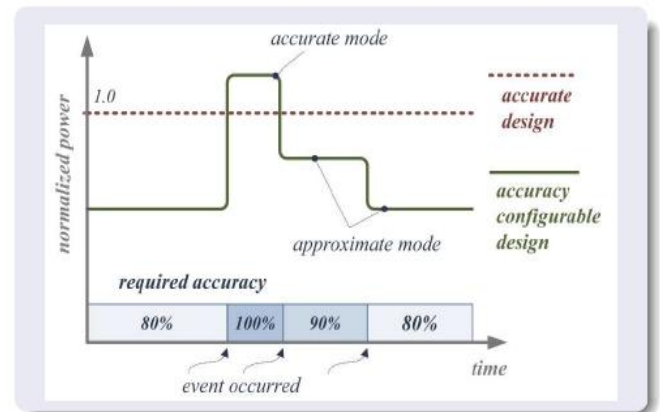


Figure 3: Accuracy and power graph

The Accuracy Configurable Adder (ACA) [16] adder has feature of runtime accuracy configurability for better trade-off between accuracy, performance, and power. In ACA adder, the carry chain is cut to reduce critical-path delay, and sub-adders generate results of partial summations to increase accuracy.

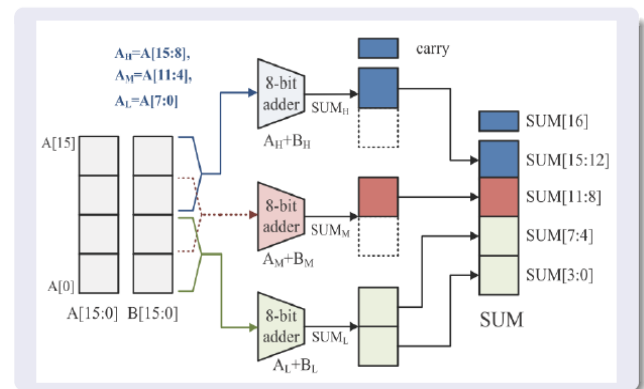
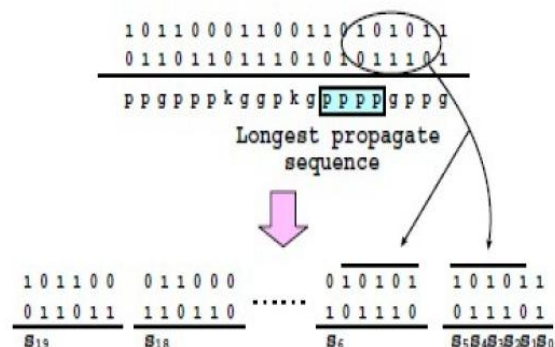


Figure 3: ACA

Without the middle sub-adder, for random input patterns the error rate is 50.1%, whereas with the introduction of the middle sub-adder, error rate is reduced to only 5.5%.



In this paper [24] they took a specific case of 20 bit VLSA, which have two elements: 20 bit almost correct adder and an error detection circuit. In order to add two n -bit integers A and B , one can define generate, propagate and kill signals at

gi = aibi
pi = ai xor bi
ki = ai + bi

ACA adder, the carry chain is cut to reduce critical-path delay, and sub-adders generate results of partial summations to increase accuracy

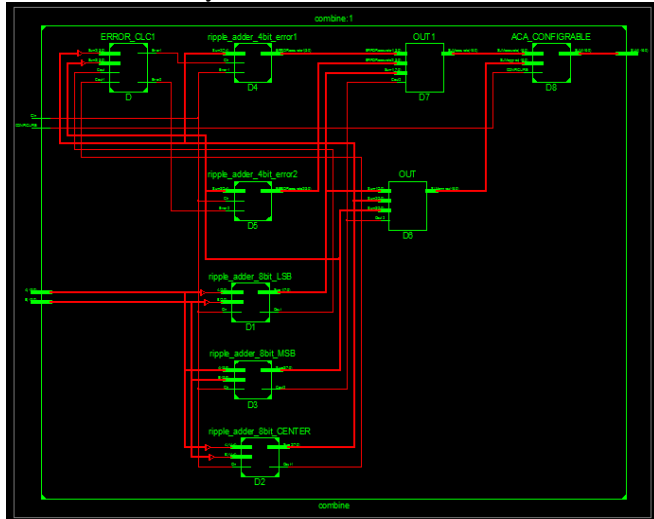


Figure 7: ACA schematic

ETA: There are many different types of adder such as ripple carry adder, look ahead adder, carry save adder. But all these have some problem regarding their speed and power. A common solution to these speed and power is ETA by compromising a bit of accuracy. It can attain great improvement in both speed and power

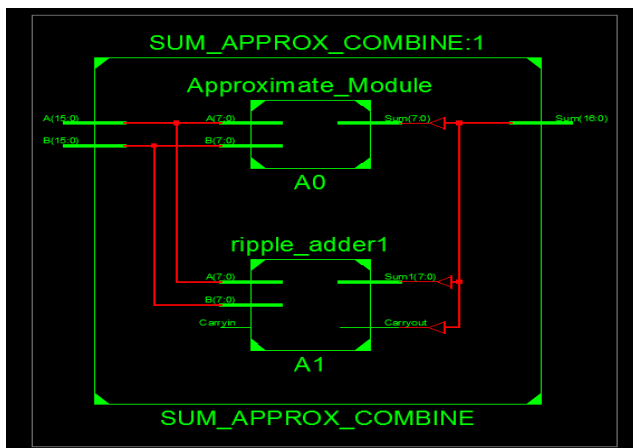


Figure 8: ETA schematic

6. Result & Analysis

In this section we represent hardware result in form of Lut, Delay and frequency. All hardware analysis is done on Vertex-6 45 nm based FPGA on Xilinx tool.

Hardware Analysis:

Here hardware analysis is done on 45nm based FPGA in term of:

- LUT
- DELAY
- FREQUENCY

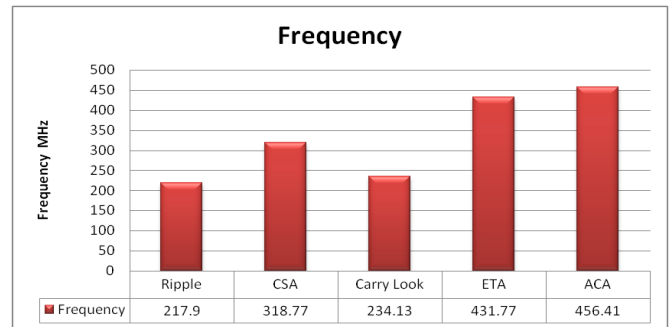


Figure 9: Hardware analysis for frequency

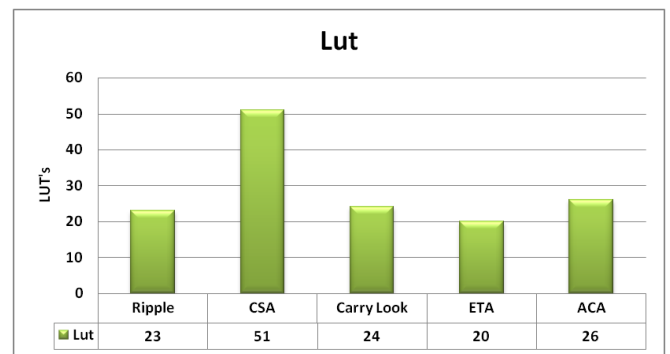


Figure 10: Hardware analysis for LUT

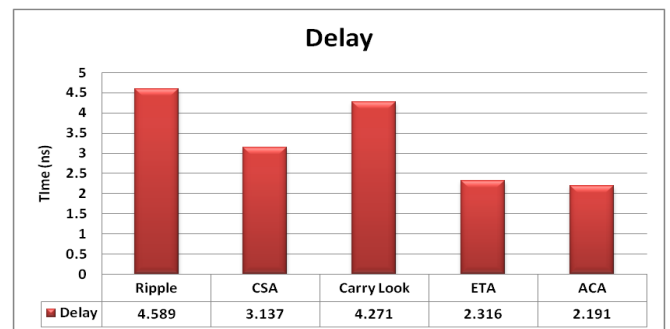


Figure 11: Hardware analysis for Delay

There is approximately 20-30% improvement is done on ACA in terms of delay as compare to other architecture.

7. Conclusion

In this paper a complete study is done on different kind of adder, which is combination of accurate and approximate adder. Here as we know there is no need of accurate system for such kind of graphics based application so there is no need of accurate adder. But according to previous existing approach still there is problem of hardware complexity and power consumption. Still there is some improvement we can do on this approximate adder architecture. According to our study we can design one approximate adder which is 16 bit. As we know half and full adder are basic building block of any adder architecture so we can change those existing architecture and we can save more power and hardware unit.

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