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Current Rebuilding Concept Applied to Boost CCM for PF Correction

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Abstract: ***Nowadays, power factor correction circuits are more important than before in applications such as home appliances, general power supplies for electric products, because the harmonic pollution is getting larger due to a drastic increase in digital product demands. Power factor correction (PFC) is necessary for switched mode power supply in order to comply with the requirements of international standards, such as IEC-1000–3–2 . A predictive algorithm strategy suitable for digital implementation of PFC is proposed in this paper. In the proposed digital control PFC algorithm is that all the duty cycles required to achieve power factor are calculated in advance by using a predictive algorithm. In this method, the switching frequency of the PFC does not directly depend on the processing speed of the digital controller. Therefore, a relatively low cost microcontroller can be used to realize digital control PFC system operating at high switching frequency. Input voltage feed-forward compensation makes the output voltage insensitive to the input voltage variation and guarantees sinusoidal input current even if the input voltage is distorted.***

Keywords: power factor correction (PFC), predictive algorithm, digital control PFC strategy**.**

1. Introduction

Power factor correction need has grown these days due to the increase in the harmonic pollution caused by various digital appliances, personal computers, switch mode power supplies. Stabilized power supply products which are used in the personal computers, laboratories, before releasing into to the market should meet specified standards such as IS 7204. PFC helps achieve these specified standards. In addition it increases the capacity of power system and efficiency by reducing harmonics being added to the line by the electrical appliances, reduces the customers power bill.

Various control techniques have been developed to achieve PFC. The advantages of the digital control PFC over analogue control PFC strategy are (1) digital control can implement more complicated algorithms (2) ease of programmability (3) use of less number of components (4) better performance can be achieved in digital control PFC than in analogue control PFC for the same cost.

Most of the digital control PFC use average current mode control technique to achieve pf correction. One of the disadvantage in digital control strategy is that the switching frequency is limited by the speed of the processor chip.

In the proposed digital control PFC a predictive algorithm suitable for digital implementation is developed to achieve unity power factor. All the duty cycles that are required to achieve pf correction are calculated by the predictive algorithm in advance. The switch of the boost converter is controlled by these calculated duty cycles to achieve sinusoidal current waveform. An important feature of the proposed digital control PFC is that boost converter can be controlled by high switching frequency which is not directly dependent on the speed of the controller. Input feed-forward technique is embedded to get stabilized output and smooth sinusoidal input current waveform even when the input voltage is distorted.

In this paper all the control techniques that are previously implement are discussed in the section 2. The mathematical analysis, feed-forward compensation, predictive algorithm are discussed in section 3, 4, 5 respectively. Simulation results are given in section 6.

2. Literature Survey

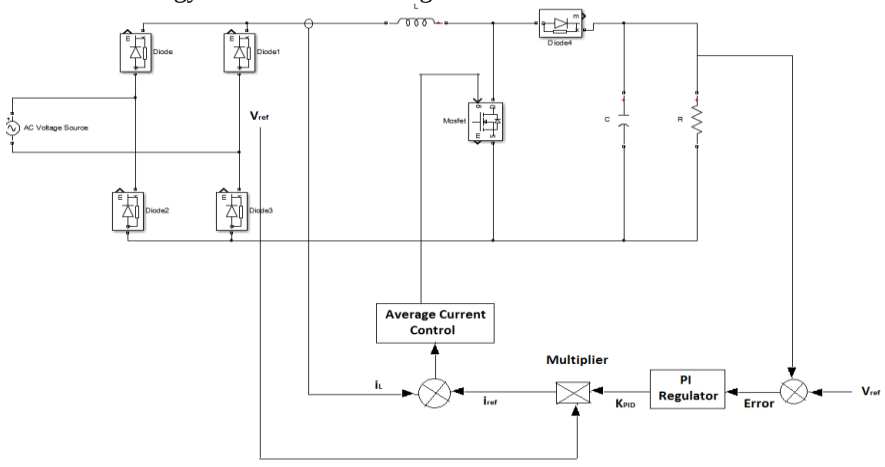

Figure 2: (a) Circuit diagram of current mode control

Delay due to sampling time and the processing time limits the switching frequency in the conventional digital control PFC systems. Fig 2 (a) shows the average current mode control. It is the most used conventional analog control technique. From Fig 2 (a) the average inductor current i_L is forced to follow the reference current i_{ref} which is proportional to the rectified voltage so that the unity power factor is achieved. The output voltage is compared with the reference voltage which gives error signal. This error signal is the input to PI regulator. Output of PI regulator and the average value of rectified voltage is multiplied giving rise to the reference current equation which depends on the rectified voltage value and the output voltage. This reference current value is compared with average value of the inductor which is an input to the average current control strategy. The average current control block decides the duty cycle. The duty cycle is calculated such that unity power factor is achieved. In single sampling in single period method (SSSP) a 50 kHz switching gate signal is controlled by the controller processing speed of 20 MHz.

Average current mode control includes sampling current and voltage, calculation of voltage error, PI regulation of error signal, calculation of reference current, calculating the duty cycle to achieve PFC. Apart from these there are also operations such as PWM implementation in ports. It is estimated that to do all the above mentioned operations there are about eleven mathematical equations involved. All these operations must be done in every switching cycle which is iterative. Because this process is iteratively running in every switching cycle the controller is almost tied up by all these operations and calculations. This is how the switching frequency is limited by the processing speed of the controller. This is the disadvantage which is common in most of the digital PFC.

One of the solution given for the above mentioned disadvantage was to update the duty cycle once in several or several tenths of switching cycle. The main aim to come up with this solution was to reduce the computation time and increase the switching frequency. Using this method the same duty cycle is applied in several or several tens switching cycles so that computation requirement for updating the duty cycle is reduced but the harmonics in the line current were increased in the boost PFC controlled by this method.

In another PFC control method two loops were used one open loop and other closed loop which were paralleled together. The open loop determines the duty cycle component based on the input voltage and output voltage. The closed loop parallel with the open loop and determines the second duty cycle component. The calculation of the second duty cycle by closed loop considers a small amount of variation in loading conditions. The closed loop function in this method was similar to that of current mode control, hence the duty cycle still need to be calculated in every switching cycle. Therefore the computation requirement was no less than that in the digital implementation based on the current mode control.

There was a predictive current control program technique which was used to implement PFC. The duty cycle for the next switching period is predicted based on the sampled current, input and output voltage and duty cycle in the present switching period. In this strategy also the duty cycle had to be calculated in every switching cycle similar to that of current mode control.

After analysing all the methods mention above with respect to PFC it can be concluded that :

(1) Switching frequency is limited due to the sampling time, processing time and large number of computation required.

(2) Even at low switching frequency the controller will be tied up with PFC stage in switch mode power supply. In digital PFC control strategy for switching frequency of 100kHz one switching cycle will be 1µs. if the duty cycle is 0.5 all the computations should be finished in 0.5 µs. This puts a big constraint on the speed of the controller. As the speed requirement in the controller increases so thus its cost also increases. Thus the digital control of PFC suffers from cost constraint of the controller.

(3) Even if we select the fastest digital controller it cannot match the speed of the analog controlled PFC systems.

There were alternative methods to overcome the above drawbacks of the digital control PFC. The first approach was digital controller combined with the analog PFC control chip. In this approach the analog IC was used in the inner loop and the duty cycle was directly calculated by analog circuit. The digital controller was used in the outer voltage loop. The digital controller provides the reference current signal to the analog IC. Thus the digital controller only handles the low frequency tasks for the outer voltage loop. Therefor the switching frequency does not depend on the speed of the digital controller and the high switching frequency could be achieved. The disadvantages of this method included complication of the controller circuit and the cost was increased as both analog and digital IC were required.

The second approach was to use FPGA along with the analog IC for digital converter. The control algorithm was a digital version which was specially coded to suit FPGA implantation. The switch turns on at the beginning of every switching period and off when the mean value of the input current reaches the reference value. The mean value of the input current is the sum of the input current samples divided by the number of samples in one switching cycle. To guarantee the resolution of the duty cycles are quick a fast ADC is required in the integral operation for the calculation of input current mean value. This is why the control circuit cost increases. The drawbacks was that a compromise had to be done between the switching frequency and duty cycle resolution. Therefore switching frequency was limited as the duty cycle resolution had to be maintained at a satisfactory level.

Stored duty cycle ratio (SDR) control is another control method which is offline. The duty cycles were calculated in advance depending on the power balance equation of boost converter. These duty cycles were stored in the memory which were used to control the switch to achieve PFC. This method was unique and as it was offline approach it did not require the current and input voltage sensing or CPU to realize the control circuit.

In the older version of SCR control a set of duty cycles to control the switch were stored in the memory. This means only one operating point was created. At this operating point the input current could exactly follow the sinusoidal waveform. This was because the offline duty cycle calculation was based on a specific operating point.

In the controlled version of SDR the operating points were raised to eight that is eight sets of duty cycle were used to control the switch. Now there were 8 operation points where the input current could follow and result in exact sinusoidal waveform. As the operating points were limited to eight the input voltage got narrowed down. But the power factor correction achieved by this method was around 0.99.

The control technique used in my project is online PFC control circuit. The online strategy ensures sinusoidal current waveform even when the input voltage is distorted and also wide range of input voltage is ensured as feed-forward voltage technique is introduced in project control strategy. The uniqueness of the project is that only voltage control loop is used in the control strategy whereas in all the above mentioned control techniques current control loop was used. Current control loop was clearly explained using the average current control with its diagram. The sinusoidal shaped of the waveform will be guaranteed by the predictive algorithm not the current feedback control.

3. Mathematical Analysis

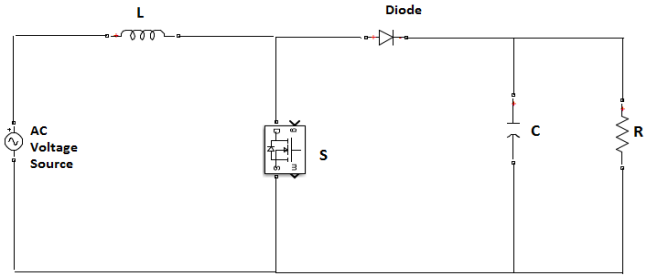

Figure 3: (a) Circuit Diagram of Boost Converter

The boost converter circuit diagram is shown in the Fig 3 (a). The mathematical analysis will be carried on the following assumptions :

1) It operates in continuous conduction mode
2) The switching frequency is greater than line frequency hence the input voltage can be assumed constant over a switching cycle

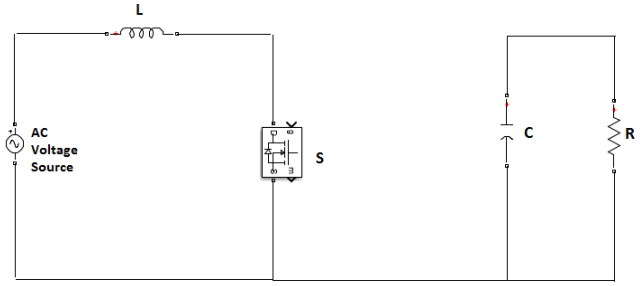

Figure 3: (b) Boost converter switched on

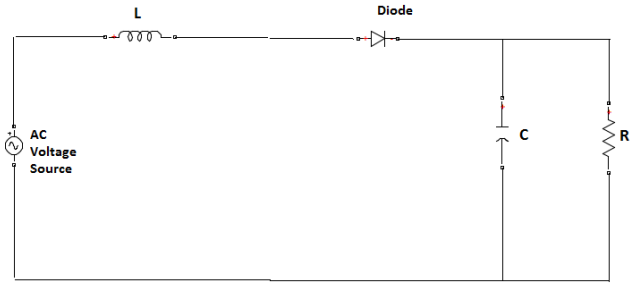

Figure 3: € Boost converter switched off

Fig 3 (b) and Fig 3 (c) shows the circuit topology when switched on and off respectively. From Fig 3 (b) the input voltage is dropped across the inductor given by the following equations

$$L\frac{di_L}{dt} = V_{in} \qquad t_k \le t < t_k + d_k T_s \quad \text{.....1}$$

$$L\frac{di_L}{dt} = V_{in} - V_o \qquad t_k + d_k T_s \le t < t_{k+1} \quad \text{.....2}$$

Iterative inductor current equation

$$i_L(k+1) = i_L(k) + \frac{V_{in}(k)T_s}{L} - \frac{V_o(k)\big(1-d(k)\big)T_s}{L} \quad \text{.....3}$$

Where d (k) and Ts are the duty cycle and switching period. $V_{in}(k)$ is the input voltage in k^{th} switching cycle. $I_L(k)$, $i_L(k+1)$ are inductor current at k^{th} and $(k+1)^{th}$ switching cycle. PFC will be achieved when the inductor current follow the reference current. The reference current is proportional to the rectified input voltage. Meanwhile the output voltage should follow the reference voltage. The equation form of representation is given by

$$V_o(k) = V_{ref} \quad \text{.....4}$$

$$i_L(k+1) = i_{ref}(k+1) \quad \text{..... 5}$$

$$i_L(k) = i_{ref}(k) \quad \text{..... 6}$$

The duty cycle at k^{th} period is given by

$$d(k) = \frac{V_{ref} - V_{in}(k)}{V_{ref}} + \frac{\big[i_{ref}(k+1) - i_{ref}(k)\big]\frac{L}{T_s}}{V_{ref}} \quad \text{..... .7}$$

Where

$$i_{ref}(k) = V_{PID}\ |\sin(\omega_{line} t_k)\ | \quad \text{..... 8}$$

V_{PID} is the output of the PID regulator which will be determined by the closed voltage loop and it represents the peak value of the rectified sine waveform. Abs (sin ω_{line} t_k) is the rectified waveform with line frequency. Sine waveform is generated by the controller using the sine wave look up table. The gain of the PID regulator is decided by the rated loading which can be easily determined.

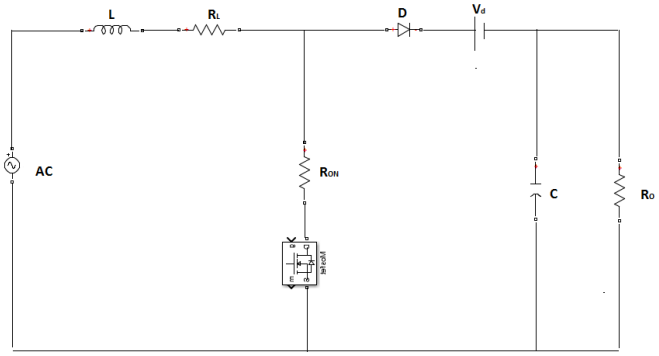

Figure 3: (d) Exact model of boost converter

Fig 3 (d) show the exact model of the boost converter which is used to derive the accurate expression for the inductor current. This circuit is used in the predictive algorithm. As we use this circuit in the predictive algorithm inductor resistance, switch resistance, drop across the diode are all considered while deriving the equation.

Based on the exact model of the boost converter the equation of duty cycle is given by

$$d(k) = d_1(k) + d_2(k) \quad \text{.....9}$$

$$d_1(k) = \frac{(V_{ref} + V_{ripple}(k) + V_d) + R_L i_{ref}(k) - V_{in}(k)}{(V_{ref} + V_{ripple}(k) + V_d) - R_{on} i_{ref}(k)} \quad \text{.....10}$$

$$d_2(k) = \frac{[i_{ref}(k+1) - i_{ref}(k)]\frac{L}{T_s}}{(V_{ref} + V_{ripple}(k) + V_d) - R_{ON} i_{ref}} \quad \text{.....11}$$

Ripple in output voltage is given by the expression

$$V_{ripple} = -I_o \times \frac{1}{2\omega_{line} C} \sin(2\omega_{line} t_k) \quad \text{.....12}$$

where Io is the load current. Duty cycle equations 7 and 9 are used in the predictive algorithm. The simple forms of the duty cycle derivations are done using the Fig 3 (a) and Fig 3 (d) require low calculations and their digital implementation is also easy. The test results using these two equations are turned out to be good. Switching losses and switching delay are not included in the model as they would make the algorithm complicated to implement and also the time require for the computation part will also increase.

Ideally the mean value of the inductor current should follow the reference current. The approximations were done to calculate duty cycle keeping this in mind. If the inductor current ripple in one switching cycle is very very small compared with the amplitude of the inductor current the digital algorithm works well. This approximation is easier to be satisfied for high load than for light load. This is the reason why the power factor for the light load is less than that for higher loads.

In the expression for duty cycle 7 is made up of two components. The first component is called voltage component and it is given by the equation

$$d_1(k) = \frac{V_{ref} - V_{in}(k)}{V_{ref}} \quad \text{.....13}$$

This voltage component alone is not enough to accomplish the objectives of the project because it is derived from open loop parameters due to which automatic voltage regulation at the output is not possible. Secondly it does not consider the energy stored or released from the inductor hence unity power factor cannot be achieved. The second component is called as the current component given by the following expression

$$d_2(k) = \frac{[i_{ref}(k+1) - i_{ref}(k)]\frac{L}{T_s}}{V_{ref}} \quad \text{.....14}$$

If the numerator of the equation 14 is observed it is similar to the voltage across the inductor. The change in the inductor current is similar to the difference in reference current in successive iterations. The change in time is similar the switching time interval. The differentiation of a sine wave in one switching period takes cosine wave shape. The integral of voltage across the inductor gives back the sinusoidal wave shape. In the reference current equation its peak amplitude is the PID regulators output. So current component corresponds to the voltage feedback. Introducing current component not only helps in output regulation but also achieve sinusoidal wave shape of line current

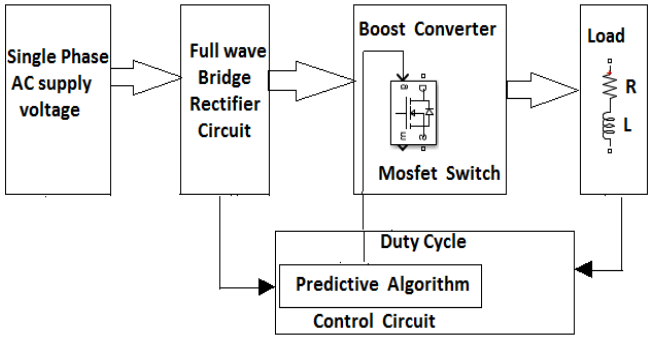

Figure 3: € Block Diagram of PFC circuit

Fig 3 € shows the block diagram of the PFC circuit used in the project. The single phase supply is rectified by the full bridge rectifier circuit. The peak value of the rectified voltage is sensed and also its zero amplitude point. The peak value of the rectified voltage is used in the predictive algorithm. The output of the multiplier is the reference current. Its amplitude is decided by the output of the PID controller in the voltage loop. Its phase and wave shape is determined by zero amplitude detector and the sine wave look up table. The output voltage is regulated using the closed loop control consisting of PID controller. The feedback signal is the output voltage. The output of the control circuit is the gated signal for the switch. As we can observe that current control loop is not used in the calculation of the duty cycle. The duty cycles required are calculated in advance by the predictive algorithm to achieve unity pf in a half line period.

4. Feed-Forward Compensation

Feed-forward compensation is used to improve two parameters (1) to make output voltage insensitive to the input voltage variations (2) compensating the calculated duty cycles to ensure sinusoidal line current when the line voltage is

distorted. Feed-forward compensation improves both steady and dynamic characteristics of the overall circuit in every switching cycle.

The equations 7 and 9 give the ideal sine shaped as it is generated from the sine wave look up table. Hence the duty cycle can be calculated in advance. The input voltage may contain distortion due to harmonics in the grid. In voltage feed-forward compensation the instantaneous value of the input voltage is sensed and used to modify the duty cycle. The duty cycle updated when there is distortion in the voltage is given by the expression

$$d_{new}(k) = d(k) + \Delta d(k) \quad \ldots\ldots 15$$

Where $d_{new}(k)$ the duty cycle sent to control the gate of mosfet switch. d(k) is the calculated duty cycle from equation 7 and $\Delta d(k)$ is the compensated component. Its expression is given by

$$\Delta d(k) = \frac{\Delta V_{in}(k)}{V_{ref}} \quad \ldots\ldots 16$$

Where

$$\Delta V_{in}(k) = V_{in}(k) - v_{in}(k) \quad \ldots\ldots 17$$

Is the input variation. $v_{in}(k)$ is the sensed instantaneous value of the input voltage $V_{in}(k)$ is the input voltage used in the algorithm. The look up table generates the ideal sine waveform. The instantaneous value of the input voltage can be stored in the look up table which can be used in the next half line period. The harmonics in the input voltage can be represented by the Fourier transform equations as

$$v_{in}(k) = \left| V_1 \sin(\omega_{line} t_k) + \sum_{i=3,5,\ldots}^{\infty} V_i \sin(i\,\omega_{line} t_k) \right| \quad \ldots\ldots 18$$

The variation between the ideal input voltage $V_{in}(k)$ and the feed-forward input voltage $v_{in}(k)$ is

$$\Delta v_{in}(k) = \left| V_1 \sin(\omega_{line} t_k) \right| - \left| V_1 \sin(\omega_{line} t_k) + \sum_{i=3,5,\ldots}^{\infty} V_i \sin(i\,\omega_{line} t_k) \right| \quad \ldots\ldots 19$$

The duty cycle are updated after the compensation given by the equation's 15 and 16.
The duty cycles calculated after feed-forward compensation is given by

$$d_{new}(k) = \frac{\left[i_{ref}(k+1) - i_{ref}(k)\right]\frac{L}{T_s}}{V_{ref}} + \frac{V_{ref} - \left| V_1 \sin(\omega_{line} t_k) \right|}{V_{ref}} + \Delta d(k) \quad \ldots\ldots 20$$

The diode voltage drop is given by

$$v_d(k) = d_{new}(k) V_o \quad \ldots\ldots 21$$

$$v_d(k) = V_{ref} + \left[i_{ref}(k+1) - i_{ref}(k)\right]\frac{L}{T_s} - V_1 \sin(\omega_{line} t_k) + \sum_{i=3,5,\ldots}^{\infty} V_i \sin(i\,\omega_{line} t_k) \quad \ldots\ldots 22$$

5. Predictive Algorithm

A system always has two states one steady state and other dynamic state. Adjustment of controlled parameters close to the expectation while the system is starting or the response for the change of the load current or input voltage depends on the dynamic characteristics. Overshoot is a common phenomenon while starting the system. When the controlled parameter in this case the output voltage, reaches the expected value the steady state is reached. Steady state characteristics differs from one system to another. In dc-dc converter system ripple voltage are the important parameter that decides the steady state point of the system. For PFC system PF is the deciding factor. Hence for a PFC system optimal control should meet both fast transient response and high PF value in different cases. Two different control algorithm should be coded to achieve PF condition.
The dynamic algorithm written for Boost PFC aim at regulating the output voltage as fast as possible in different cases. The rectified voltage is a half sinusoidal waveform in which the output voltage varies quickly near the peak value of the input voltage where the larger duty ratio provided by the dynamic algorithm is needed to increase inductor current and improve transient response.

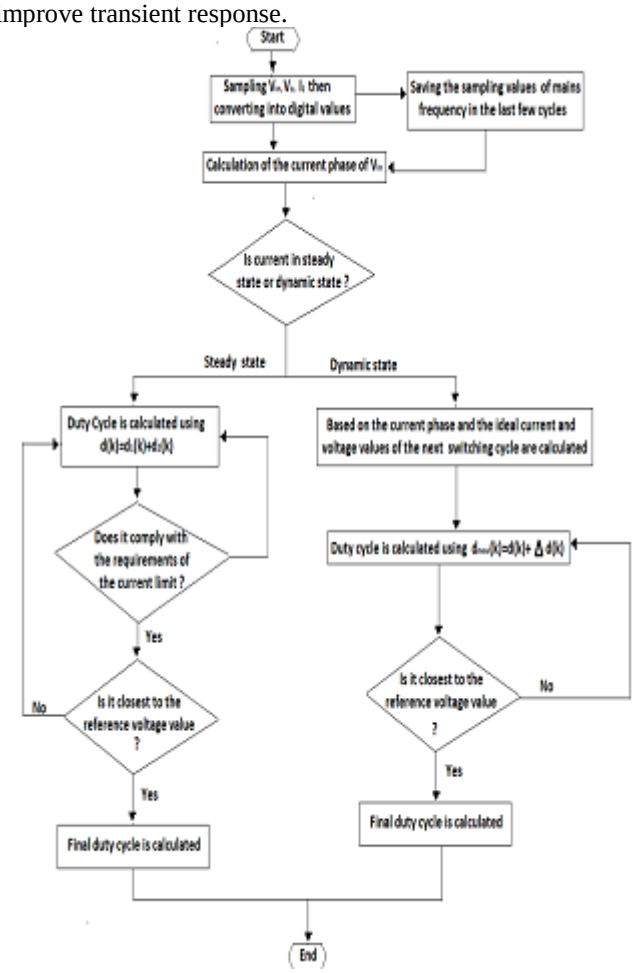

Figure 5: (a) Predictive Algorithm

The steady state algorithm should do two jobs. First make the output voltage nearly same as the reference voltage. Second make the inductor current follow the input voltage so that PF is achieved. The phase and amplitude of V_{in} (t) decides the value of the inductor current as per the equation written for

$i_L(k+1)$. This inductor current tracks the input voltage according to the predictive algorithm. The duty ratios are also calculated. The influence of the time delay is ignored.
The working of the control algorithm explained step by step as follows:

Step 1: All the values of voltage and current are acquired. These values are digitised and a copy of these values is stored in a memory location. These sampled parameters affect the steady state and transient characteristics of the whole circuit. It is prerequisite to evaluate the performance of various algorithms in the determined parameters. Updating the sampling at the beginning of every switching cycle can avoid the accumulation of prediction error.

Step 2: The variations that occur in the input voltage are period. Based on the previous values of the voltage variations the phase of the current is decided. This requires the access of the input port to read at least half of the line frequency data values to detect phases.

Step 3: The branching of the program flow to dynamic or steady state depends on the allowable difference between the expected voltage value and the current voltage value. If the difference is small then the program branches to steady state or else it branches to the dynamic state calculations.

Step 4: If the program branches to the dynamic state calculations then the output voltage is passed though the PI regulator in order to check for any overshoot. As per the equations of $i_L(k+1)$. When the inductor value overshoots the duty cycle is calculated when output voltage is near to the reference voltage value. When inductor current value is not overshot the output voltage value is tried to bring near to the reference voltage value in the next cycle. When duty cycle meets the above conditions the speed of response time increases.

Step 5: In steady state first the input current value is made to track the input voltage curve. Thereafter the duty cycle is calculated by using the prediction algorithm. $I_L(k+1)$ is calculated according to the line frequency of input voltage and its phase. The successive iteration values of the inductor current can be calculated and hence the duty cycles also. The number of iterations depend on the line frequency values and the number of samples used in the data acquisition. The optimal duty cycle ratio is obtained when the value of the inductor current is such that is perfectly tracks the shape of the input voltage.
The predictive algorithm runs once in every switching cycle to calculate the duty ratio.

6. Simulation

Simulation is performed in MATLAB to verify the digital control PFC strategy. The simulation is carried out for an input voltage of 160 V and 60Hz frequency. The boost converter is simulated with a capacitance value of 300 µF and inductance of 2 mH. The value of reference voltage is 390 V.

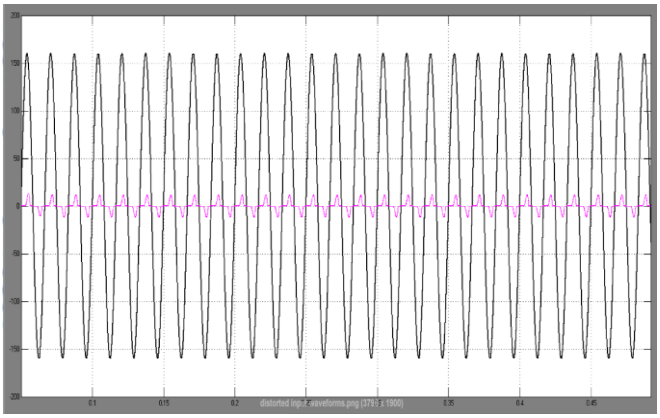

Figure 6: (a) Without PF Input waveforms

Fig 6 (a) show the input voltage and current waveforms without PF correction. The load used is RL- type. Form the waveforms it is clear that the current waveform in pink color is distorted.

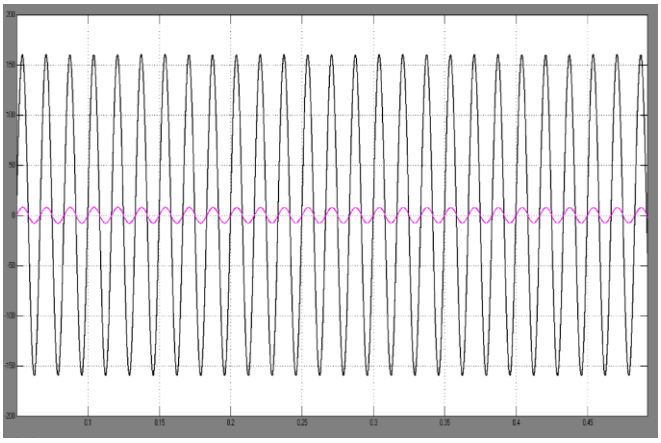

Figure 6: (b) PF corrected Input waveforms

Fig 6 (b) shows the voltage and current waveforms after PF correction. The same RL load is used. From the waveforms it is clear that the current waveform in pink color is smoothly sinusoidal. Hence predictive algorithm is verified.

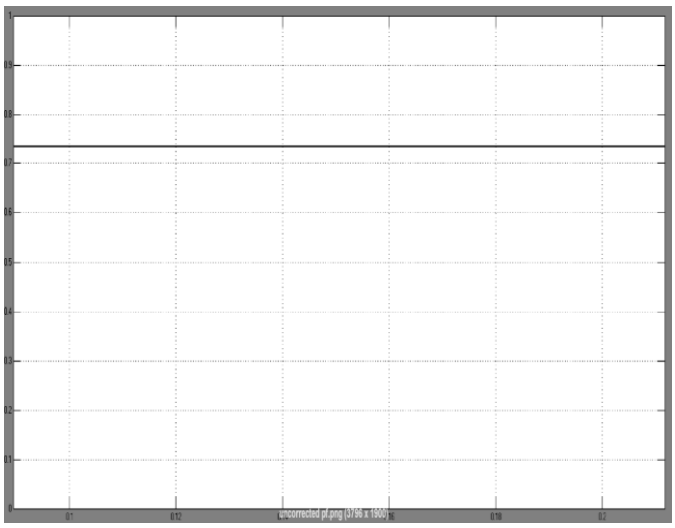

Figure 6: € PF of uncorrected Input waveforms

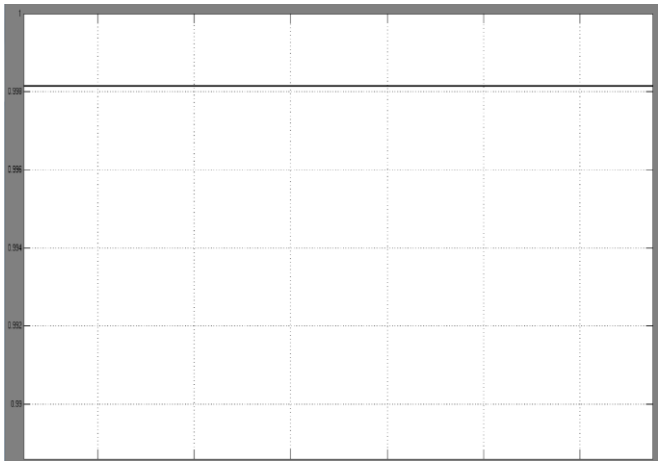

Figure 6: (d) PF of corrected Input waveforms

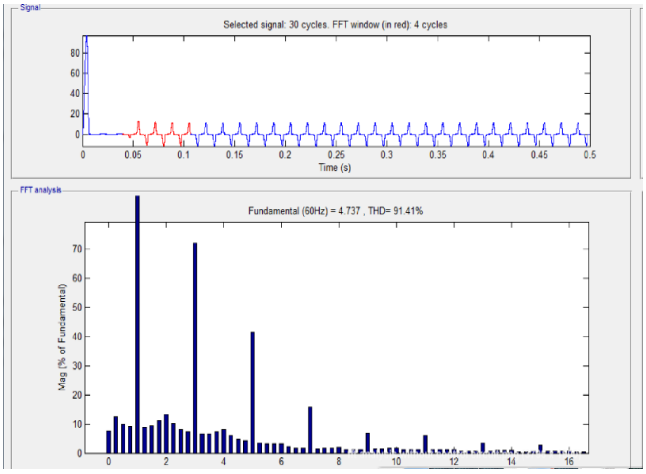

Figure 6: € FFT of uncorrected Input waveforms

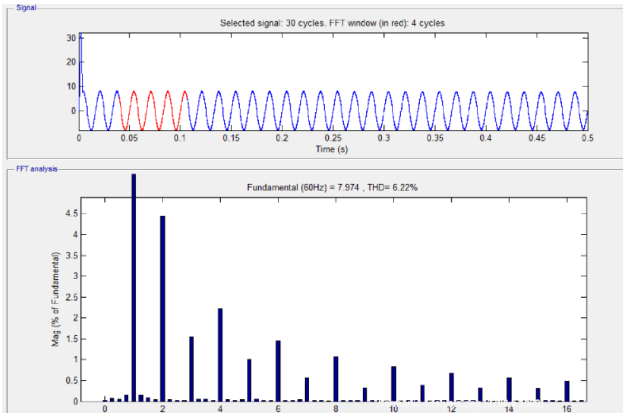

Figure 6: (f) FFT of corrected Input waveforms

7. Conclusions

A digital control PFC strategy to achieve unity PF included predictive algorithm. All the duty cycles required to achieve the objective were calculated in prior by predictive algorithm. The boost converter was controlled by these calculated duty cycles. A feed-forward compensation was also included to get a stabilized output and a smooth sinusoidal waveform even when the input voltage contained distortions. The simulation results show in the section 6 clearly verifies all the objective of the digital control strategy. Without PF correction the input current waveforms were distorted, the pf was 0.77 with THD of 91.4 % for a RL load. After the digital PF correction a smooth sinusoidal input current waveform was observed, pf was improve to 0.998 and harmonics were reduced to THD=6.22%. Hence the digital control PF strategy is verified.

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