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An Improved Feedthrough Logic for Low Power and High Speed Arithmetic Circuits

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Abstract: ***This paper presents the design of low power and high speed circuit using a new CMOS logic family called feedthrough logic. FTL arithmetic circuits provides for smaller propagation time delay when compared with the standard CMOS technologies. The proposed circuit has very low dynamic power consumption and lower propagation delay compared to the recently proposed circuit techniques for the dynamic logic styles. A long chain of inverters (20 stages) and a 16-bit ripple carry adder (RCA) is designed by modified feedthrough logic. Then comparison analysis has been carried out by simulating the circuitry in 180nm CMOS process technology from TSMC using Tanner EDA 14.11 tool.***

Keywords: Feedthrough logic (FTL), high speed, low power adder, CMOS logic circuit.

1. Introduction

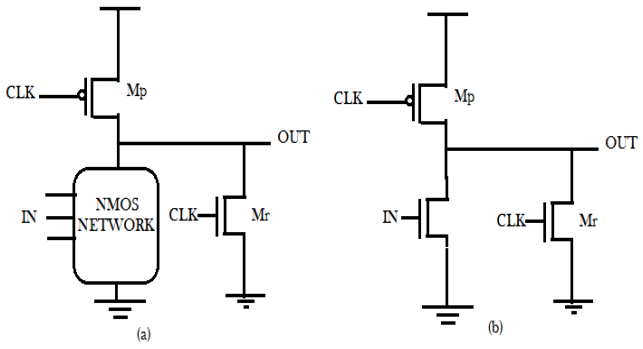
In the past few years, as transistor dimension shrinking gradually approaches to its physical limit, the scaling of CMOS technology has slowed down. At this condition traditional constant field scaling i.e. all device dimensions and voltage supply can be scaled down by factor 1/s, can no longer be applied. Most of the new CMOS process technologies have approximately same supply voltages nowadays. But modern era have same requirement as earlier i.e. high speed of operation and low power consumption. To fulfill this requirement the only solution is design style of CMOS logic families. Means we have to design a circuit in such a way that it should consume less power and it should have low propagation delay. Although CMOS based logic have low power dissipation, its propagation delay is high. The evolution of CMOS is done in the form of dynamic logic. But dynamic logic suffers from false detection when large number of cascading required.

In order to enhance the performance of dynamic logic circuit in terms of power and speed and to remove false detection problem, a new logic family called feedthrough logic (FTL) was proposed in [3]. This logic works on domino concept along with the important feature that output is partially evaluated before all the inputs are valid, and due to use of extra supply voltage [3] very fast evaluation in computation blocks have been achieved.

The FTL concept was successfully used for design of high speed and low power arithmetic circuits in [2]. We also extend our research to high speed and low power circuits and analyzed the 16-bit ripple carry adder (RCA) sensitivity against capacitive load (fF) and temperature (^{o}c). Our results showed substantial performance improvement in modified FTL structure, with respect to basic FTL structure without losing the need of low power dissipation. In this work we proposed a modified FTL structure and comparison analysis has been taken with respect to convention FTL structure.

2. Basic FTL Principle

The basic structure of FTL is shown in Fig. 2 (a). It consist a NMOS reset transistor Mr for resetting the output node to low logic level, a pull up PMOS load transistor Mp and an NMOS block. Mp and Mr controlled by the clock signal CLK. The basic principle of operation of a FTL circuit was presented in [3] and is briefed here. When CLK is high(reset phase), Mr turned on and the output node pulled to ground through Mr. When CLK goes low (evaluation phase) Mr is turned off and the output node conditionally evaluates to logic high (V_{OH}) or low (V_{OL}) depending upon input to NMOS block. A long chain of inverter (1st to 29th stages) is designed using FTL structure. When CLK=1, all the output nodes are at logic zero. When CLK goes low, the output node of all inverters rises to the gate threshold voltage V_{TH}. At this point any small variation in the input node causes a fast variation in voltage at the output node.



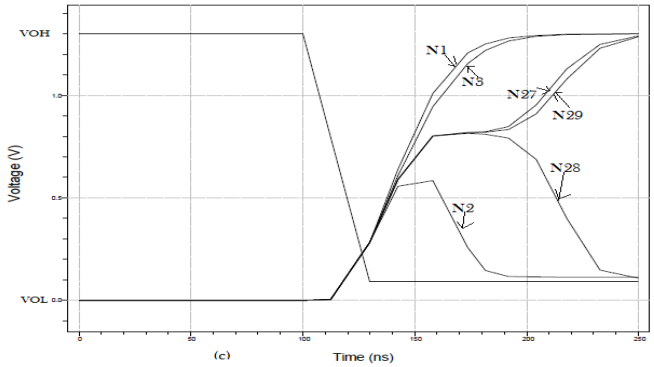


Figure 2: (a) Basic FTL structure, (b) Inverter using basic FTL, (c) Output waveform of 1st to 29th inverter stages

3. Proposed Modified FTL

The proposed modified circuit is presented in fig.3 This circuit reduces V_{OL} by using additional PMOS transistor M2 in series with M1, and NMOS transistors M3 and M4 prevents switching current through NMOS block . The operation of this circuit is similar to that of FTL in [3]. During reset phase i.e. when CLK = 1, output node is pulled to $V_{DD}/2$ through M5, when CLK goes low (evaluation phase) M5 is turned off and the output node conditionally evaluates to logic high (V_{OH}) or low (V_{OL}) depending upon input to NMOS block. If the NMOS block evaluates to high then output node pulled toward V_{DD} i.e. V_{OH} =V_{DD}, otherwise it goes at logic low i.e. V_{OL}.

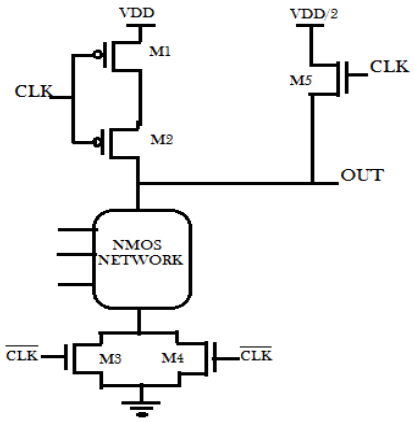


Figure 3: Proposed Modified FTL structure

4. Performance Analysis of Proposed FTL Logic

The proposed FTL structure has been verified against basic FTL structure in [3] by designing a long chain of inverter consisting 20 stages. We have used 180nm CMOS process technology model file from TSMC at 25^0C. Power supply V_{DD} is constant for all simulations and is equal to 1.8V. Circuits are simulated in Tanner EDA 14.11 tool. As The sufficient condition for equal propagation delay i.e. $t_{plh} = t_{phl}$ in CMOS circuits as described in [1] may be given as:-

$$V_{T,n} = V_{T,p} \quad \text{.....(1)}$$

and,

$$k_n = k_P \text{ (or } W_p/W_n = \mu_p/\mu_n) \quad \text{.....(2)}$$

since electron mobility is greater than hole mobility ($\mu_n > \mu_p$) so we have used $W_n/W_p = 1.14$ for all our simulations.

Table I shows the dynamic power consumption, average values of propagation delays (tp), and power delay product comparison of proposed modified FTL and the existing FTL in [3] for 10 fF capacitive load at 100 MHz when simulation long chain of inverters (20 stages). The proposed FTL shows 48.7% less power consumption with a speed up factor of 1.32 with respect to existing FTL.

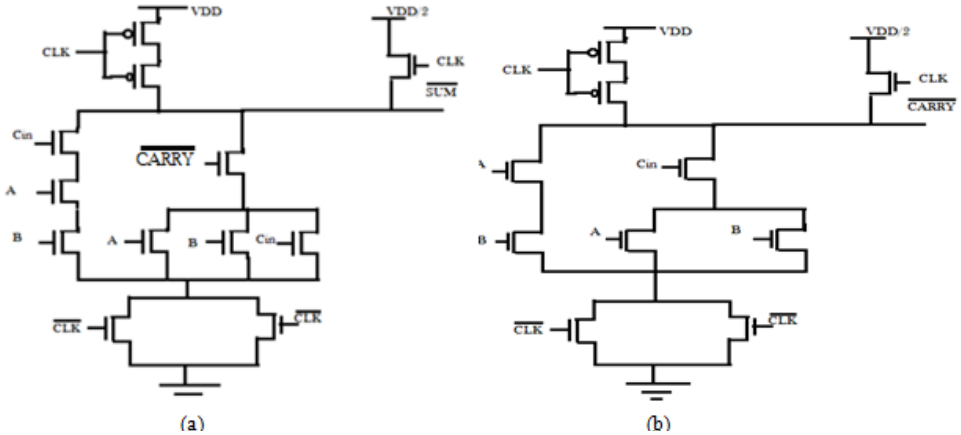
Table 1: Simulation result for FTL and Modified FTL (20 stages of inverter)

Logic Family	Power (µwatt)	Propagation delay (nsec)	PDP (µwatt*nsec)
FTL	887	0.795	705.17
Modified FTL	455	0.6027	274.23

5. 16-Bit Ripple Carry Adder Design and its Performance Analysis

Fig.5.(a),and (b) shows basic sum and carry cell designed by proposed modified feedthrough logic. Simulation is done in 180nm technology at 25^o C using Tanner EDA 14.11 Tool. Bar graph shows power dissipation, propagation delay and PDP of 16-bit RCA using modified FTL and existing FTL.

The Fig.5 (d),(e),(f) shows sensitivity of RCA designed by modified FTL against temperature(^{o}C) and capacitance(fF). Bar graph Fig.5 (c) shows the 16-bit RCA performs fast logic evaluation (1.115 times) and consumes (46%) less power when simulated with proposed modified FTL structure as compare to existing FTL. The clock frequency and capacitive load is same as we have taken in inverter design.



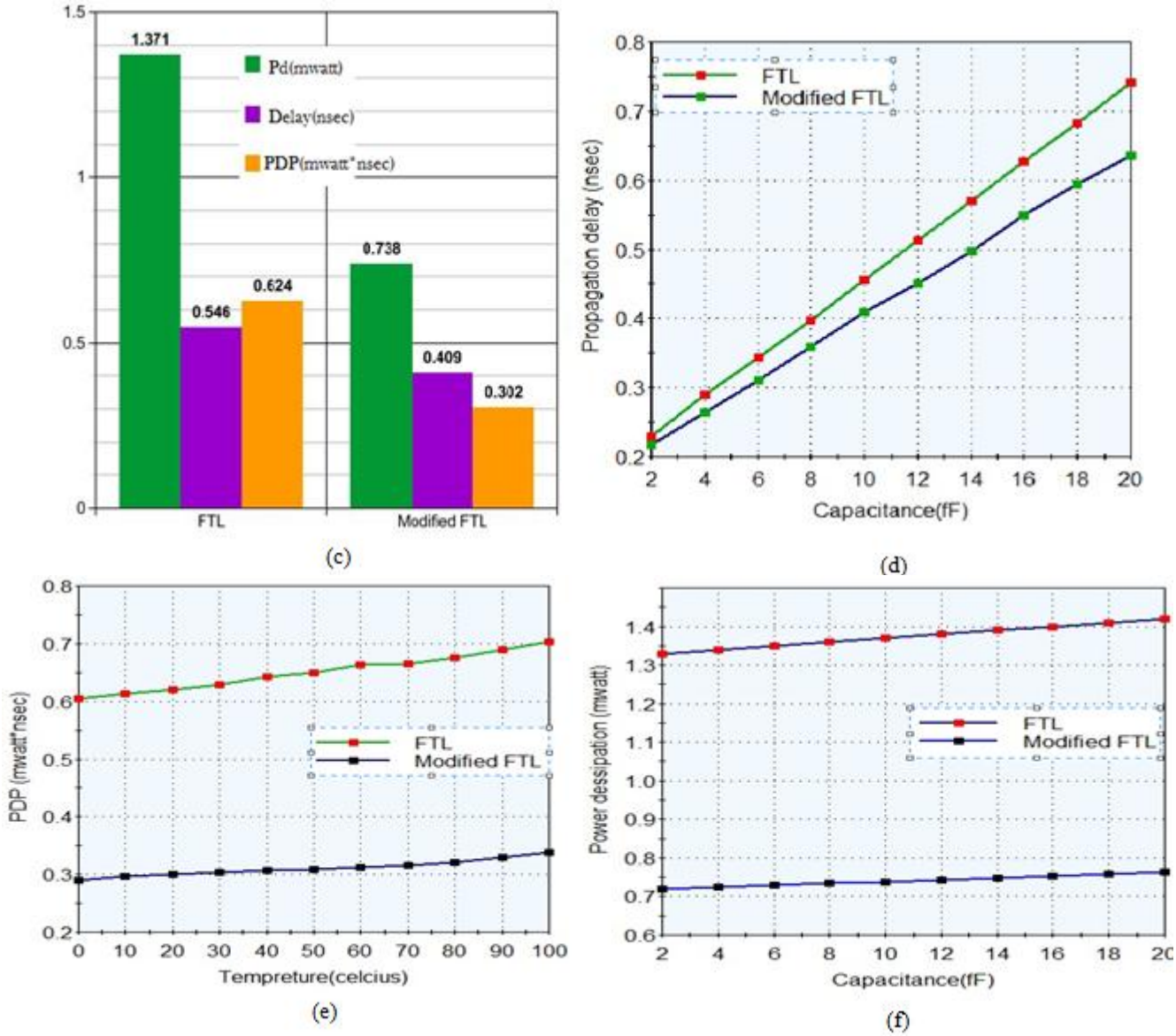


Figure 5: (a) Basic sum cell, (b) Basic carry cell, (c) Output comparison analysis of 16-bit RCA using basic FTL and proposed FTL,(d) Sensitivity of propagation delay against capacitive load, (e) sensitivity PDP against temperature variation, (f) sensitivity of power dissipation against capacitive load.

The power delay product for both the structures is shown in Fig.5(c). We have obtained a sufficiently reduced value of power delay product; hence the performance of proposed modified structure is better than basic FTL structure. Fig. 5(d) shows effect of load capacitance variation on propagation delay. Our proposed structure has less sensitivity against increase in capacitive load than basic FTL structure. Fig.5 (e) shows effect of temperature variation on power delay product and Fig.5 (f) shows effect of load capacitance variation on dynamic power dissipation.

6. Conclusion and Future Scope

In this paper, we proposed a low power and high speed dynamic circuit. The proposed circuit is simulated in 180nm CMOS process technology from TSMC using tanner EDA 14.11 tool. The proposed modified circuit when compared with recently modified circuits it consumes 46% less power without losing the need of high speed. The simulation for a long chain of inverter (20-stage) and 16-bit ripple carry adder is also carried out in this work. The simulation result confirms that for a given load and at same frequency of operation the power delay product of the proposed circuit is much better than that of existing FTL structure. The proposed circuit can be used for designing of low power and high speed processor where high speed and low power consumption is essential requirement.

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