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A Power Efficient Design of Reversible RAM Using Pseudo Reed-Muller Expression

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Abstract: ***Power dissipation is considered as one of the most important factors while designing a circuit. Reversible logic has become a promising technology in low power design. It is because reversible logic utilizes only very less power, thereby leading to less power dissipation. Conventional circuits which are irreversible in nature are subject to very large amount of minimum power dissipation per signal transition. Reversible logic is considered as a computing paradigm in which there is a one-to-one mapping between the input vectors and the output vectors. In this paper we discuss with reversible circuits and reversibility which in future will be considered as a trend towards low power design. Combinational circuits were the primary ones to be implemented using this technique. Later on, few researches also contributed towards sequential circuits. In this paper we implement a Reversible RAM that dissipates less power than the conventional RAM circuitry. Here we use Pseudo Reed-Muller expressions (PSDRM) for the synthesis of the design. There are also various other methods of synthesis. But it has been found that PSDRM circuits are more efficient than other techniques such as Positive Polarity Reed-Muller (PPRM) expression and Fixed Polarity Reed-Muller (FPRM) expression based circuits. By using this technique there is more optimization as well as improvement in other factors such as number of gates, memory usage, garbage output, quantum cost etc.***

Keywords: Reversible logic, Sequential circuits, PSDRM, Garbage output, quantum cost, RAM.

1. Introduction

Landauer [1] states that, conventional circuits dissipate large amount of heat energy during computation due to the loss in information. It has been proved that for each bit of information loss there is kTln2 joules of heat energy; where T is the absolute temperature on which computation is performed and k is Boltzmann's constant. Bennett [2] proved that energy dissipation issues can be reduced if all the gates in the circuits are made reversible. It is because reversible logic makes each and every step of computation to be completely reversible, so that no information is lost at any step of computation. The levels of logic in reversible circuits are significantly high than the standard logic and they are considered as a special case of quantum circuits [7].

Reversible computation can be only made possible by using reversible gates. Most of the gates that we use in digital circuits such as AND, OR, NAND, NOR etc. are considered irreversible in nature. Only NOT gate among them is reversible. Some other reversible gates include the Peres gate, Toffoli gate, Fredkin gate, Feynman gate etc. The commonly used reversible gates are shown in Figure.1. It should be noted that reversible logic circuits must always be designed using minimum number of reversible gates, and with minimum number of constant inputs. Before using synthesis techniques replacement technique was used, where the irreversible parts of the design was replaced by reversible gates [9]. Reversible circuits are of two types that is reversible combinational and reversible sequential circuits. There are

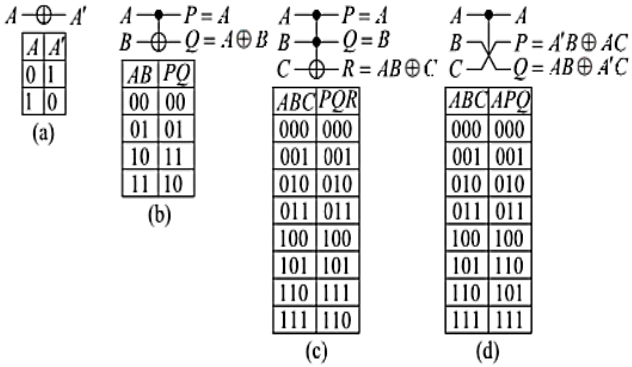

Figure 1: Commonly used reversible gates (a) NOT gate. (b) Feynman gate. (c) Toffoli gate (d) Fredkin gate.

many research attempts focusing on reversible logic synthesis but they are mostly centered on reversible combinational logic synthesis. Only a few researches among them are carried over reversible sequential circuits. Reversible Logic Design is quite different from the traditional Combinational Logic Design. It is important that in Reversible Logic, the number of input and output lines must be equal such that each output line is being used only once thereby making the resulting circuit acyclic. Thus Reversible Logic circuitries consist of n-inputs and n-outputs with one-to-one mapping. By this it is possible to determine the outputs from the inputs and vice-versa. Hence we say that there is a one-to-one correspondence between the input vectors and the output vectors. Reversible logic finds application in fields like low power CMOS, nanotechnology [6], DNA computing, optical computing and Quantum computing. Thus in total Reversible logic can be considered as a new trend in Low power circuitry design.

Here in this paper, we deal with the design of a Reversible

RAM which is synthesized using PSDRM expression. The next state of RAM is expressed in terms of Pseudo Reed-Muller expressions (PSDRM). Prior to PSDRM, the Positive Polarity Reed-Muller (PPRM) and Fixed Polarity Reed-Muller (FPRM) based reversible circuit synthesis was adopted. FPRM-based reversible circuit synthesis method is more efficient than PPRM-based synthesis. Pseudo Reed-Muller (PSDRM) expression is a more generalized class of Reed–Muller expression and requires less or at most equal number of product terms than FPRM expression. Thus we in this paper make use of the effective PSDRM expressions. The rest of the paper is organized as follows. Section 2 gives a brief background on Reversible logic. Section 3 presents Reversible logic synthesis using PSDRM; Section 4 describes the design of reversible LFSR; Section 5 provides the results and discussion obtained by designing the circuit. Finally we conclude the paper in Section 6.

Background on Reversible Logic

A reversible circuit maps every input combination into a unique output combination. This unique mapping implies that a reversible circuit comprise of the same number of inputs and outputs. A reversible logic with n input/output is usually called as an n×n reversible circuit. Thus a network of reversible gates together forms a reversible circuit [8].

We generally start with universal gate libraries and some specification of a Boolean function for conventional (irreversible) circuit synthesis. The primary goal is thus to find a logic circuit that is capable of implementing the Boolean functionality and minimize given cost metric, e.g., the number of gates or the garbage output etc. Hence we can say that reversible circuit synthesis is just a special case in which no fan-out is allowed and all gates must be reversible.

2.1. Cost Metrics

A reversible circuit can be implemented in several ways, resulting in different cost. This section focuses on some of the major cost metrics associated with Reversible circuits and are used to evaluate and compare them.

2.1.1 Gate Count

It refers to the number of gates in total that is required to implement the circuit. It is one of the major cost metric used in the evaluation of reversible sequential circuit [3].

2.1.2 Garbage Output

Some outputs pins are used only to maintain the reversibility of the logic, but are not used as the final outputs or as input to other circuits. These unused outputs are called as garbage outputs.

2.2.3 Quantum Cost

The quantum cost of a reversible gate is referred to as the number of quantum gates or the 1x1 and 2x2 reversible gates required to design the gate. The quantum costs of all reversible such as the 1x1 and 2x2 gates are taken as unity.
A detailed study on different reversible gates is presented in [8]. They can be used for the design of classical gates. Figure.2 shows the realization of classical gates such as AND gate and OR gate using reversible gate.

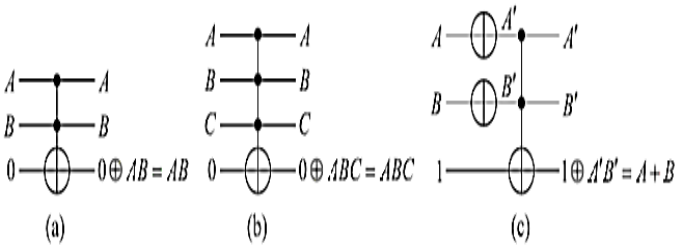

Figure 2: Reversible realizations of classical (a) two-input AND gate, (b) three- input AND gate and (c) two-input OR gate.

The figure also shows the reversible realization of two input and three inputs AND gates. The complexity of reversible circuit design is generally compared in terms of quantum cost. Reversible realization of two-input AND gate requires five quantum cost and two garbage outputs and that of three-input AND gate requires 14 quantum cost and three garbage outputs. Reversible realization of two-input OR gate is shown in Figure 2(c), which requires seven quantum cost and two garbage outputs.

3. Reversible Logic Synthesis

Consider an n-variable Boolean function f (x_1, x_2., x_i,.., x_n) , which can be expanded using following equations:

$$f(x_1, x_2., x_i,.., x_n) = f_0 \oplus x_i f_2 \text{ (positive Davio, pD) (1)}$$

$$f(x_1, x_2., x_i,.., x_n) = f_1 \oplus xi' f_2 \text{ (negative Davio, nD) (2)}$$

If we apply pD expansion on all variables of an n-variable Boolean function f (x_1, x_2., x_i,.., x_n), then we obtain two trees corresponding to positive Davio as well as negative Davio[4]. For example consider a function given as below.

$$f(x1,x2,x3) = \sum(3,4,6,7). \text{ (3)}$$

If we apply equations (1) and (2)in the above example we obtain two trees as given below. Figure.3 shows the positive tree obtained. Similarly we also get a negative tree as shown in Figure.4. After obtaining both the trees we create an arbitrary tree as shown in Figure.5 to synthesis the given functionality.

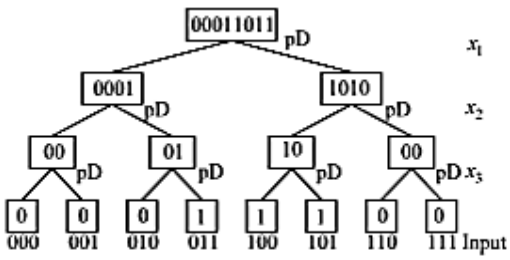

Figure 3: PSDRM tree obtained after applying Eqn.1 on function (3)

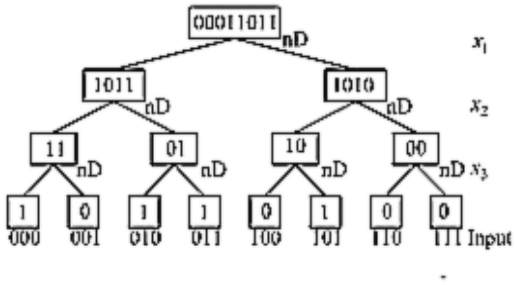

Figure 4: PSDRM tree obtained after applying Eqn.2 on function (3)

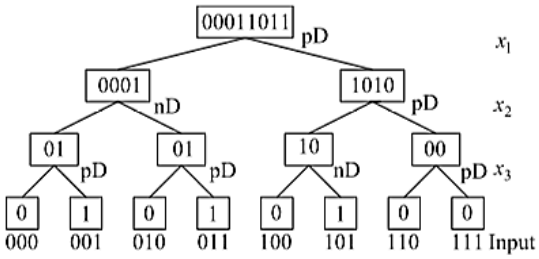

Figure 5: Arbitrary PSDRM tree obtained after applying Eqn.2 on function (3)

The leaves of the tree represent the coefficient vector. The resulting expression is determined from the ones of the coefficient vector and their corresponding input combinations. The resulting expression of the tree of Figure.3 is given as

$$f(x_1,x_2,x_3)= x_2x_3 \oplus x_1 \oplus x_1x_3. \quad (4)$$

Similiarly we can obtain output expression for negative tree as

$$f(x1,x2,x3)=1 \oplus x_2' x_3' \oplus x_1' x_3' \quad (5)$$

Determination of the PSDRM expression from the PSDRM tree is similar to that shown above. However, in this case, the expansion for each variable is separately considered by traversing the path from the root to a leaf with coefficient one. The resulting PSDRM expression from the tree of Figure.5 is

$$f(x_1,x_2,x_3)= x_3 \oplus x_2'x_3 \oplus x_1x_3'. \quad (6)$$

The PSDRM expression of equation (4) and (5) can be realized using reversible gates. We determine PSDRM expressions for the next states from the constructed PSDRM trees. At the right descendants of the root, apply either pD or nD expansion that produces the minimum number of ones at the next level of the tree. Break the tie by choosing pD expansion. And thus we obtain the PSDRM expression. This similar approach is also adopted for the synthesis of Reversible RAM which is described in detail in the next section.

4. Design of RAM

In this section we discuss about the design of Reversible RAM(RRAM). The implementation of Reversible RAM is done using reversible gates such as Feynman gate, Fredkin gate and toffoli gate etc [12]. Other components included in the design consist of D flip-flop, 8x1 Multiplexer and 2^n xn decoder. Here we deal with the design of components used in RRAM design. The components include a memory cell, multiplexer, decoder and two important gates associated with them which is the Double Feynmann Gate and Newfault tolerant gate.

First we discuss with the design of a 2^mx m Multiplexer where m denote the number of select pins. Here m is 3, thus we design a 8x1 multiplexer as shown in Figure.6 Since only FRG is used to design a 2n×1 MUX, the represented design is characterized with parity preserving feature too. But it has no significance here. The MUX has 2m inputs and m selectors. Inputs are defined by I_0... I_N-1 and selectors are defined by S_0…..S_m-1.

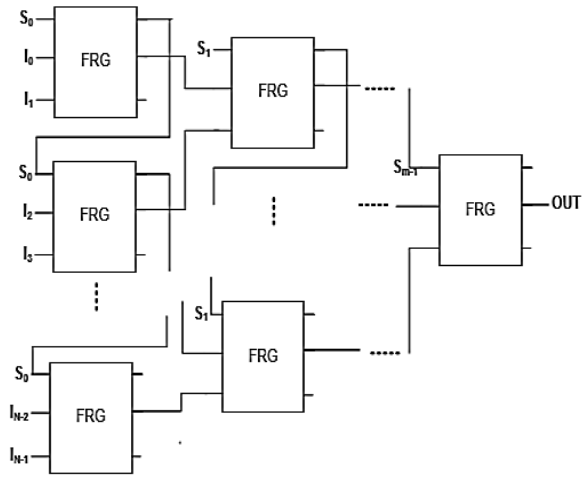

Figure 6: Proposed Multiplexer , Here N=8.

A single Double Feynman gate is shown in Figure.7. It can be used to design the basic 1 to 2^1 decoder. Using this decoder we can systematically add 2^n-1 number of Fredkin gates to the design to achieve n to 2n decoder. Here n denotes the number of gates. F2G represent the Double Feynman Gate. The design of decoder has 1 quantum cost, 1 delay and no garbage output. Our proposed decoder is shown in Figure.8. The decoder has 7 reversible gates and 7 garbage outputs for the case of a 3×8 decoder.

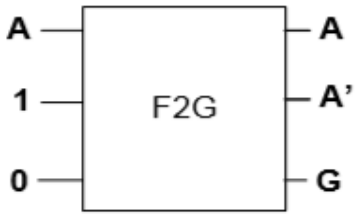

Figure 7: Proposed 1 to 2^1 decoder.

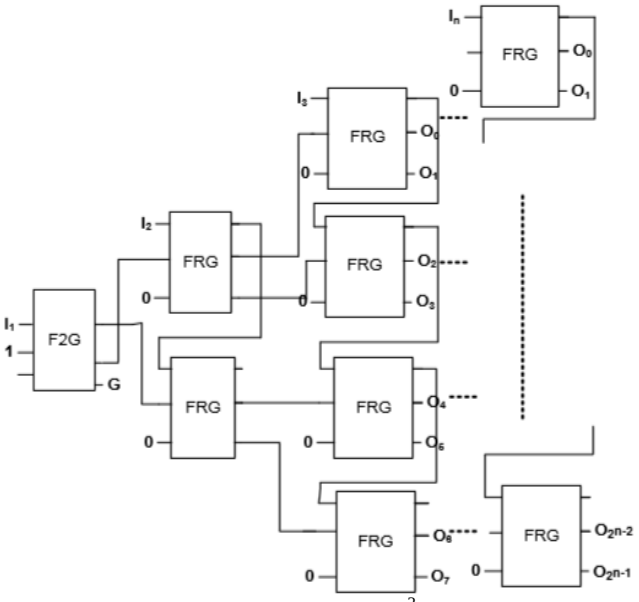

Figure 8:. Proposed 3 to 2^3 decoder.

The general design of reversible memory cell is illustrate in Figure.9. As is shown in this figure, the memory cell contains three input line and three output lines [12]. Three input lines include data D, as input of memory cell, clk as a clock, and W, the writing control line. It can be realized using D flip-flop. The realization of D flip-flop is shown in Figure.10. Any one of the realization can be used for the design of Reversible RAM (RRAM).

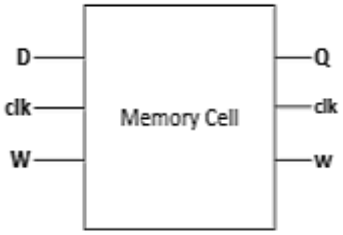

Figure 9: The general design of proposed reversible memory cell.

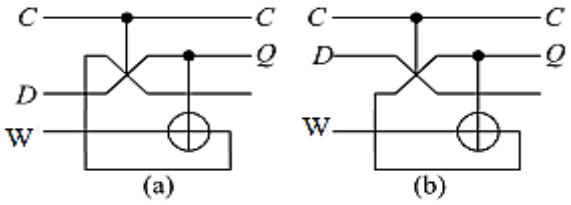

Figure 10: Reversible realization of (a) level-triggered and (b) falling-edge triggered D flip-flops

Finally the proposed design of 2n *m bit RRAM is shown in Figure.11. A RAM consists of two dimensional arrays of flip-flops. There are about 2^n rows in which each row contains about m flip-flops. Each time only one among the 2^n output lines of the decoder is active which selects one row of flip-flops of the RAM. Whether a read or a write operation is performed depends on the W input. When W is high, m flip-flops of the selected row of the RAM are written with the inputs D_1 to D_m. When W is low, Q_1 to Q_m contains stored bits in the flip-flops of the selected row and simultaneously the flip-flops are refreshed with the stored bits. In this paper we consider the designing of 4x4 Reversible RAM.

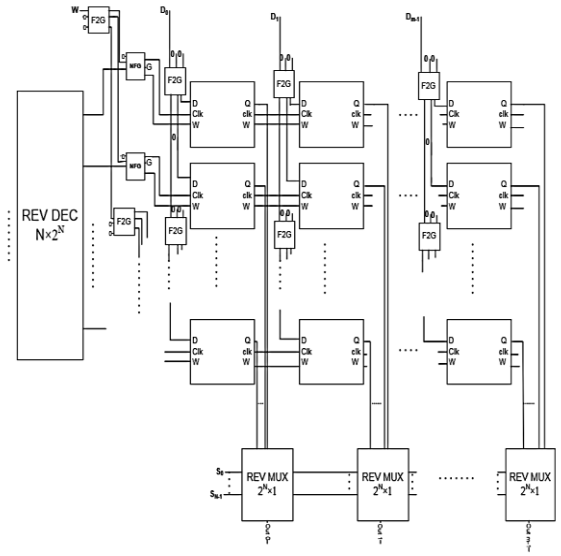

Figure 11: Design of Reversible RAM.

5. Results and Discussions

Simulation of the designed circuit has been carried using Modelsim 6.3f and the power report is obtained using Xilinx ISE 8.1i simulator. The simulation results given below are for 4X4 reversible RAM. We are using either VHDL or Verilog codes; hence the simulation can also be viewed using Xilinx. The HTML power report is shown in Figure.12. From the report we observe the fact that reversible RAM dissipate 112mW of power.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		112
Vccint 1.80V:	59	106
Vcco33 3.30V:	2	7
Inputs:	7	13
Logic:	32	58
Outputs:		
Vcco33	0	0
Signals:	4	8
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Figure 12: HTML power report of reversible RAM

The comparison of Reversible and a non-reversible RAM is shown in the tables given below.The first table gives the comparison of various cost metrics involved in the designing of the circuit. Various cost metrics are used for comparison. Factors like power dissipation, number of gates, quantum cost, garbage output etc. are considered. It can be seen from the table that power consumption is reduced in Reversible RAM. Generally by observing the table we see that all the cost metrics are improved in Reversible RAM. Hence the cost incurred during the design of circuits can also be reduced if the factors such as garbage output, quantum cost, number of gates etc. are reduced. Now let us view in detail about the various cost metrics.

Table 1: Comparison of conventional RAM with that of Reversible RAM

Cost metrics	Conventional RAM	Reversible RAM
Power consumption	432mW	112mW
Gate counts	863	696
Garbage output	248	120
Quantum cost	3547	1243
Peak memory usage	186MB	135MB
Delay	15.93ns	13.2ns

In conventional RAM the amount of power dissipation is about 432mW whereas for reversible circuits the power consumption is reduced by 320mW i.e 112mW. The next metric that is taken into account is the Gate counts. From the table it can be clearly seen that there is a great reduction in the gate counts. The reversible logic uses very less number of gates and is only about 696. Factors like garbage output and quantum cost is also reduced to 120 and 1243 respectively.The peak memory usage of conventional RAM is about 186MB, whereas in the proposed design it is reduced to 135MB. Other cost metrics which is the Delay of input-output block is also reduced from 15.93ns to 13.2ns in RRAM. The second table provides a comparison of direct design technique that we use here with that of replacement technique [9]. From the table we can clearly say that direct design technique that we have adopted has great improvements. There is 53.64% reduction in the garbage output. Similarly the quantum cost also decreases by 64.96%.

Table 2: Comparison of direct design with the design technique adopted in [9]

	Direct design	Replacement design	% Improvement
Garbage output	120	248	51.61
Quantum cost	1243	3547	64.96

6. Conclusion

Reversible logic is very much reliable for low power circuits. Reversible gates are used to implement Reversible circuits. Commonly used reversible gates include Fredkin gate, Feynman gate, Toffoli gate etc. Although there is large number of research which is carried over combinational reversible gates, the designing of sequential circuits are still at its primary stage. In this paper we discuss about the designing of reversible sequential circuits. The synthesis method that we adopt is PSDRM expression. And by this method we design a Reversible RAM (RRAM) that is efficient in terms of power consumption, garbage output, gate counts etc. All the cost metrics are improved in RRAM. Thus we can say that Reversible RAM is more efficient than the conventional RAM. Reversible RAM finds application in fields like low power CMOS, Quantum computing. In future we can also implement other reversible sequential circuits such as LFSR, counters, ALU etc. Hence RRAM can be considered as a trend towards Low power design.

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