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Multiple Patients ECG Monitoring Using Daubechies Wavelet Filter

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Abstract: ***A portable multi monitoring ECG system is proposed using conveyable Daubechies wavelets filter with memory based APC and OMS techniques which gives rise to the multiple patients ECG monitoring within single unit. This technique uses only odd multiples that are stored in LUT's and even multiples that are achieved by shifting operation. It significantly reduces the equivalent data-rate of the ADC output without affecting the information content of the input signal, leading to a reduction of data memory access processing complexity. This happens because the Daubechies wavelets filter doesn't use the feedback loop. Low power consumption around 69.08mW is achieved. By using this technique, best results for multiple patient ECG samples is obtained.***

Keywords: APC and OMS technique, Daubechies wavelets filter, Look Up Table (LUT).

1. Introduction

The study of electrocardiogram (ECG) signals is a growing research topic due to its role in diagnosing many cardiac diseases. The ECG signal is a "graphic record of the direction and magnitude of the electrical activity that is generated by the depolarization andre polarization of the atria and ventricles". Each full cardiac cycle is represented by an ECG signal that consists of P-QRS-T waves. Figure 1 shows a normal ECG signal highlighting its main features in terms of its primary waves and time intervals. The majority of the medically useful information in the ECG is originated from the intervals and amplitudes defined by its features (characteristic wave peaks and time durations) [5].Typical normal values for ECG Amplitudes and durations of a healthy normal person are summarized in Table 1 and Table 2 respectively. The improvement of ECG feature extraction is of great importance, particularly for the examination of long recordings. There is a significant research effort paid to the investigation of methods for extracting useful features carrying medical information from ECG signals that presented a low complexity algorithm for extracting fiducially points from ECG signals using Discrete Wavelet Transform (DWT)[7] compared to six distinct approaches for an EGC signal feature extraction. Their findings revealed that the Eigenvector method outperformed the other 5 presented schemes. Similar to this work they have devised a mechanism for detecting R peaks followed by the rest of the signal features. However their method is totally based on Wave segmentation. A number of other techniques have been proposed in for the detection of ECG features. Most of the aforementioned methods for ECG signal analysis were based on the time domain. But it is not always adequate to study all

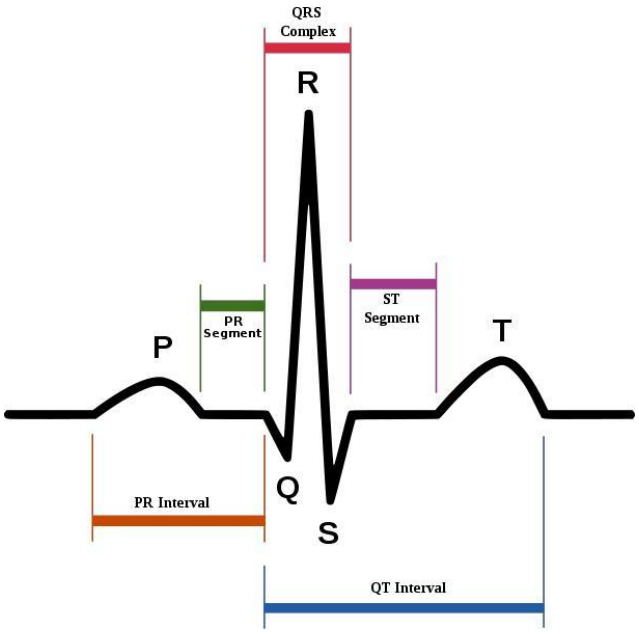

Figure 1: Typical ECG signal

the features of ECG signals in the time domain. Therefore, the frequency representation of a signal is equally important and its processing is more appealing. Current study is inspired by the ECG feature extraction algorithm [3]. Daubechies family of wavelet is used for the analysis and decomposition of the signal and the extraction of primary features of the denoised and decomposed ECG signals. By extracting these primary ECG features, it is thought that some fundamental parameters such as the amplitudes of the waves and their durations such as RR, QRS, and PR intervals can be easily obtained which is then used for subsequent automatic analysis. In [11] this Existing system the implementation of a delayed least mean square(DLMS) adaptive filter is used . For achieving lower adaptation-delay and area-delay-power efficient implementation, use a novel Partial Product Generator(PPG) is used The Fixed point LMS Adaptive filter implementation is used to reduce the number of pipeline delays along with area, sampling period and energy consumption. The design is efficient in terms of the Power Delay Product(PDP) and Energy Delay Product(EDP)This structure to minimize the adaptation delay in the error-

computation block, followed by the weight-update block The structure for error-computation unit of an *N*-tap DLMS adaptive filter.

2. Filter Architecture

The block diagram of the filter and its building blocks are shown in fig2. In addition to this various circuits have been proposed for each module to compute the DAUB4 and DAUB6 wavelet coefficients. This new scheme enables resource sharing and yields lower hardware cost and power consumption, and higher process throughput. The architecture of Daubechies4 is used to select the desired transform unit based on the application and end user's requirement. For slowly varying signals, the DAUB4 gives best results. It fits in an image compressor for applications like wireless capsule endoscopy [10].

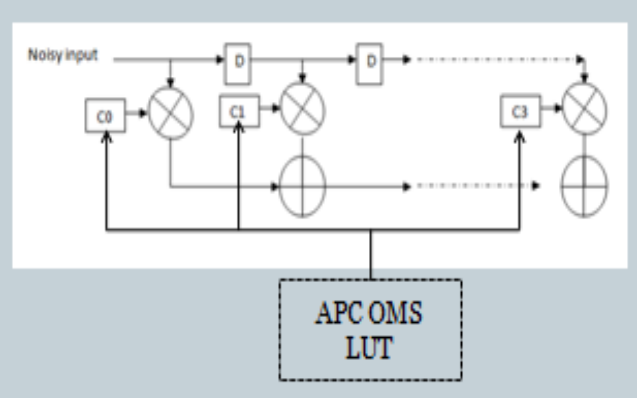

Figure 2: Filter block diagram

The input signal is applied to the filter to remove the unwanted signal and the output is sent to the comparator .The comparator compares the desired signal and the input signal and the error output is sent to the filter. The output of APC-OMS again sent to the filter and the output is realized[11].

2.1 Adder tree

In the RCA (Ripple Carry Adder) method, two inputs are added from LSB to MSB where each carry is added with the forthcoming bits. It increases propagation delay. In the parallel adder method, both sum and Carry are generated in same time cycle using XOR and AND gates. The carry zero (0) is to be stored in the Parallel Adder (PA) and the carry one (1) is to be stored in the BEC (Binary Excess Code). Multiplexer is used for multiplication operation. In this adder tree computation time is reduced. Hence the power is saved.

2.2 Shift/add tree

The shift/add tree is placed inside the filter using multiplexer. The operations of this shift/add tree includes shifting and adding of the inputs and resulting in ones and twos compliments. If the shift/add tree does not exist, number of operations will be increased which increases the complexity of the system.

3. The APC-OMS Technique and Implementation

In the APC-OMS technique, the LUT tables size is reduced to third-fourth of the conventional LUT. The APC-OMS block diagram shown in the Fig. A conventional lookup-table (LUT)-based multiplier is shown in Fig. 1, where A is a fixed coefficient, and X is an input word to be multiplied with A. Assuming X to be a positive binary number of word length L, there can be $2L$ possible values of X, and accordingly, there can be $2L$ possible values of product $C = A \cdot X$. Therefore, for memory-based multiplication, an LUT of $2L$ words, consisting of pre computed product values corresponding to all possible values of X, is conventionally used.

3.1 APC for LUT optimization

For simplicity of presentation, we assume both X and A to be positive integers.[11]The product words for different values of X for $L = 5$ are shown in Table I. It may be observed in this table that the input word X on the first column of each row is the two's complement of that on the third column of the same row. In addition, the sum of product values corresponding to these two input values on the same row is $32A$. Let the product values on the second and fourth columns of a row be u and v, respectively. The product values on the second and fourth columns of Table I therefore have a *negative mirror symmetry*. This behavior of the product words can be used to reduce the LUT size, where, instead of storing u and v, only $[(v - u)/2]$ is stored for a pair of input on a given row. Since one can write $u = [(u + v)/2 - (v - u)/2]$ and $v = [(u + v)/2 + (v - u)/2]$, for $(u + v) = 32A$, we can have

$$u = 16A - \left[\frac{v-u}{2}\right] \quad v = 16A + \left[\frac{v-u}{2}\right]. \tag{1}$$

The 4-bit LUT addresses and corresponding coded words are listed on the fifth and sixth columns of the table, respectively. Since the representation of the product is derived from the anti symmetric behavior of the products, we can name it as *antisymmetric product code*. The 4-bit address $X\_ = (x\_3x\_2x\_1x\_0)$ of the APC word is given by

$$X' = \begin{cases} X_L, & \text{if } x_4 = 1 \\ X'_L, & \text{if } x_4 = 0 \end{cases} \tag{2}$$

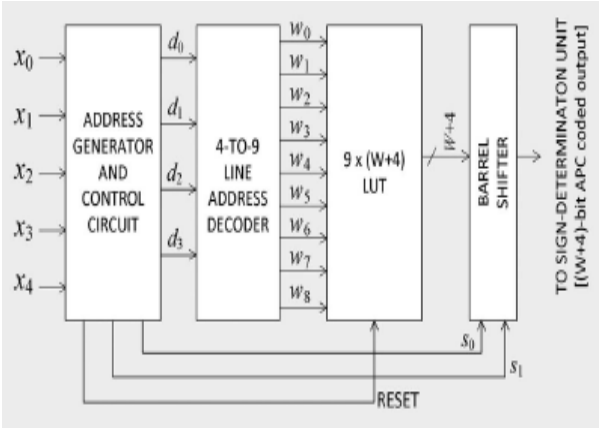

Figure 3: Proposed APC-OMS combined LUT

Product word = 16*A* + (sign value) × (APC word).where sign value = 1 for *x*4 = 1 and sign value = −1 for *x*4 = 0. The product value for *X* = (10000) corresponds to APC value "zero," which could be derived by resetting the LUT output, instead of storing that in the LUT .where *XL* = (*x*3*x*2*x*1*x*0) is the four less significant bits of *X*, and *X_L* is the two's complement of *XL*. The desired product could be obtained by adding or subtracting the stored value (*v* − *u*) to or from the fixed value 16*A* when *x*4 is 1 or 0, respectively.

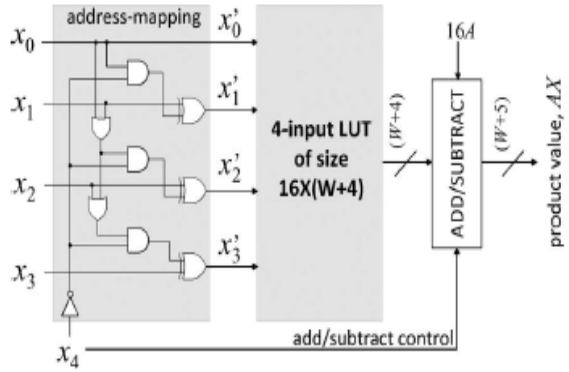

Figure 4: LUT-based multiplier for *L* = 5 using the APC technique

3.2Modified OMS for LUT optimization

The multiplication of any binary word *X* of size *L*, with a fixed coefficient *A*, instead of storing all the 2*L* possible values of *C* = *A* · *X*, only (2*L*/2) words corresponding to the odd multiples of *A* may be stored in the LUT, while all the even multiples of *A* could be derived by left-shift operations of one of those odd multiples [11].In Table II, [11]we have shown that, at eight memory locations, the eight odd multiples, *A* × (2*i* + 1) are stored as *Pi*, for *i* = 0, 1, 2, . . . , 7. The even multiples 2*A*, 4*A*, and 8*A* are derived by left-shift operations of *A*. Similarly, 6*A* and 12*A* are derived by left shifting 3*A*, while 10*A* and 14*A* are derived by left shifting 5*A* and 7*A*, respectively. A barrel shifter for producing a maximum of three left shifts could be used to derive all the even multiples of *A*. It may be seen from Tables II and I that the 5-bit input word *X* can be mapped into a 4-bit LUT address (*d*3*d*2*d*1*d*0), by a simple set of mapping relations *di* = *x*``*i*+1, for *i* = 0, 1, 2 and *d*3 = *x*0 '' where *X''*= (*x''*3*x''*2*x''*1*x''*0) is generated by shifting- out all the leading zeros of *X*_ by an arithmetic right shift followed by address mapping.

$$X'' = \begin{cases} Y_L, & \text{if } x_4 = 1 \\ Y'_L, & \text{if } x_4 = 0 \end{cases} \quad (3)$$

where*YL* and *Y _L* are derived by circularly shifting-out all the leading zeros of *XL* and *X_L*, respectively

4. Measurement and Comparison Results

4.1 Measured output

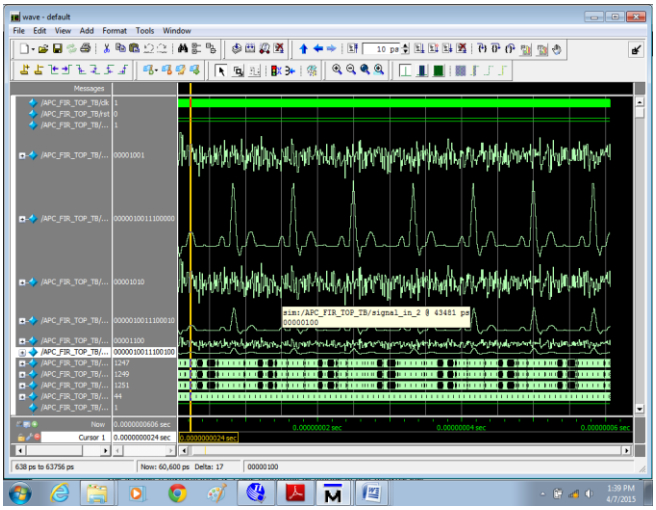

Figure 5: Simulation Result

4.2 Simulation of ECG Wave Form

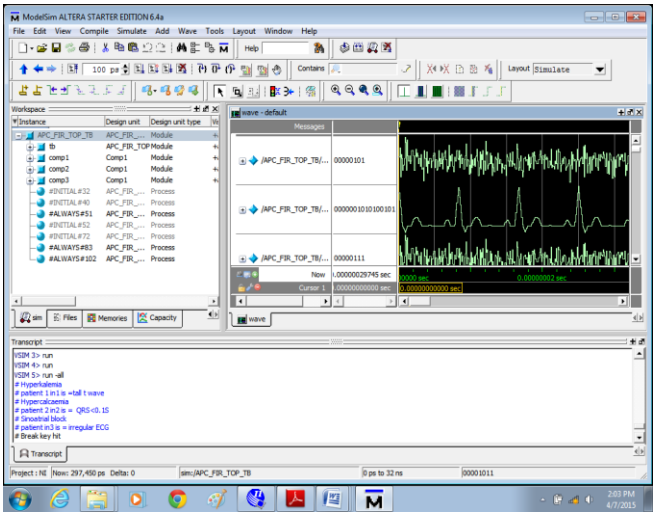

Figure 6: Simulation result of disease

Fig 6. shows the simulation result of disease. It identifies the disease called Hyperkalemia, hypercalcaemia and sinosatrial block based on the signal wavelength within nanoseconds.

4.3 Simulated output of APC and OMC

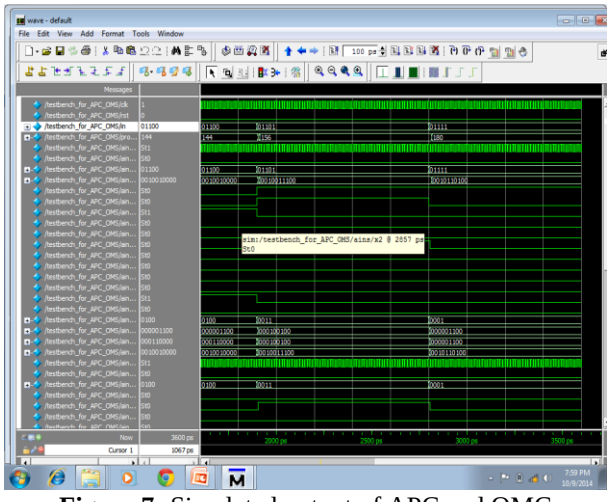

Figure 7: Simulated output of APC and OMC

Fig 4.3 shows the simulated output of APC and OMS in which the barrel shifter control values S_0, S_1, address generation (d_0, d_1, d_2, d_3), APC word output and process of OMS values and final output are described.

4.4 Comparison table

Table 1 shows the comparison between of Area and Power Adaptive Filter and Daubechies wavelets filter .The proposed Daubechies wavelets filter based on APC and modified OMS multiplier are compared with FIR filter in terms of total area used by the logic elements, static power and dynamic power shows from simulated output

Table 1: Comparison of area and power for Adaptive filter and Daubechies wavelets filter

FILTER DESIGN	AREA	TOTAL POWER	DYNAMIC POWER	STATIC POWER	I/O THERMAL POWER DISSIPATION
ADAPTIVE FILTER	736 LEs	107.95mW	40.48mW	46.24mW	21.22mW
DAUBECHIES FILTER	561LEs	69.08mW	3.77mW	46.14mW	19.17mW

5. Conclusion

The combination of the APC(Anti symmetric product code),and OMS(Odd Multiple Storage), provides reduction in LUT to one fourth of its size in a Daubechies wavelets filter when compared with the Adaptive filter. The obtained results from the proposed architecture shows much reduction in computation time and area used.

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