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Design and Analysis of Asynchronous 16*16 Adiabatic Vedic Multiplier Using ECRL and EEAL Logic

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Abstract: ***In this paper, we describe adiabatic Vedic multiplier using efficient charge recovery logic (ECRL) and energy efficient adiabatic logic (EEAL). In today's world low power hindrance have become a major important factor in modern VLSI design. Because of the increasingly draconian demands for battery space and weight in portable multimedia devices, energy productive and high yielding circuits are required, particularly in digital multipliers which are basic building blocks of digital signal processors. For speed and power criteria the Urdhva-Tiryagbhayam Vedic multiplier is effective and adiabatic logic style is said to be an attractive solution for low power electronic applications. With adiabatic logic most of the energy is restored to the source instead of dissipating as heat. Proposed work focuses on the design of low power and area-efficient adiabatic Vedic multiplier using TSMC0.18µm CMOS process technology in HSPICE G2012.06.***

Keywords: Adiabatic logic, Vedic Multipliers, ECRL logic, EEAL logic, Performance Comparison.

1. Introduction

Providing new low power solutions for Very Large Scale Integration (VLSI) designers is the main objective of this paper. At different levels to reduce the power dissipation of the circuit various techniques of the design process have been implemented, at system level and architectural level. In computations multipliers play a vital role which makes them one of the key components of every ALU. Than addition and subtraction, multiplication requires substantially more hardware resources and processing time. In the design of large computers and personal information systems the dynamic power requirement of CMOS circuits is rapidly becoming a major concern.

In this paper, based on adiabatic switching principle a new CMOS logic family called *ADIABATIC LOGIC* is presented. It substantially reduces the power dissipation. Adiabatic logic offers a way to utilize the energy stored in the load capacitors rather than the traditional way of discharging the load capacitors to the ground and shrink this energy. As the need of high speed processors are increasing the need of high speed multipliers are also increasing. In many real time signal and image processing applications to achieve the desired performance, higher throughput arithmetic operations are important.

2. Literature Survey

Vedic mathematics was rediscovered from the ancient Indian scriptures by Jagadguru Swami Sri Bharati Krisna Tirthaji (1884-1960), [3] a scholar of Sanskrit, history, mathematics and philosophy, between 1911 and 1918. Vedic mathematics is based on 16 Vedic principles; it is based on solving the whole range of mathematical problem by natural ways. Here, we use Urdhva Tiryagbhayam principle to reduce the partial products which we obtain during normal multiplication technique. The term 'adiabatic' describe the thermodynamic processes where there is no energy exchange with the environment, and dissipated energy loss is negligible. A part of the signal energy is covered by adiabatically charged logic and if the circuits are slowed down, approaching nearly so that all of the energy can be recovered. In designing low power consuming devices, CMOS technology plays a dominant role from the past few decades. CMOS has less power dissipation so it has become superior when compared to all other previous lower power techniques of different logic families [9]. The less the power dissipation, the more efficient the circuit will be [8]. The cost of approaching adiabatic logic is usually high in complexity, circuit area, or timing. Either timing-based logical reversibility or reversible logic gates is required.

In traditional digital integrated circuits to overcome the power challenge, reversible logic is used. It potentially benefits from the reversible computation principles associated with energy recovery. The signal energy is not recovered by the Standard Complementary Metal Oxide Semiconductor (CMOS), which leads to significant heat dissipation and energy waste, limiting the accessible device densities, and thereby, also the operating frequencies and available computing power. As reported in [1], to get the area and power requirements of the computational complexities in the VLSI circuits, the width and length of transistors are shrunk into the deep submicron region.

3. Adiabatic logic

In the design of many digital circuits CMOS is the basic element. By the combination of both PMOS and NMOS devices it can be formed. Where the PMOS source is connected to V_{dd} and NMOS source is connected to ground and the output is taken across the drain combination of both PMOS and NMOS devices. Figure 1 shows the basic CMOS inverter. Power dissipation in conventional CMOS circuits primarily occurs during device switching. Both PMOS and NMOS transistors can be modeled by including an ideal

switch in series with resistor in order to represent the effective channel resistance of the switch and the interconnect resistance.

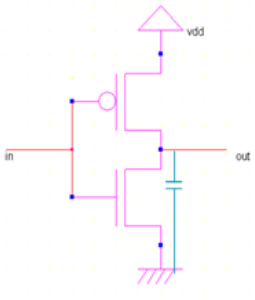

Figure 1: CMOS inverter

The power dissipation in conventional CMOS design can be decreased by reducing the values of certain parameters, but they suffer from certain disadvantages. Reducing the supply voltage may also suffer from leakage problems. Adiabatic logic gate operation is divided into two different stages: one stage is used for logic evaluation; reset gate output logic value is the other stage. Adiabatic switching principle is used in both the stages. This logic is commonly used to minimize energy loss during charging/ discharging. Previously diodes are utilized for pre-changing output nodes in adiabatic circuits [5]-[7]. It has less power dissipation compared to the conventional CMOS design. It uses AC power supply. It has less switching time. By using some of its techniques, both the true function and complimentary function can be realized in a single circuit, thereby reducing the area to some extent.

3.1 Transistor Based Adiabatic Logics

The term adiabatic logic is referred as reversible logic in many VLSI circuit designs. Adiabatic logic is shown in the below figure 2.In this, Power clock plays the vital role in the principle of operation. Main design changes are focused on it.

The following three rules are used for energy conservation in adiabatic circuits:

1) When there is a voltage potential between the source & drain never turn on the transistor (Vds>0).
2) When current is flowing through a transistor never turn it off (Ids-0).
3) Never pass current through a diode.

With regard to the inputs when the 3 conditions are satisfied, in all the 4 phases of power clock, in power clock recovery phase will restore the energy, resulting considerable energy saving. Thus without loss or gain of electric charge, the adiabatic logic circuits operate. However, by slowing down the speed of operation one can achieve very low energy dissipation and only switching transistors under certain conditions [4].

Here, by using a constant-current source (instead of using the constant-voltage source as in the conventional CMOS circuits) the load capacitance is charged. Here, R is the resistance of the PMOS network. A linear voltage ramp is indicated for constant charging current. Assume, the capacitor voltage VC is zero initially.

The voltage across the switch = IR
Switch P (t) = RI2 – (1)
Energy during charge = T (I2R) -(2)
E.E= T (I2R) = RT (CV/T) 2 =C2V2/T R – (3)
E = Edis = (RC/T) CV2 = (2RC/T) (1/2CV2)

Where, in Equation (3) the various terms are described as follows:
E — amount of energy dissipated during charging,
Q — charge being transferred to the load,
C — load capacitance value,
R — when MOS switch is turned on its resistance,
V — voltage final value at the load,
T- Time.

Now, based on Equation (3) a number of observations can be made as follows:

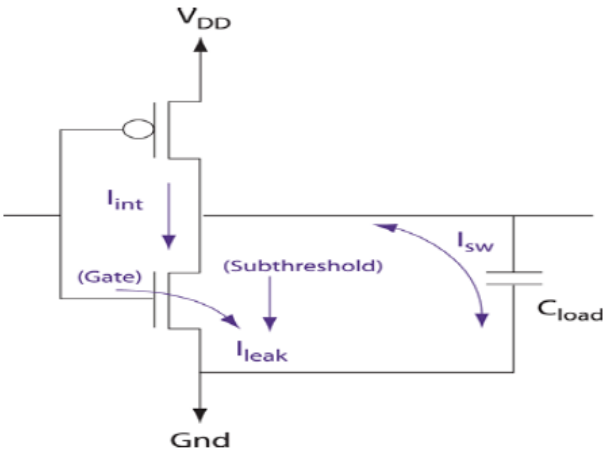

Figure 2: Adiabatic logic

4. Vedic Multiplication

The term ‘Vedic’ is derived from the word ‘Veda’, which means store house of all knowledge. Even to the problem involving trigonometric functions, applied mathematics conics, Plane and sphere geometry, differential calculus and integral calculus different kinds of Vedic mathematics logics and steps can be applied. This has accredited to fact that the Vedic formulae have declared to be building on natural rules on which human mind operates. Thus, this shows some methodical algorithms, which can apply to various branches of applied science.

4.1 Urdhva-Tiryagbhayam Principle

In the proposed method, Urdhva Tiryagbhayam principle is used. In the decimal number system, this principle has been used for multiplication of two numbers. It is nothing but the principle is related to vertical and crosswise. This formula is postulated for n x n bit numbers. The method for Urdhva Tiryagbhayam for 2-bit binary number is shown in figure 3.

When two 2 bits A and B is taken the multiplication method is explained below wherever A = a1a0 and B =b1b0 as shown in figure. The Vedic Multiplication technique for two 2-bit Binary numbers is shown below.

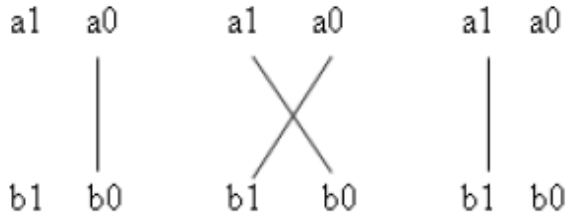

Figure 3: Vedic multiplication of 2-bit binary number.

1. First LSB bits of the right-hand digits are multiplied.
2. Secondly the second bit LSB of the base number is multiplied with the LSB of the top number and count them together.
3. Multiply the MSB digit of the top number by the LSB digit of the base number by, then the MSB digit of the base one with the LSB digit of the top number and multiply the bit after that count all together.
4. Move one place to left, multiply the MSB of one number with second digit of other number.
5. Finally to get the result, multiply the LSB of both the numbers together.

An example of two 3digit decimal numbers which is multiplied by using Urdhva Tiryagbhayam is shown in the below figure 4.

By using this 2*2 multiplier block 4*4,8*8,16*16 etc multiplier blocks can be implemented. In N*N multiplication we need four N/2*N/2 multipliers, two N bit Adders, a half adder and an N/2 bit adder.

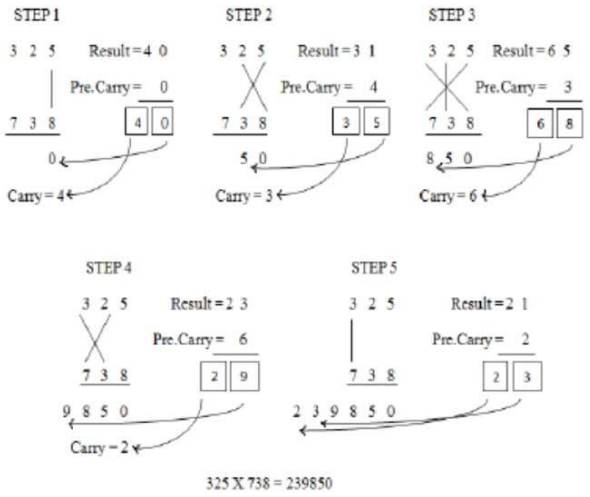

Figure 4: Multiplication of two decimal numbers 325*738

6. Energy Efficient Adiabatic Logic

The energy saving benefits of adiabatic logic and asynchronous logic is combined in the unique design technique called Energy efficient adiabatic logic. The gates are designed based on the basic structures of adiabatic ECRL [2] logic. Asynchronous circuits are also a favorable technology to focus on low power like adiabatic circuits. As circuits include a built-in insensitivity to fluctuations in power supply, with a lower voltage arise in slower operations lightly than the functional failures that would be seen if conventional synchronous systems they are used as one of the properties of asynchronous systems which make them useful in many applications. Another benefit is that when a conventional asynchronous system is idle, the clock signals are not utilized, whereas in synchronous systems, without performing any useful computations these clock signals are propagated throughout the entire system and convert energy to heat. In this paper alternative solutions to limit power dissipations are proposed [10].

Asynchronous circuits perform compact between their components to perform all necessary harmonize, sequencing of operations and communication in diversity to the synchronous circuits. Asynchronous circuits come into different classes, each contributing different assets. The main privilege of this circuit is its low power utilization, emanate from its destruction of clock drivers.

7. Efficient Charge Recovery Logic

Efficient Charge Recovery Logic (ECRL) uses cross-coupled PMOS transistors which is shown in figure 5. It‘s the architecture kind of like Cascode Voltage Switch Logic (CVSL) with differential sign. An AC power furnish PWR is employed for ECRL gates, therefore on recuperate and reprocess the equipped energy. Full output swing is attained as a result of the cross-coupled PMOS transistors in each pre-charge and get back phases. The circuits suffer from the non-adiabatic loss each within the pre-charge and recover phases, however attributable to the brink voltage of the PMOS transistors. That is, to say, ECRL continuously pumps charge on the output with a full swing. However, the PMOS electronic transistor gets turned off when the voltage on the equipped clock approaches to Vtp,

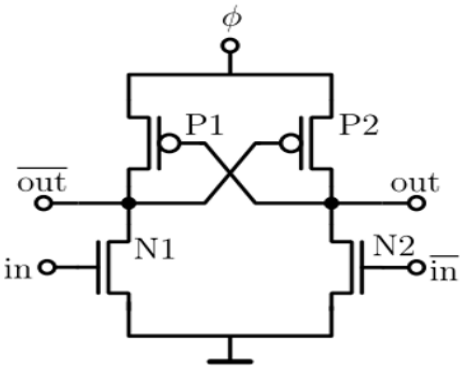

Figure 5: The basic structure of Adiabatic ECRL logic

So the reconstructive path to the equipped clock is disconnected, thus, leading to incomplete recovery. Vtp is that the threshold voltage of PMOS semiconductor device. The number of loss is given as

EECRL = C|Vtp|2 / a pair of -- (1)

It may be implied that the non-adiabatic energy loss build up on the load capacitance and freelance of the frequency of operation. The ECRL circuit‘s area unit regulate during a pipelining vogue with the four-phase provides clocks. Once the output is directly connected to the input of following, just one part is enough for a logic price to propagate. The input signals propagate to ensuing stage during a single part, and also the input values area unit holds on in four phases (1-

clock) safely. At the start of a cycle, once the provision clock power rises from zero to Vdd, out remains at a ground level, as a result of in activates F- tree (NMOS logic tree). The outputs hold valid logic levels when power reaches Vdd. A major detriment of this circuit is that the presence of the coupling effects, as a result of two outputs area unit connected by the PMOS latch and also the two complementary outputs will inhibit one another.

8. Experimental Results

The schematic diagrams of ECRL NAND-AND gate Figure 6, ECRL NOR-OR gate Figure 7, EEAL NAND-AND gate Figure 8 and EEAL NOR-OR gate Figure 9 is shown below. The output waveforms for adiabatic logic Vedic multiplier ECRL and EEAL are given in below figures 10 and 11. Then the comparison table for the average power, average delay and power delay product is given in Table 1

In the below schematic diagrams, it explains the operation of specific gates. When the inputs 00,01,10,11 are given its corresponding outputs are shown accordingly.

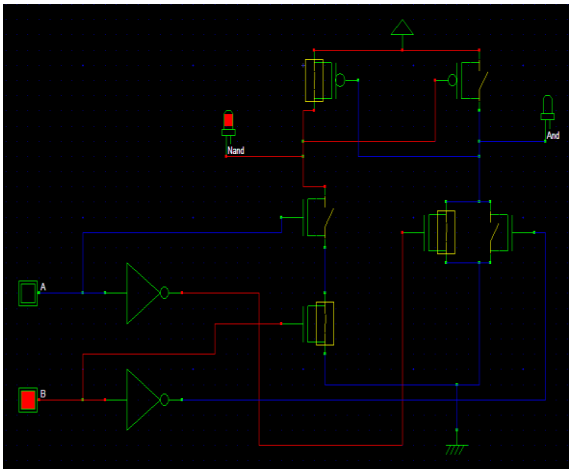

Figure 6: ECRL NAND-AND gate

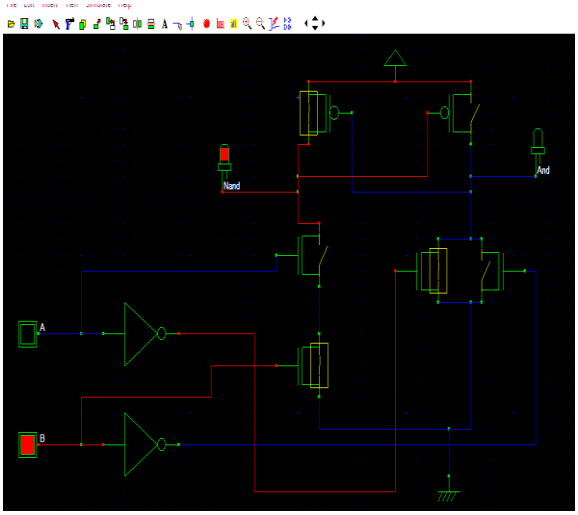

Figure 7: ECRL NOR-OR gate

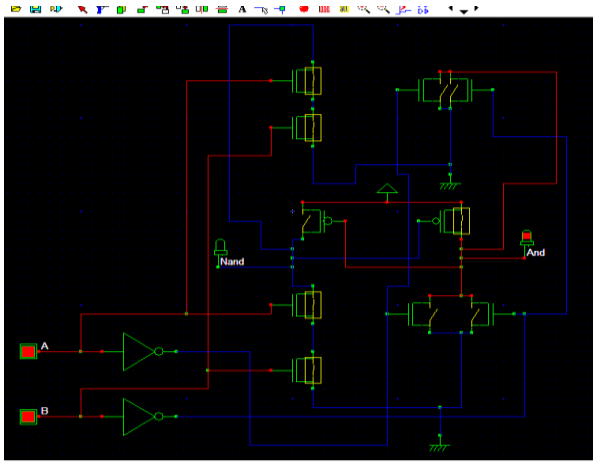

Figure 8: EEAL NAND-AND gate

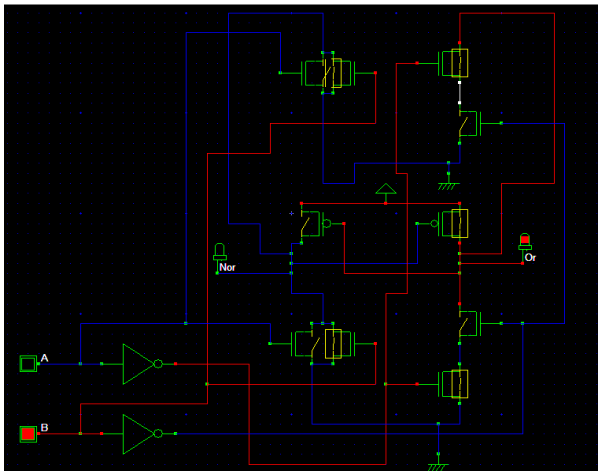

Figure 9 : EEAL NOR-OR gate

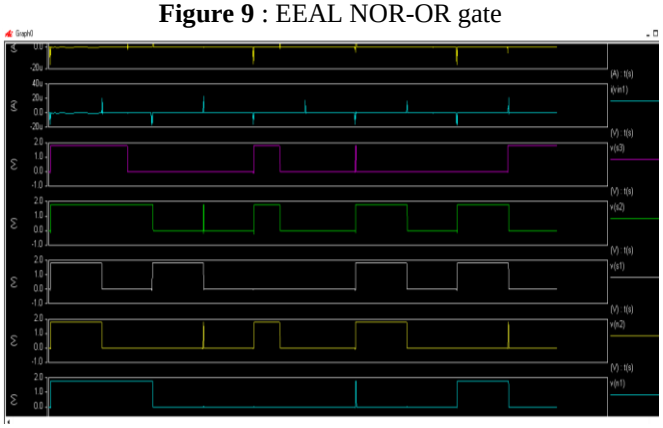

Figure 10: Simulation waveform of ECRL

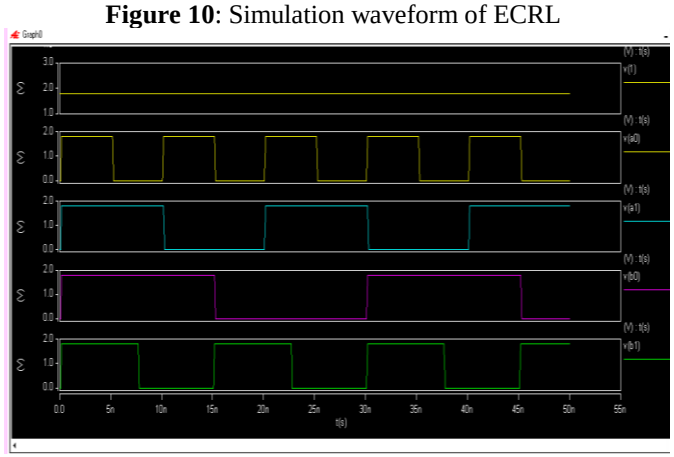

Figure 11: Simulation waveform of EEAL

9. Performance Comparison

The below table 1 clearly shows that the power is reduced while using Efficient Charge Recovery Adiabatic Logic and Energy Efficient Adiabatic logic than by using static logic.

Table1: Comparison of performance of ECRL and EEAL logics.

Multiplier	*Parameter*	*Static*	*ECRL*	*EEAL*
2*2	Average power	6.046u	4.469u	4.330u
	Average delay	29.23p	32.33p	18.03p
	Power delay product	176.7a	144.5a	78.08a
4*4	Average power	17.64u	30.23u	29.33u
	Average delay	2.46n	2.47n	2.46n
	Power delay product	43.44f	74.80f	72.22f
16*16	Average power	452.3u	409.3u	379.8u
	Average delay	3.52n	2.47n	2.461n
	Power delay product	1.582p	2.46n	935.06f

10. Conclusion

This paper primarily was targeted on the construction of low power CMOS cells structures, and proposed by using energy efficient adiabatic logic technique and efficient charge recovery logic using Vedic multiplier. The multipliers circuit are created and related with conventional CMOS multiplier that is using static logic. The power results are analyzed. Thus adiabatic logic consumes less power when compared with conventional CMOS. All the parameters are computed on Hspice at 180 nm Technology at 1.5V supply voltage. Adiabatic logic attains low power by maintaining small potential differences beyond the transistors while they are conducting, and allowing the charge stored in the output load capacitors to be recycled. The circuit becomes low power faster but hardware complexity is also high, which can be overcome by using very large scale integration fabrication techniques. With the adiabatic switching approach the power dissipation can be reduced up to 78% to 90% of the digital system.

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