Review of Different Types of Over-Current Protection Circuits used in Various Applications

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Abstract: This review paper inherits few different types of over-current protection circuits which are used in various applications differently. The over current protection circuits are generally used for protecting the device from large current which is not good for our device. This protects our device as well as by using some techniques we can lower the circuit's power dissipation, and enhance the reliability of the system.

Keywords: Over current protection ,Power amplifier, Power consumption, Pre comparison, Current limit.

1. Introduction

Different type of approaches are used to protect the circuits from over current. In recent years, more and more digital power amplifiers are used in all kinds of portable applications. Digital power amplifier achieves the higher power efficiency by using pulse width modulation (PWM), in theory, it can get a theoretical efficiency of 100% and practical efficiency of 80% or even more [1], which increases the overall systems battery lifetime and reduces the heat dissipation.

Current limit is also one of the most desirable features for many smart discrete power devices such as smart power MOSFETs and IGBTs. The current limit function usually provides protection for smart power devices against inadvertent load shorts[2,3]. Additionally, the design of low power dissipation in power devices becomes more and more important[4].

2. Traditional over-current protection circuit for USB



Figure 1: Traditional over current protection circuit

Figure.1 is Traditional over current protection circuit which were used in earlier[5,6].Mp is power MOSFET, M1 is sampling tube.The current flowing through R0 is the current of load.

$$\mathbf{V}_{\mathrm{GS1}} = -\mathbf{R}_0 \mathbf{I}_{\mathrm{OUT}} \tag{1}$$

When the current of load is normal, M1 is in cutoff region.

The gate voltage of MP is the output of driving circuits. When the current of load exceeds the threshold, M1 is in saturation region. The gate voltage of MP is high to limit load current on a specific value.

The shortcoming of this circuit is: first, the dropout voltage of R0 reduces conversion efficiency especially in the high load; secondly, this circuit has still large power consumption due to the current of MP limiting on a specific value.



Figure 2: CMOS over current protection circuit

Fig.2 is another common over-current protection circuit [7]. MP is power MOSFET, M2 is sample tube. Sampling tube M2 proportional samples the load current. The voltage of point A is:

$$\mathbf{V}_{\mathrm{A}} = \mathbf{R}_{0}\mathbf{I}_{2} + \mathbf{V}_{\mathrm{EB}} \tag{2}$$

When the current of load is normal, the output of comparator is high level. M1 is in cutoff region. The gate voltage of MP is the output of driving circuits. When the load current is to the threshold voltage, the output of comparator is low level, M1 is on. The gate voltage of MP is high to limit load current on a specific value.

In this circuit, sampling resistor and power MOSFET is not in series, so this circuit improves the conversion efficiency greatly [5]. But this circuit still has some shortcomings: firstly, the gate source voltage of MP and M2 is same, the drain voltage of MP and M2 is different and this reduces the reliability for sampling current inaccuracy; secondly, this circuit has still large power consumption due to the current of MP limiting on a specific value.



Figure 3: High reliable over current protection circuit with low power consumption

Fig.3 shows a kind of over current protection circuit to solve the issue of reliability and large cutoff current, a high reliability over-current circuit with low power consumption. Over-current circuits are defined that it can protect system and load once over-current and overload. The current sampling method is to connect sample resistance and power devices in series which make severely consumption especially in the circuit of low voltage with large current. The circuit[8] of the paper can efficiently avoid these issues.

M2 is power switch, M1 and M3 proportional sample on the current of M2. When the system is working normally, the pre- comparing circuits AMP_1 works and output high level to open M7, then the gate voltage of M8, M9 is low level. The positive feedback comparator made of M4, M5, M8, M9, M6 is shut off which has large power consumption. The inn voltage of AMP 2 is lower than the inp voltage, the level of ocp_out is high. The system works normally. Once the load current exceeds the limit or the systems is short current, the output of the AMP_1 is low level, the next stage begin to work. Positive feedback system forces the source voltage of M4 to follow the source voltage of M5,M6. The output voltage decreases quickly, the V_{GS} voltage of M4 changes heavily than M5. The current source of I1 can help the positive feedback system start faster and absorb some current. A diode connected NMOS is active resistance, like M10 and M11 connecting in series. The inn voltage is equal to multiply by sample current and divide resistor.

In this circuit due to the property of pre comparision and proper shut down of some portion of circuit power consumption is low this makes circuit very reliable but it is complex.

The over-current protection circuits in this section has high reliability and low power consumption. The circuits proportionally sample current of load and will not cause extra dropout between IN pin and OUT pin. It has low power consumption because the stage having high power consumption is shut off by the pre-comparing circuit. It has low power consumption because of the pre-comparing circuits. Once over-current, the circuits output alarm signal to shut off power MOSFET. The function of delay start turns on switch tube 5 us later. This can prevent the damage from the frequent switch and has long life.

3. CMOS current limit circuit for smart discrete power devices

Fig.4 illustrates a circuit diagram of the CMOS current limit circuit. M1 is the power pass device and M3 is the sense MOSFET. The current mirror M4 and M5 make the sense current more precise. The voltage across the sense resistor R_s is input to the negative input terminal of a comparator to compare with a reference voltage. M6 and M7 serve as a bias current source.

When the voltage across the sense resistor R_s is below thereference voltage, the pull-up MOSFET M2 stays off. Therefore, the power MOSFET operates in its normal operating mode. With the increasing MOSFET current, the voltage across R_s arises and eventually turns on the pull-up MOSFET M2 as soon as the voltage is above the reference voltage. Therefore, the gate voltage of M1 is enhanced and the current of M1 is effectively limited.



Figure 4: CMOS current limit circuit

However, the current conducted by the power device in Fig.4 is still large since the current limit circuit has been working. Subsequently, the power dissipation lost in the circuit is large. So this circuit will not fit to large power circuits. In terms of power dissipation, the circuit of Fig.4 is improved and a foldback current limiting scheme is implemented[10], as illustrated in Fig.5. The idea is to make the maximum allowed output current, during overload conditions, a function of the output voltage. Consequently, the maximum current permitted is reduced as the output voltage is decreased[9].



Figure 5: Low power high reliable CMOS current limit circuit

In Fig.5, M9 has the same function with M3. In order to obtain the precise sampling current, the drain voltage of M9 must be approximately equal to the drain voltage of M1. So we made the width-length ratio of M10 large enough to reduce the gate-source voltage of M10. The resulting relationship can be expressed as

$$I_{M9} = \left(\frac{W_{M9}/L_{M9}}{W_{M1}/L_{M1}}\right) I_{o}$$

In normal operating condition, V_{G12} <Uo+V_{TH12}.Therefore, M12 stays off and conducts no current. M8 is off too and the foldback circuit is out of work. Once the output is shorted to ground or the output current exceeds the maximum allowed value, the circuit in Fig.4 starts to work and reduces the output voltage Uo. Uo will continue to decrease, which eventually forces M12 to conducting current. When $V_{SG8} =$ I_{M12}R₃> Vth8 with increasing of the current of M12, M8 turns on and the gate voltage of M8 is reduced. Additionally, the turn on of M8 will largen the gate voltage of M1 and subsequently force the output current to decrease. If the value of (W /L)_{M11} and resistor R4 are set properly, reduces in Io will cause V_{GS12} to increase further. Therefore, VG8 continues to decrease and the gate voltage of M1 keeps increasing. Thus, Io will be forced to decrease further until it is limited at a certain level.

4. Novel over-current protection circuit for digital power amplifier

Translation efficiency of digital power amplifier is higher, but the risk of the chip over-current due to short circuit in the load should be considered similarly, otherwise, the four output MOS buffers in the chip may be damaged. In order to limit the excessive power dissipation in the load when short circuit occurs and protect four output buffers, an over current protection circuit should be designed. Usually, there are three kinds of short circuit to be considered: the first is short circuit between two ends of load, the second is short circuit between one end of load and power ground, the last is short circuit between one end of load and power supply. Different from reference [11], in this paper[12], the current in the four output MOS transistors are real-time controlled, and if one current exceeds the threshold set to 3A, the MOS transistor would shut down and the current is reduced to zero. Since it completely turns off the output buffer, it minimizes the risk of over current.

The paper[12] presents a over current protection circuit for 2.75W digital power amplifier, it can effectively protect the chip when above-mentioned short circuit occur.

4.1 Output stage of Digital power amplifier

Figure-6 shows the schematic of output stage circuit which is composed of deglitch circuits, driver stages and H-bridge output buffers. Deglitch circuit is used to get rid of narrow pulse in PWM. Driver stage is designed to drive H-bridge output buffers, which include P_1 , P_2 , N_1 and N_2 four high power MOSFETs. Two detectors are used to detect whether



Figure 6: Schematic of output stage circuit

over-current is happened through sampling voltages of gate and drain of MOSFETs in both sides of output buffer. As soon as over current occurs, the output signal "OC_F" of module would change to high level. Because output buffer adopts H-bridge architecture, there are two over-current detector circuits to sample voltages in both positive and negative output.

4.2 Novel protection circuit

It presents[12] a novel over-current detector circuit in figure 7, MOSFET "N10" and "N1" is connected as a pair of mirror current source, as soon as the current through "N1" is over current when short circuit occurs, the current through "N10" would also increase proportionately. When the current through "N1" is larger than over-current threshold, the voltage of node "B" would increase, NMOS "N17" would change from saturation region to shut-off region, voltage of drain of "N17" also increases to high logic level "1", MOSFET "N18" would turn on , the voltage of drain of "N18" would change from logic "1" to logic"0", at last, the "OC_Flag1" would change from "1" to "0" as soon as over current occurs. The over current threshold may be easily calculated with the following equations.

$$I_{N10} = \frac{(W/L)_{N10}}{(W/L)_{N1}} \cdot I_{N1}$$
(1)
$$I_{P10} = \frac{(W/L)_{P10}}{(W/L)_{P1}} \cdot I_{P1}$$
(2)

When short circuit occurs between output pin "OUT1" and power ground, the output MOSFET "P1" is easy to be damaged for over current, so pMOS "P10" is connected as a mirror current source to sampling over current floating through "P1". As soon as over current occurs, the voltage of node "A" would reduce and "P16" would shut off, voltage of drain of "P16" would change to logic "0", "P17" would turn on, the drain of "P17" would change to logic "1", at last, the "OC Flag1" would change from "1" to "0" as soon as over current occurs.

The third kind of short circuit occurs between output pin "OUTP" and "OUTN". Because speaker load is bypassed, the current through two buffers (P1 and N2, or P2 and N1) increases largely similarly. At the same principle, the proposed short current protection scheme can also work well to real-time shut down power buffer.



Figure 7: Novel over current detection

5. Future Work

Above described circuits were few over current protection circuits. These all have some advantages and disvantages. Future work must contains regarding the improvement of previous given circuits. The parameters like power dissipation of over all circuit, output power, threshold current , efficiency of the circuit, THD, delay etc should be of main concern when they will be studied.

6. Conclusion

The over current protection circuit described in this paper is a summarized form of different over current protection circuits. This paper shows a hierarchy of over current protection circuits from earlier to current work in this area. These all circuits are different from each other and all are used in different application such as USBs,smart power devices, power amplifier etc.

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