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Review on Different Types of Power Efficient Adiabatic Logics

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Abstract: ***This paper shows a new adiabatic approach known as Positive Feedback Adiabatic Logic. Adiabatic circuits and static CMOS logic are used in low power VLSI chips to achieve improved device performance. Power reduction is achieved by recovering the energy in the recovery phase of the power clock. The power saving in the adiabatic logic over static CMOS logic can reach more than 90%. The main goal of this paper is to provide low power solutions to VLSI designers. The dynamic power requirement of CMOS circuits is a major concern in the design of personal information systems and large computers. The clocking schemes and signal waveforms are different from those of standard CMOS circuits. Adiabatic logic provides a way to reuse the energy stored in load capacitors rather than the conventional way of discharging the load capacitors to the ground and wasting this energy.***

Keywords: Static CMOS, Adiabatic logic , Low power, Energy dissipation , PFAL, Energy recovery**.**

1. Introduction

Energy efficiency has become a major design concern in high performance and mobile computer systems. Excessive power dissipation requires increasingly large, heavy, expensive, and noisy cooling machinery including special packages, heat sinks, heat pipes, and fans. Excessive energy consumption on mobile computer systems results in increasingly large, heavy, and expensive batteries, power conversion circuits, or fuel cells, which themselves may introduce further heat removal issues. Several effective power management design techniques have been developed over the past few years, including lowering the supply voltage. As process scaling continues below 90nm, however, it becomes more difficult to scale the supply voltage for several reasons. The Energy dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter circuits. It is finding that adiabatic technique is good choice for low power application in specified frequency range.

2. Operation of Adiabatic Logic

The word ADIABATIC comes from a Greek word that is used to describe thermodynamic processes that exchange no energy with the environment and therefore, no energy loss in the form of dissipated heat. In real-life computing, such ideal process cannot be achieved because of the presence of dissipative elements like resistances in a circuit. However, one can achieve very low energy dissipation by slowing down the speed of operation and only switching transistors under certain conditions. The signal energies stored in the circuit capacitances are recycled instead, of being dissipated as heat. The adiabatic logic is also known as ENERGY RECOVERY CMOS[1].

It should be noted that [2] the fully adiabatic operation of the circuit is an ideal condition which may only be approached asymptotically as the switching process is slowed down. In most practical cases, the energy dissipation associated with a charge transfer event is usually composed of an adiabatic component and a non-adiabatic component. Therefore, reducing all the energy loss to zero may not possible, regardless of the switching speed. With the adiabatic switching approach, the circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems.

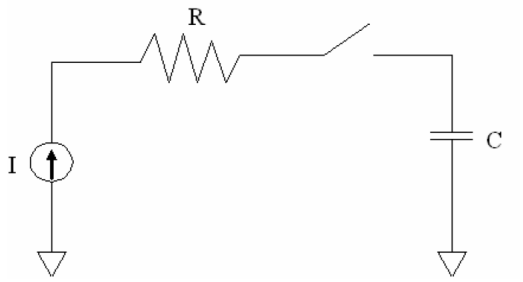


Figure 1: Circuit Explaining Adiabatic Switching.

Here, the load capacitance is charged by a constant current source (instead of the constant-voltage source as in the conventional CMOS circuits). Here, R is the resistance of the PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume, the capacitor voltage V_C is zero initially

The voltage across the switch = IR

$$P(t) \text{ in the switch} = I^2R \quad \ldots. (1)$$

Energy during charge = $(I^2R)\,T$

$$E = (I^2R)T = = \left(\frac{CV}{T}\right)^2 RT \quad \ldots\ldots. (2)$$

$$\text{Hence, } E = E_{diss} = \left(\frac{RC}{T}\right)CV^2 = \left(\frac{2RC}{T}\right)\left(\frac{1}{2}CV^2\right) \quad \ldots\ldots..(3)$$

Where , the various terms of above equation are described as follows:

E — energy dissipated during charging.
Q — charge being transferred to the load.
C — value of the load capacitance.
R — resistance of the MOS switch turned on.
V — final value of the voltage at the load.
T — time spent for charging.
Now, a number of observations can be made based on above Equation as follows:

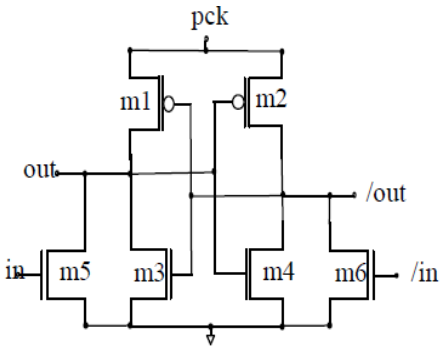
- The dissipated energy is smaller than for the conventional case, if the charging time T is larger than 2RC. That is, the dissipated energy can be made arbitrarily small by increasing the charging time.
- Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on-resistance of the PMOS network will reduce the energy dissipation.

3. Adiabatic Logic Circuits

There are the many adiabatic logic design technique [1] are given in literature but here four of them are chosen 2N-2N2P , ECRL , PFAL and CAL . The logic circuits such as inverter and inverter chain have been designed using these four adiabatic techniques. These adiabatic logic families show good improvement in energy dissipation as compared to conventional CMOS.

A. 2N-2N2P

The schematic 2N-2N2P inverter[1] gate is shown in Fig. 2. 2N-2N2P uses four phase clocking rule to efficiently recover the charge delivered by pck such as 'evaluation', ' hold', 'recover' and 'wait' is shown in Fig. 2. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to V_{DD}, since m5 and m2 are on so output 'out' remains ground level. Output '/out' follows the pck (evaluation phase). When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively (hold phase). This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck hence delivered charge is recovered (recover phase). Wait phase is inserted to maintain the clock symmetry. In this phase valid inputs are being prepared in the previous stage .



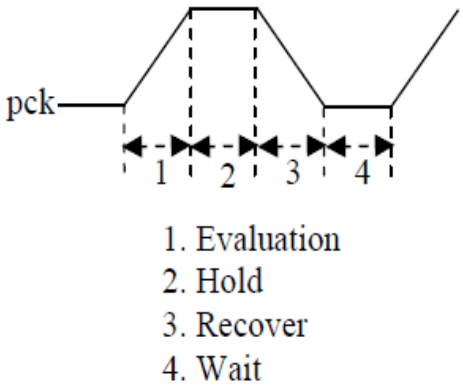


Figure 2: Schematic of 2N-2N2P inverter and power clock(pck)

B. Efficient Charge Recovery Logic (ECRL)

The schematic the ECRL inverter gate is shown in Fig. 3. ECRL also uses four phase clocking rule to efficiently recover the charge delivered by pck such as 'evaluation', ' hold', 'recover' and 'wait' is shown in Fig. 3. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to V_{DD}, since m3 is on so output 'out' remains ground level. Output '/out' follows the pck (evaluation phase). When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively (hold phase). This output values can be used for the next stage as an inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck hence delivered charge is recovered (recover phase). Wait phase is inserted to maintain the clock symmetry. In this phase valid inputs are being prepared in the previous stage .

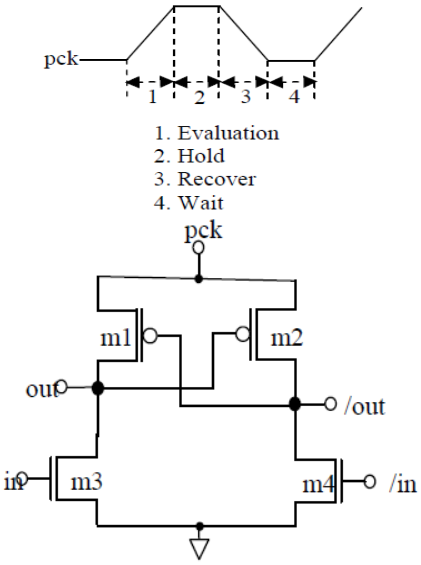


Figure 3: Schematic of ECRL inverter and power clock

C. Positive Feedback Adiabatic Logic (PFAL)

The schematic PFAL inverter[1] gate is shown in Fig. 4. PFAL uses four phase clocking rule to efficiently recover the charge delivered by pck such as 'evaluation', ' hold', 'recover' and input '/in' is low. When power clock (pck) rises from zero to V_{DD}, since m5 and m4 is on so output 'out' remains ground level. Output '/out' follows the pck (evaluation phase). When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively (hold phase). This output values can be used for the next stage as

an inputs. Now pck falls from V_{DD} to zero, '/out' returns its energy to pck hence delivered charge is recovered (recover phase). Wait phase is inserted to maintain the clock symmetry. In this phase valid inputs are being prepared in the previous stage .

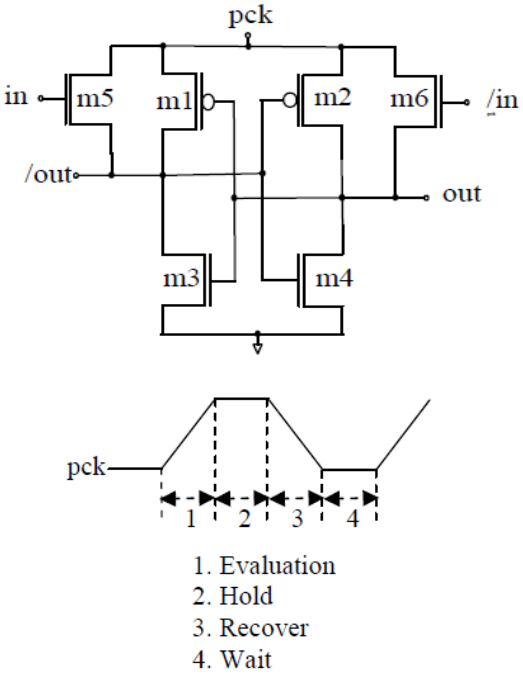
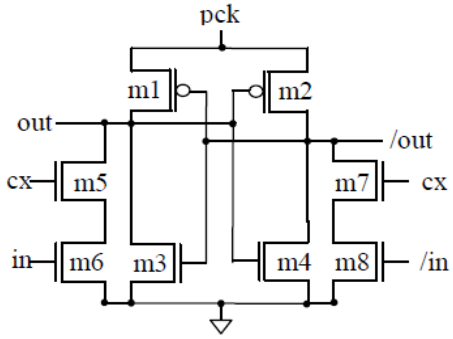


Figure 4: Schematic of PFAL inverter and power clock(pck)

D. Clocked Adiabatic Logic (CAL)

The schematic of the CAL inverter gate is shown in Fig.5. Clocked enable devices (m5 and m7) added in series with m6 and m8 respectively. The purpose of clocked enable devices is to allow operation with a single power clock pck. Initially, input 'in' is high and input '/in' is low. When auxiliary clock 'cx' is high and power clock (pck) rises from zero to V_{DD}, since m5 and m6 are on so output 'out' remains ground level. Output '/out' follows the pck (evaluation phase). When pck reaches at V_{DD}, outputs 'out' and '/out' hold logic value zero and V_{DD} respectively (hold phase). Now pck falls from V_{DD} to zero, '/out' returns its energy to phase). Now in next clock period, the auxiliary clock 'cx' is low disables the logic evaluation so previously stored logic state is repeated at the outputs 'out' and '/out', regardless of the inputs .



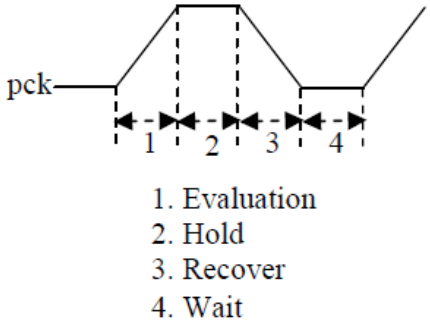


Figure 5: Schematic of CAL inverter and power clock(pck)

4. Adiabatic PFAL two input AND /NAND gate design

The partially adiabatic PFAL two-input NAND/ AND gate [4] can be implemented as shown below in the Figure 6. Power dissipation in this circuit is reduced up to 90% compared to static CMOS circuit design.

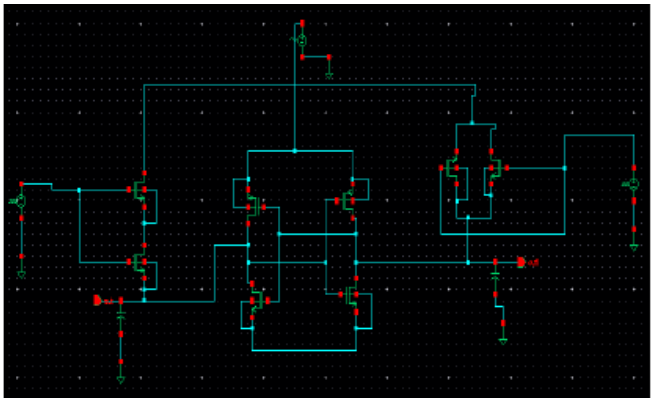


Figure 6: Schematic of PFAL AND/NAND Gate

5. Adiabatic PFAL Two Input OR /NOR Gate Design

An adiabatic PFAL OR/NOR gate [4] is implemented as below in Figure 7 .The OR/XOR gate implemented using PFAL will show reduced power dissipation as compared to the conventional CMOS logic.

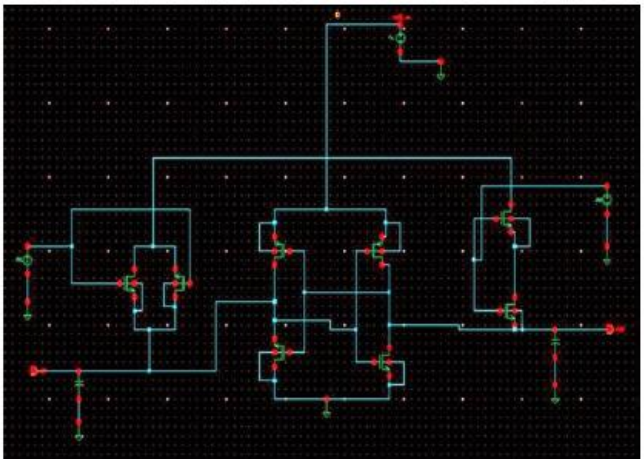


Figure 7: Schematic of PFAL OR/NOR Gate

6. Adiabatic PFAL Two Input EXOR /EXNOR Gate Design

An adiabatic PFAL exclusive-OR/exclusive NOR gate[4] is implemented as below in Figure 8. The EXOR/EXNOR gate implemented will show reduced power dissipation as compared to the conventional CMOS logic.

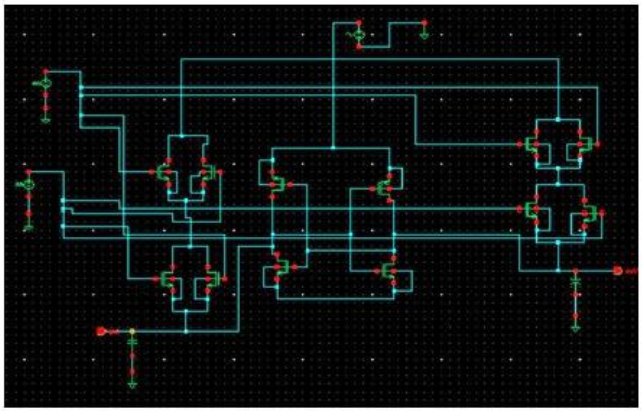


Figure 8: Schematic of PFAL EXOR/EXNOR Gate

7. Adiabatic PFAL 2:1 Muliplexer Design

A 2:1 multiplexer [5] is designed using PFAL logic, it contains two inputs A, B one select line S and outputs out and out bar shown in fig. 9. A sinusoidal power clock is applied Vpc. When input is low, the output terminal 'out' follow the sinusoidal power clock .This circuit reduces the power dissipation compared to static CMOS by using the recovery phase of the power clock.

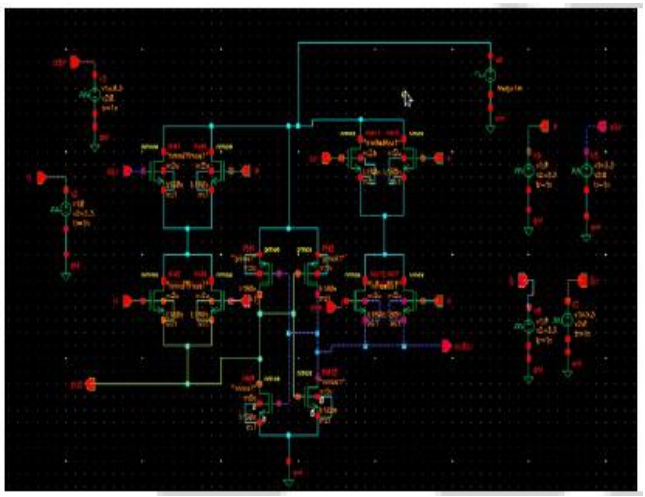


Figure-9 Schematic of PFAL 2:1 MUX

8. Adiabatic PFAL Full Adder Design

An adiabatic PFAL FULL ADDER is implemented as below in Figure 10. The FULL ADDER implemented using PFAL will show reduced power dissipation as compared to the conventional CMOS logic.

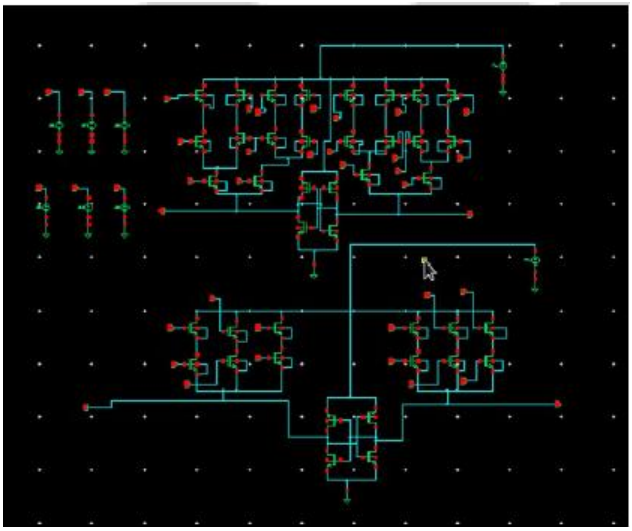


Figure 10: Schematic of PFAL FULL ADDER

9. Future Work

The above described circuits shows the reduced power dissipation compared to static CMOS circuit. In future , we will design circuits using PFAL,ECRL,CAL,2N-2N2P etc, adiabatic logic so that we can save power more than 90% in portable electronic devices , where power consumption is a major issue.

10. Conclusion

The adiabatic PFAL offers significant power reduction and so better power performance over conventional static CMOS. The above discussion shows that PFAL circuit can recover 50% of the energy dissipated in conventional static CMOS logic. However the PFAL suffers from large switching time, so it is not suitable to application where the delay is critical. Thus suffer from low speed of operation and is not suitable for the application where fast switching is required.

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