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Design and Simulation of Low Dropout Regulator

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Abstract: ***The proposed CMOS Low Dropout (LDO) regulator has been designed and simulated using TSMC 0.25µ CMOS process in cadence analog design environment . This paper illustrates the design criteria and corresponding analysis relevant to LDO. The experimental result shows that, it regulates an output voltage at 3.3V from a 3.5V supply, with a minimum dropout voltage of 200mV at a maximum output current of 50mA using a reference voltage of 1.2V. The regulator provides a load regulation of 0.092V/A, line regulation of 0.16mV/V. Efficiency of 93.27% is achieved. Detailed analysis of CMOS LDO has been presented.***

Keywords: Low Drop-out, Low voltage regulator, CMOS, Linear regulator, power supply circuits, operational amplifier**.**

1. Introduction

Power management is a very important issue in portable electronic applications. The need for multiple on-chip voltage levels makes voltage regulators a critical part of an electronic system design. Low-dropout linear regulators (LDOs) have gained popularity with the growth of battery-powered equipment. Portable electronic devices like cell phones require very efficient power management to increase the battery life whereas high-speed microprocessors need stable voltages that can supply fast varying currents on the order of few amperes. Low supply voltage noise is also an important requirement for noise sensitive RF circuits that are integral parts of all portable electronic devices.

The choice of a voltage regulator for a given application offers numerous design trade-off considerations. While switch mode regulators provide efficiencies that can reach more than 90% in many practical realizations, they are costly in terms of silicon area, and the magnetic elements are bulky and cause electromagnetic interference (EMI). Moreover, the output voltage ripple and output noise of switching regulators might not be acceptable for several applications such as critical RF circuits. On the other hand, linear regulators have very small output voltage ripple, are compact, have low output noise, and are stable with varying loads. However, linear regulators have lower efficiency that depends on the dropout voltage, which is defined as voltage difference between unregulated supply voltage and regulated output voltage. The minimum permissible dropout voltage of a linear regulator defines the maximum achievable efficiency.

The emphasis on efficiency has made low dropout (LDO) regulators the most popular class of linear regulators. But this increase in efficiency is achieved at the cost of a compromise in stability of the regulator. LDO regulators have high output impedance; this impedance, along with the load capacitance, creates a low frequency pole and decreases the overall phase margin. The increase in power consumption of portable electronic appliances, low power and high performance LDO is required. To meet the above mentioned requirements, several advanced techniques are proposed and presented to design a high performance LDO with fast load transient response, high power supply rejection ratio, small inrush current, good load Regulation and precise over current protection. Bandwidth is another important specification in voltage regulator design. The higher the bandwidth of a regulator, the more quickly it can react to changes in input and power supply and keep the output voltage constant. High bandwidth also improves the power supply rejection ratio (PSRR) of the regulator, which is a measure of how well the regulator attenuates noise on the power supply. The better the power supply rejection, the less the output voltage changes in response to fluctuations in the supply[3]. Therefore, to achieve good specifications, a novel LDO with a very simple circuit structure is employed. Transistor level implementation of the design is realized in 0.25u CMOS process

2. Low Dropout Regulator Structure and Schematic Design

The structure of the proposed LDO is shown in Fig.1. The building block of the LDO circuit consists of three parts: the error amplifier, the pass element, and the feedback resistor.

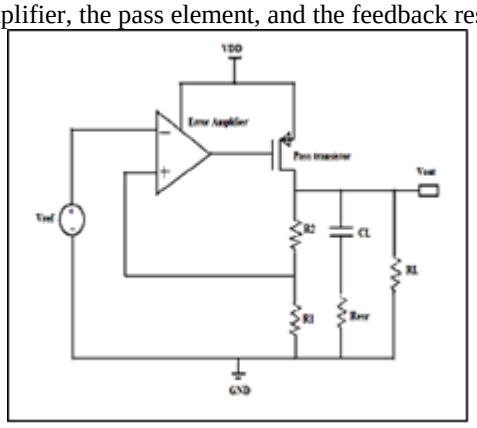

Figure 1: Proposed LDO circuit diagram

The PMOS differential pair error amplifier (with a current mirror providing a constant current supply for the error amplifier) is used to provide error signal for voltage regulation and common source amplifier which has a high output swing. Pass device function as the voltage-controlled current source, which is made up of PMOS transistor. Feedback path consist of R1, R2 resistors. The high loop gain provides good line and load regulations.

The circuit schematic in Fig.2 shows that the error amplifier is a PMOS differential pair, while the second gain stage is a common source stage, with a bias-current source. The output swing of the second stage is much better than the source follower in turning on or off the power transistor, and therefore this configuration is suitable for low-voltage LDO designs. The current mirrors provide current sources for both stages. The error amplifier is implemented using a two stage without miller compensation topology in order to achieve a gain larger than 60dB and GBW =5MHz using 0.25µm CMOS technology.

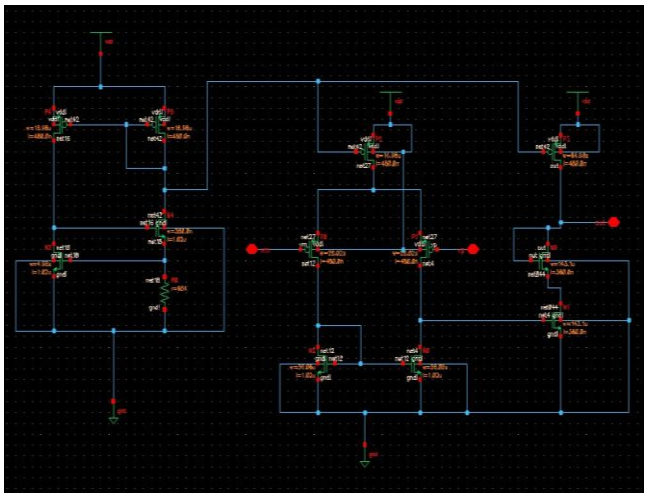

Figure 2: Schematic of two stage operational amplifier

The power transistor (MPT) is designed to operate in linear region at dropout. Although the voltage gain of the power transistor is less than unity, the loop gain is not degraded due to the error amplifier and the second gain stage. A loop gain of more than 60dB and gain bandwidth more than 5MHz can be easily achieved in the proposed design and is sufficient for good line and load regulations. In the proposed design, for the good transient response performance reason, the transistor size reaches millimetre or even centimetre orders, which generates a bigger gate capacitance. The input voltage Vin works from 3.5V to 4V, which is the proposed LDO's regulating range.

2.1 Design of LDO

The Design of LDO can be subdivided into design of power transistor (MPT) and design of two stage operational amplifier

2.1.1 Design of Error Amplifier

A procedure is developed that will enable a first-cut design of the two-stage op amp. The hand calculation approaches 70% of the design process. The two stage op amp is designed for the following specs.

Table 1: Design specifications of operational amplifier.

Av≥1500V/V	GBW>5MHz	VDD=1.75V	VSS=-1.75V
Cl=10pF	SR>10 V/µs	Pdiss>2mW	ICMR=1.75V to -1.75V

In order to simplify the notation, it is convenient to define the notation Si = Wi/Li = (W/L)i , where Si is the ratio of W and L of the ith transistor. We assume that gm1 = gm2 = gmI, gm6 = gmII.

The first step is to calculate the minimum value of the compensation capacitor CC, it was shown that placing the output pole P2 2.2 times higher than the GB permitted a 60 phase margin (assuming that the RHP zero Z1 is placed at or beyond ten times GB). It was shown that such pole and zero placements result in the following requirement for the minimum value for Cc:

$$C_C = 0.22\, C_L$$

Next determine the minimum value for the tail current I5, based on slew-rate requirements.

$$I_5 = SR\,(C_C)$$

The aspect ratio of M3 can now determined by using the requirement for positive input common-mode range.

$$S_3 = \left(\frac{W}{L}\right)_3 = \frac{I_5}{K_3'\left[VDD - Vin_{max} - |\mathrm{Vto}|_{3,\max} + \mathrm{Vt}_{1,\min}\right]^2}$$

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$$

Requirements for the transconductance of the input transistors can be determined from knowledge of Cc and GB. The transconductance gm1 can be calculated using the following equation:

$$gm_1 = GBW \times C_c$$

The aspect ratio (W/L)1 is directly obtainable from gm1 as shown below:

$$S_1 = \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{gm_1^2}{K_1' \times I_5}$$

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate VDS5 using the following relationship shown:

$$Vds_5 = Vin_{(\max)} - Vss - \left(\frac{I_5}{\beta}\right)^{\frac{1}{2}} - Vt_{1,\max}$$

With VDS5 determined, (W/L)5 can be extracted using the following way

$$S_5 = \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 = \frac{2I_5}{K_5' \times (Vds_5)^2}$$

$$\left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6$$

At this point, the design of the first stage of the op amp is complete. We next consider the output stage. For the phase margin of 60, the location of the output pole was assumed to be placed at 2.2 times GB then zero is placed at least ten times higher than the GB. The transconductance gm6 can be determined using the following relationship:

$$gm_6 \geq 10 gm_1$$

So for reasonable phase margin, the value of gm6 is approximately ten times the input stage transconductance gm1. At this point, there are two possible approaches to completing the design of M6 (i.e., (W/L)6 and I6). The first is to achieve proper mirroring of the first-stage current-mirror

load of (M3 and M4). This requires that VGS4 = VGS6 then assuming gm6 = 1319µs and calculating gm4 as:

$$gm_4 = \sqrt{2 \times (\mu nCox)_4 \times \left(\frac{W}{L}\right)_4 \times Id_4}$$

We use equation to get:

$$S_6 = \left(\frac{W}{L}\right)_6 = S_4 \times \left(\frac{gm_6}{gm_4}\right)$$

Knowing gm6 and S6 will define the dc current I6 using the following equation:

$$I_6 = \frac{gm_6^2}{2 \times K_6' \times S_6}$$

The device size of M7 can be determined from the balance equation given below:

$$S_7 = \left(\frac{W}{L}\right)_7 = \left(\frac{W}{L}\right)_5 \times \left(\frac{I_8}{I_5}\right)$$

At this point, the design of Error amplifier is complete as shown in fig.4.

2.1.2 Design of MPT stage

The design step of power transistor stage is as follows:
Since

$$Vdropout \approx 200mV \Rightarrow Vdssatpass \leq 200mV$$

The equation for the drain current is given as follows:

$$I_D = \frac{1}{2} \mu pCox \left(\frac{W}{L}\right) (Vdssatpass)^2$$

$$\Rightarrow \left(\frac{W}{L}\right) = \frac{2I_D}{\mu pCox (Vdssatpass)^2}$$

Assuming µpCox value
The pass transistor size can be calculated by

$$\left(\frac{W}{L}\right) = X$$

Let X be the size of pass transistors
In order to minimise the gate capacitance, we use minimum length L=0.6µm
W= X × 0.6µm
The gate capacitance of the pass transistor is given by the following equation:

$$C_{gate} = C_{gs} + (gm_p \times R_{par} + 1) C_{gd}$$

Where,

$$C_{gs} = \frac{2}{3} \times W \times L \times C_{ox}$$

$$C_{gd} = W \times L_D \times C_{ox}$$

$$R_{par} = R_{ds} \| (R_1 + R_2) \| R_L$$

$$R_{ds} = \frac{1}{\lambda I_{ds}}$$

The vales of Cgs and Cgd can also be obtained if we run a DC simulation and verify the operating point of the pass transistor. Using this last method, we found:
R1 and R2 are calculated using:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) V_{ref}$$

$$R_L = \frac{V_{out}}{I_{load}}$$

The Fig.5 shows the overall architecture of voltage regulator. The output accuracy of the proposed LDO is high with regard to the effect of the offset voltage since there is only two pair of devices that require good matching. The offset voltage due to large variations at the error amplifier output, occurring in the classical LDO's, is reduced in proposed LDO due to the gain stage formed by M6 and M7. In the simple circuit structure, the output noise of the proposed LDO is low.

Table 2: Design values of Pass transistor

MPTL=0.6µm	MPTW=40mm	Vref=1.2V	CL=10µF
R2= 420kΩ	R1=240kΩ	Resr=5Ω	RL=66Ω

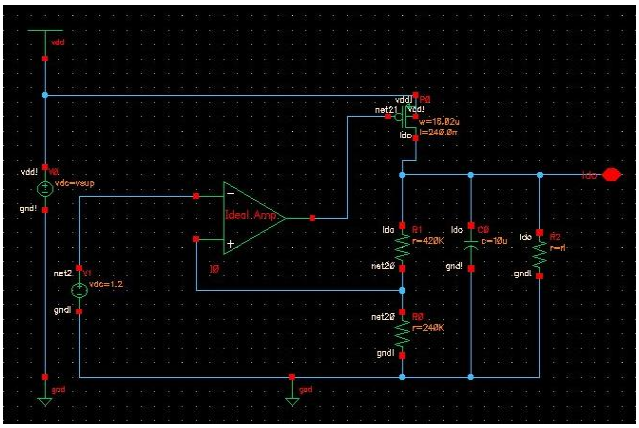

Figure 3: Complete design of a Low Dropout Regulator

3. Experimental Results

The proposed LDO is designed in TSMC 0.25µm CMOS process. The LDO is capable of operating from 3.3V to 4V, which covers a wide range of the typical battery voltage. A dropout voltage of 200mV at a 50mA maximum load current is achieved.
The important aspects of the LDO can be summarized into three categories, namely, regulating performance, quiescent current, and operating voltage. Other specifications that serve as metrics for the LDO include dropout voltage, Line regulation, Load regulation, output voltage variation resulting from a transient load current step, quiescent current, maximum load current, input/output voltage range etc.

Fig.6 shows the input/output simulated characteristics of the 3.3V LDO regulator. LDO output voltage starts stabilizing to 3.3V when input voltage is 3.5V. The dropout voltage of LDO is 200mV (3.5V – 3.3V) at 50mA. An input voltage of 3.5V and bias current of 30µA is supplied to the LDO. A small resistance of 1pΩ is connected on the path to the ground to measure the quiescent current. Quiescent current is observed to be 0.544mA.

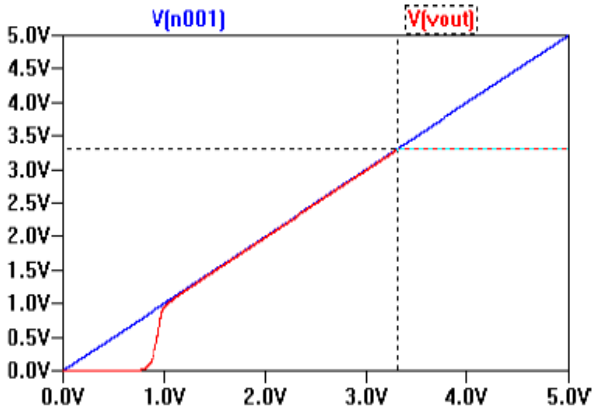

Figure 4: Dropout Voltage regulator.

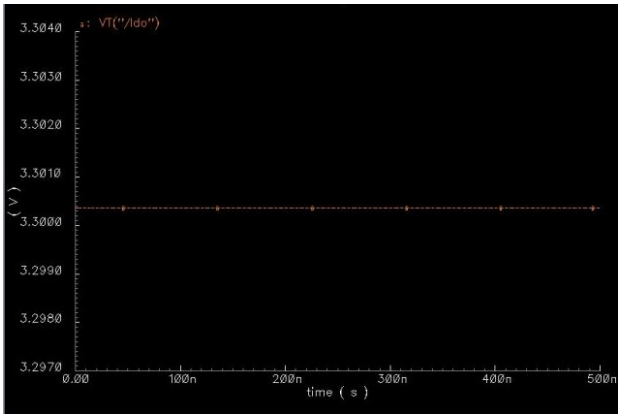

Figure 5: Transient result of output voltage of LDO

Owing to the high loop gain provided by the design structure and extremely large size of power transistor, both line and load regulations are pretty good. The results are as shown in the below figures.

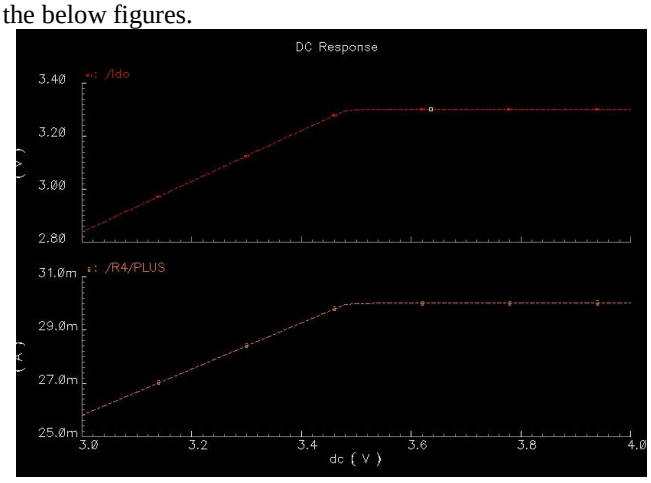

Figure 6: Line Regulation of output voltage and current

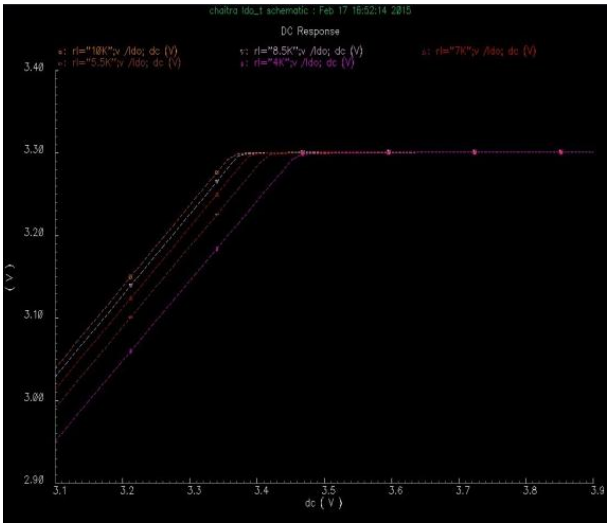

Figure 7: Load Regulation of output voltage

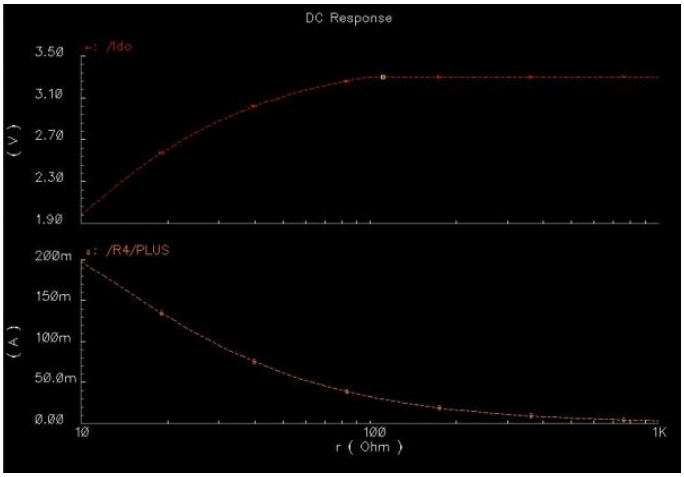

Figure 8: Load Regulation of output voltage and current

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows.

$$Efficiency\ at\ 3.5V = \frac{IoVo}{(Io+Iq)Vi} \times 100$$

Moreover, the power supply rejection (PSRR) is -22dB @ 100KHz as shown in Fig.10. A simple circuit technique is presented for improving PSRR of a proposed LDO.

4. Conclusion

A Low power LDO was designed with a dropout of 200mV, and the output voltage of 3.3V with load and line regulation of 0.092V/A and 0.16mV/V and power supply rejection ratio of -22dB at 100kHz is achieved. The use of technique to improve PSRR performance of LDO is considered with large improvement of PSRR ratio of -170dB at 100kHz. Efficiency of 93.2% is achieved. The designed LDO is suitable for Powering up.

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