Design of CMOS Tapered Buffer for High Speed and Low Power Applications using 65nm Technology

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Abstract: This paper describes the power dissipation and propagation delay issues in CMOS buffer circuits while driving large capacitive loads which are often presents in CMOS IC's and proposes a CMOS buffer design for minimizing power dissipation and propagation delay. The reduction in power dissipation is achieved by minimizing short circuit power and subthreshold leakage power which is predominant when supply voltage (V_{DD}) and threshold voltage (V_{th}) are scaled down for low voltage applications. The proposed buffer has been designed and simulated using Tanner SPICE tool in 65 nm VLSI technology. The results show that modified taper buffer design has a substantial amount of decrease in power dissipation.

Keywords: CMOS, Taper Buffer, VLSI

1. Introduction

In CMOS integrated circuits, large capacitive loads occur both on-chip (where high localized fan-out is often encountered) and off-chip (where highly capacitive chip-tochip communication lines exist). In order to drive these large capacitive loads at high speeds while ensuring that the load placed on previous stages of the signal path is not too large buffer circuits are required which must source and sink relatively large currents quickly while not degrading the performance of previous stages. These buffers are used in the memory access path as word-line drivers, to drive large off-chip capacitances in I/O circuits and in clock trees to ensure that skew constraints are satisfied.

The tapered buffer is placed between the logic/registers and the large capacitive load. The tapered buffer provides a high impedance input, so as not to load down the logic registers and sources (sinks) high current able to quickly charge (and discharge) the large capacitive load. Thus, the buffer isolates the logic registers from the load amplifying the signal along the way. Historically, the supply voltage (V_{DD}) has been scaled down in order to keep the dynamic power consumption under control. Hence, the transistor threshold voltage (V_{th}) has also been scaled down. Threshold voltage should be kept between $0.2V_{DD}$ and $0.4V_{DD}$ to achieve minimum power dissipation. This is desirable to maintain a high drive current and achieve performance improvement.

High-performance VLSI design is attracting much attention because of rising need for miniaturization and hence design optimization for trading-off power and performance in nanometer scale integrated circuits is the need of the present scenario which demands a decrease in both supply voltage V_{DD} (to maintain low power dissipation) and threshold voltage V_{th} (to sustain propagation delay reduction) but the fact is that the decrease in V_{th} not only increases leakage power but also short circuit power. The paper is organized as follows: In section II simple buffer and its specifications are discussed. In section III taper buffer and its design aspects are discussed. Section IV presents proposed CMOS taper buffer design. The concept of power delay optimization is discussed in section V.The results and discussions are reported in Section VI.

2. Buffer

A buffer in an operating system is a temporary storage location for data while the data is being transferred. During the write process, buffer can be used as a work area where control words can be inserted into a data stream. The block data is then written to the device. In electronics, buffer is an electronic circuit whose primary function is to connect a high impedance source to a low impedance load without significant distortion in signal. Buffers are generally applied in analog systems to minimize loss of signal strength due to excessive loading of output nodes. A buffer is a unity gain amplifier. A buffer amplifier is one that provides electrical impedance transformation from one circuit to another. A voltage buffer is used to transfer voltage from one circuit having high output impedance to another circuit having low input impedance.

A current buffer is used to transfer current from one circuit having low output impedance to another circuit having high input impedance. Buffer amplifiers are used for impedance matching. In general, a buffer is something that serves as a potential barrier. In circuit design, it is an amplifier that provides an interface between mismatched circuit elements. Buffers are used when signal source doesn't have sufficient capacity to deliver the current to load circuit. If buffers are not used then a problem called input loading occurs which causes the circuit to be malfunctioned or damaged.

3. CMOS Tapered Buffer Design

This section presents the details of concept of CMOS taper buffer design. The split capacitor model of taper buffer is used here. The split-capacitor model is introduced by

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Kanuma. The model is named as split capacitor model because the input gate capacitance C_i and the output diffusion capacitance C_d of the inverter are modelled separately which provides improved accuracy as compared to the single capacitor model utilized by Lin and Linholm and Jaeger.

The tapered buffer design consists of a chain of inverter stages where width of each MOS transistor in a stage is increased by a constant factor (called tapering factor) than that of the transistors placed on the previous stage. The constant increase in width of transistors in each stage provides fixed ratio of output current drive to output capacitance and hence equal rise, fall, and delay times for each stage.

CMOS tapered buffers are frequently used to drive large capacitive loads which arises from long global interconnect lines such as clock distribution networks, high capacitance fan out, and off-chip loads. Typically, local interconnect Capacitance is assumed to be negligible during the design of these tapered buffer systems.

However, the interconnect capacitance within the buffer system can be significant, particularly when floor planning considerations require the Buffer to be located in separate functional blocks or different rows of cells. Design of taper buffer is based on analytical modeling of performance criteria and analyzing them individually with respect to the parameters like capacitive load dependent tapering factor and number of stages which are the two primary variables in the design of tapered buffers.



Figure 1: N stage Taper Buffer

Here C_i denotes the input capacitance of minimum size inverter, C_d denotes the drain capacitance of minimum size inverter, C_{load} denotes the load capacitance of the last stage inverter, N denotes number of stages in the buffer chain and F denotes the scaling/tapering factor per stage in the inverter buffer chain. The number of buffer stages(N) required depends upon the technology dependent tapering factor (F), load capacitance and input capacitance of buffer.

$$N = \frac{\ln(CL/Ci)}{\ln E}$$

The technology dependent tapering factor (F) is given by, $F[\ln(F)-1] = C_d/C_i$

The power dissipation in the taper buffer has three main components which are dynamic power, short circuit power and sub-threshold leakage power. Hence total power dissipation is given by,

 $P_{t} = P_{dyn} + P_{S.C.} + P_{sub}$ where,

$$P_{dyn} = V^2_{DD} f(C_d + FC_i) \left(\frac{\frac{C_L}{C_i} - 1}{F - 1} \right)$$

$$P_{S.C.} = P_{dyn} \left(\frac{9}{8} + \frac{V_{DO}}{0.8V_{DD}} ln \frac{10V_{DD}}{eV_{DD}} \right) \times \frac{1}{\alpha - 1} \frac{1}{2^{\alpha - 1}} \frac{(1 - 2V_T)^{\alpha + 1}}{(1 - V_T)^{\alpha}}$$

$$P_{sub} = V_{DD} l_{sub} \left(\frac{\frac{C_L}{C_i} - 1}{F - 1} \right)$$

4. Proposed Buffer Design

It is known that the most of the power dissipation in CMOS circuits is caused by charging/discharging of the output node and by the short-circuit current that flows from the power supply to the ground during switching of structures. In CMOS buffer circuits the short circuit power dissipation is important because in VLSI circuits a great amount of energy is dissipated due to on-chip and off-chip signal driver circuits, which are based on inverting buffers. The problem becomes more complicated when the input signal operates at high frequencies because the number of times the power dissipates in a specific interval may also be proportionately high. So, it is desirable to reduce the short circuit power dissipation.

Hence a modified buffer design approach is proposed which dissipates lesser power because the short circuit component of power is eliminated in the design by tri-stating its output node momentarily before every output signal transition. This is achieved by applying the gate driving signal of PMOS (NMOS) transistor to NMOS (PMOS) transistor of the output stage through a feedback network which delays the driving signal and avoids simultaneous activation of NMOS and PMOS transistors during signal transition which is the cause of short circuit current. Further, the capacitive load dependent tapering factor is applied to all the stages including the final stage.



Figure 2: Proposed design of 4 stage Taper Buffer

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In Figure 2 a 4 stage proposed taper buffer is given in which input signal is applied at IN which is amplified by 1st and 2nd stage. The feedback network is applied in 3rd and 4th stage where T2, T3, T6, T8 are NMOS transistors and T1, T4, T5, T7 are PMOS transistors. INV1 and INV2 are minimum sized inverters which are connected to the gate terminals of T7 and T8 for their input and with T5 and T2 as output respectively. The output of 2nd stage is connected to T1, T3, T4 and T6 only.

5. Power and Delay Optimization

While working in nano-meter scale technology the total power dissipation of clock drivers (which generally have CMOS inverters) is quite large and have 30 to 50% share only of the short circuit current and sub-threshold leakage current. To solve this problem of high power dissipation and high propagation delay, a design scheme has been proposed which not only minimizes short circuit power and sub-threshold leakage power but also optimizes propagation delay. The short circuit power dissipation can be minimized by designing a circuit with extra feedbacks so that to avoid simultaneous activation of NMOS and PMOS. Sub-threshold leakage power can be minimized by maintaining threshold voltage between $0.2V_{DD}$ to $0.4V_{DD}$. Propagation delay can further be reduced by increasing no. of buffer stages.

6. Result and Discussions

Schematics of buffer are drawn on S-EDIT using 65nm technology file. These simulation and results are obtained from T-SPICE. Computations have been made for parameters like tapering factor, no. of buffer stages etc. under different load conditions. Both designs have been compared on performance parameters like power dissipation and propagation delay.



Figure 3: Schematic of 2 stage Proposed Taper Buffer



Figure 4: Design of 4 stage Conventional Taper Buffer



Figure 5: Design of 4 Stage Proposed Taper Buffer



Figure 6: Waveform of Taper Buffers (2 and 4 stage)

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F C_{L (fF)} N Tapper Buffer Proposed Buffer % Increase in Propagation Propagation Power Power % Decrease in Power delay (ns) dissipation delay (ns) dissipation Propagation (uW) (uW) Dissipation Delay 0.05873 0.07637 15 1.26 0.21049 0.14988 28.79 30.03 2 3.02 0.37434 0.28265 24.49 75 3 0.0677 0.09136 34.94 150 0.08166 0.89442 39.81 4 2.720.114180.57201 36.04 1500 0.14435 3.1409 0.19575 2.5679 18.24 5 3.53 35.6

Table 1: Comparison for Propagation delay and power dissipation between conventional and proposed tapered buffers

7. Conclusion

In this paper power dissipation and propagation delay parameters are calculated during design of CMOS buffer driving large capacitive loads. The proposed buffer has been designed using 65 nm technology and simulated using TANNER EDA tool. A reduction of 18-36% in power dissipation has been achieved but with that an increment of 30-40% in propagation delay is obtained for different no. of buffer stages because of power-delay trade off. Hence, the proposed buffer can be used to provide power efficient solutions for portable VLSI applications at optimum propagation delay. This ideology is applicable to design circuits where micro watts of power dissipation become major factor and less amount of power to drive the circuit. This type of design circuitry is use where power dissipation is more important to minimize as compared to propagation delay.

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