the implementation is carried out without manual placement or routing. Also a high resolution is acquired with excellent linearity and monotonicity. It is basically demonstrated through a 1 MHz clock frequency and 14 bit DPWM. But in accordance with (2), the DCM resources are also used in order to match the clock period to the delay line of 2^M elements. So taking into account the frequency limit of DCM, a 178 MHz clock is experimentally tuned to well match the delay elements. Besides all these advantages there are certain parameters that must be taken into account.

Although the carry chains or the delay line is auto-placed using the FPGA programming tools, the decoding logic still require very careful manual placement and routing which increases complexity and development time. Moreover including an asynchronous circuit makes the static timing analysis harder to perform and may result in glitching due to routing and controlling of logic.

Table 1: Delay line and DCM comparison

Delay line based DPWM	*DCM based DPWM*
Implemented in Xilinx Virtex 4 FPGA	Implemented in Xilinx XC3S500E Spartan 3E FPGA
Architecture include both synchronous and asynchronous parts	Fully synchronous
Internal logic blocks used for implementation.	Implemented using a single embedded resource i.e. DCM
1 MHz clock frequency	50 MHz clock frequency (maxim 200 MHz limited for DCM)
Resolution obtained -90ps	Resolution obtained – 625ps

The second approach i.e. the DCM based DPWM is a fully synchronous architecture. A synchronous design improves the reliability of circuit and eases the design process. Besides it makes the design more independent and improves the design portability.

As compared to the delay line approach the DCM implementation is much simpler and efficient, since various logic blocks has to be used if a large bit carry chain is required. Further, even the delay line approach makes use of the DCM resource in order to improve the resolution. Although the DCM approach utilize the manual placement or routing method, the placement is made close such as a minimum routing delay is observed. The comparative analysis is summarized in table 1.

5. Conclusion

Several architectures are presented till date regarding the high resolution DPWM and each comprised of certain advantages and disadvantages. In the continuing effort to improve the results the proposed paper reviews the two recent architectures of DPWM which are implemented in two families of FPGA. It has been observed that the delay line method eases the implementation by excluding the manual placement methods, whereas the DCM provides a high resolution PWM in a simpler way being a low cost device. Hence it would be preferred to carry out a more enhanced architecture using the DCM blocks in order to achieve a high coarse resolution leading to an efficient application for digital control.

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