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Generation of a High Resolution Digital Pulse-Width Modulator through Digital Control in General Purpose Field Programmable Gate Array

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Abstract*: Pulse width modulators are the basic building block in digital control architectures of any power converters. The design of power converters requires a high resolution high frequency pulse width modulators (HRPWMs) in order to reduce the size and cost, improved dynamic behaviour and power density. Hence, this paper proposes a review of digital pulse-width modulation (DPWM) architecture that takes advantage of the field programmable gate array (FPGA) advanced characteristics, especially the Internal Logic Blocks (Internal Carry Chain) present in the Virtex 4 FPGA and the Digital Clock Manager (DCM) present in the low cost Spartan – 3E FPGA. Given the interest of obtaining high-resolution DPWMs, a lot of different architectures have been proposed in the last years, and even a classification of them has appeared. These architectures are designed and compared to analyze the performance.*

Keywords: DPWM, DCM Block, Delay line, Digital Control, Signal Resolution.

1. Introduction

Recent development in digital control and semiconductor technology has enabled the use of higher switching frequencies through power devices. Thereby allowing the design of power converters with reduced size and cost, and improved dynamic behavior and power density. However, these designs require high-frequency high-resolution PWMs (HRPWMs) in order to take the most of the power converter [1]. Compared to the analog control techniques, conventionally applied in power converters, the digital control offers the following advantages: flexibility, reliability, expandability [2] along with programmability, advanced control algorithms, reduced component count, low sensitivity to external factors or ageing, ease of design, prototyping, etc. [3]. In contrast to the IC controller realizations, digital controller design scales well and can thus take advantage of advances in fabrication technologies.

Since their introduction during the 1970s, digital control systems have become more attractive as they allow the implementation of complex control strategies with the powerful calculations and math-intensive algorithms. In the field of power converters and drives high-performance digital devices are needed as many or most of the advanced control techniques could not be implemented at all, due to their complexity and the very short control interval.

Power converters offer a high capability to efficiently manage electrical energy flows. Until a few years ago, their primary use was in supplying motors in industrial applications and in electric traction systems. Nowadays, in addition to those fields they are employed in a very wide range of low, medium, and high power applications including residential applications, renewable energy systems, distributed generation, and automotive. Hence digital control represents a key element of modern power converters [4].

The basic building block in digital control architectures of any power converter is the digital pulse width modulator (DPWM) [1].The important thing to take into account regarding the DPWM or any power converter is its resolution. The accuracy of system mostly depends on the resolution of PWM. It is one of the important drawback of digital control. The need of high resolution DPWM is because of a factor named limit cycling [5]. Limit cycles, i.e., oscillations of the regulated output under steady-state operation, which result from the presence of quantizers (of the sampling and control units) in the control loop. The issues of limit-cycle oscillations are addressed in various digitally controlled pulse width modulation (PWM) converters, trying to resolve up to great extent [6], [7].

2. Need of FPGA

The Field Programmable Gate Array (FPGA) is a general-purpose device filled with digital logic building blocks. FPGA-based systems can literally rewire their internal circuitry to allow reconfiguration after the control system is deployed to the field. FPGA devices deliver the performance and reliability of dedicated hardware circuitry.

Present converters are provided with higher switching frequency beyond MHz, which needs high resolution DPWM and high computation throughput in order to gain high power density and better dynamic performance. Most of the DSPs and ASICs are unable to fulfill such requirements, whereas, FPGAs are capable to control such converters due to its flexibility in re-configuring and hardware parallelism.

Due to the following advantages in [8], [9] and [10], FPGA is chosen to implement the desired concept of DPWM in contrast to other processors and controllers:

- Hardware Parallelism: Multiple control loops can run on a single FPGA.
- Reconfigurability: Can rewire the internal circuitry after

system is deployed to field.

- Compactness: Incorporation of millions of logic gates in a single IC, thereby reducing size.
- Improved performance: FPGA capabilities are measured in million instructions per second (MIPS) surpass DSPs, leading to faster program execution time and decreased processing delays, elevating one of the drawbacks of DSPs based digital systems.
- FPGA boards have evolved in system resources in terms of clock frequencies and memory capabilities as compared to DSPs.

3. DPWM- Architectural Review

Several DPWM architectures are presented in the open literature which include the Counter comparator [11], Delay line [12], [13], [11], Hybrid DPWM [14], Segmented delay line [15], Dithering [12], [16], etc. Each of the existing DPWM architectures has some advantages and disadvantages depending on the application. Taking into account the need for high resolution, two architectures are reviewed in order to achieve desired results for DPWM ; Delay line based DPWM and DCM based DPWM . They are described below with a comparative analysis and study.

3.1 DPWM architecture using Internal Carry Chains

This is a hybrid DPWM architecture to achieve the coarse counter resolution known as the delay line based appraoach [17]. Hybrid in the sense that it combines a synchronous and an asynchronous part. It provides with a high resolution without using very high frequency clock. This approach is based on the internal logic elements/blocks i.e. the carry chains present in one of the FPGA family to construct the delay line. The delay line consists of tapped delay elements and a multiplexer to control the amount of delay applied to the input signal. A simplified architecture of DPWM is shown if fig.1. As seen, it comprises of a synchronous (counter –comparator) and an asynchronous (delay line) part.

The synchronous part controls the duty cycle command, whereas the asynchronous part resets the duty cycle signal and determines the resolution. 2^M tapped delay line outputs passing through the multiplexer must be delay matched in order to achieve monotonicity. The carry chain used in [18] is a low latency path used to propagate the carry bit through consequtive 2-bit adders. The propagation delay t_p of the carry bit through each adder is fixed and it determines the time resolution of DPWM. Thus the total delay of carry chain is calculated as,

$$T_d = t_D + \mathrm{d} \cdot t_p \quad (1)$$

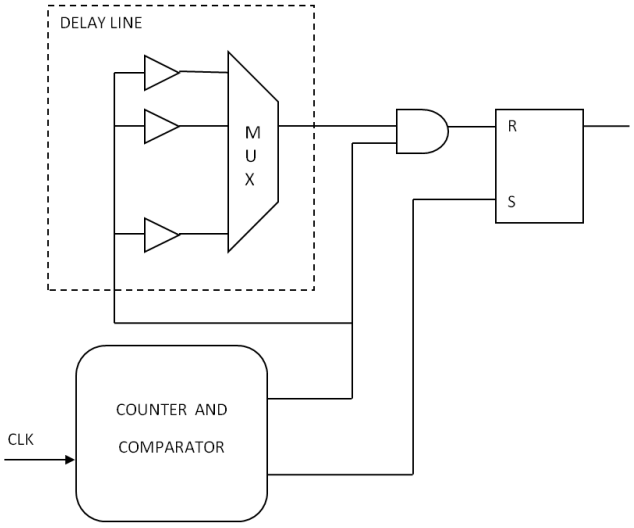
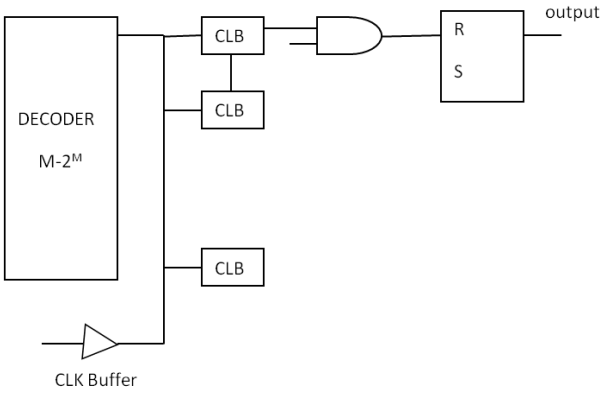
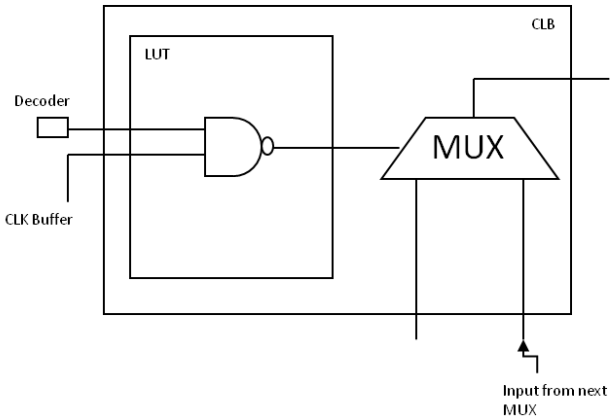


Figure 1: Delay line structure



(a)



(b)

Figure 2: (a) Carry chain block architecture (b) CLB structure

Where, t_D is the propagation delay from decoder to the carry chain, d is the duty cycle signal and t_p is the propagation delay of carry bit through each adder. Whereas ideally the clock period of hybrid DPWM is,

$$T_C = t_D + k \cdot t_p \quad (2)$$

The implementation of this DPWM architecture is carried out in the Xilinx Virtex-4 FPGA with inherently routing routines

which eliminate the need of manual placement or routing. It comprises of embedded memory blocks. Based on the carry chain logic block architecture fig.2 (b) shows the configurable logic block (CLB) which consists of a multiplexer acting as a delay element along with a look up table (LUT) carrying a NAND gate as shown in fig.2. It has been observed that the carry chain is allowed to begin only when the trigger signal goes high provided through the clock buffer.

It has been observed that the delay line resolution has reduced to slightly better than 90 ps, thereby leading to monotonic behavior without manual routing through 1MHZ clock frequency. When this architecture is combined with the counter-comparator part of fig. 1 , it would lead to far better resolution than 90 ps. Since 2^M tapped delay lines are to be delay matched in atleast one unit cycle, using (2) the DCM resources are used to match the clock period to a delay line of 2^M elements. The clock frequency used is around 178 MHz due to DCM usage.

3.2 DPWM architecture using DCM block

Digital Clock Manager is a clock managing feature, which is present in the advanced low cost FPGA –specifically the Spartan-3 FPGA series. It enables clock frequency multiplication, division and duplication along with generation of four phase shifting signals.[19], [20] and [1] Fig.3 shows a simplified diagram of a DCM block present in the Spartan-3 series.

The block basically comprises of four functional units:

1) Phase Shifting Unit: The most important unit of DCM which controls the phase relation of output clock with respect to the input clock thereby shifting the phase of the DCM clock output by a fixed fraction of input clock. It provides with four phase shifted clock versions-CLK0, CLK90, CLK180, and CLK270
2) Frequency Synthesizing Unit: It helps in clock frequency multiplication and division.
3) Deskew Unit: A deskew circuit is provided by the Delay Locked Loop (DLL) in order to generate clock output without any delay.
4) Status Logic: It indicates the current state of DCM whether the output is in phase with the input clock.

The DCM operation is explained as follows: According to [1] the first approach was mentioned using a single DCM in order to obtain 2 bit resolution increase. This approach made use of a multiphase circuit. It comprises of a synchronous digital circuit that generates the reset of the SR latch. Thus avoiding the asynchronous circuits in[19] and [20] which may cause glitching problems. Based on this approach a more advanced scalable architecture is introduced in order to improve the DPWM resolution as shown in fig. 4.

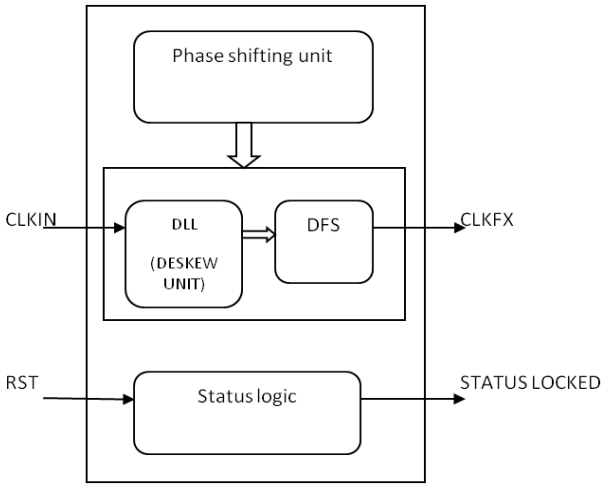
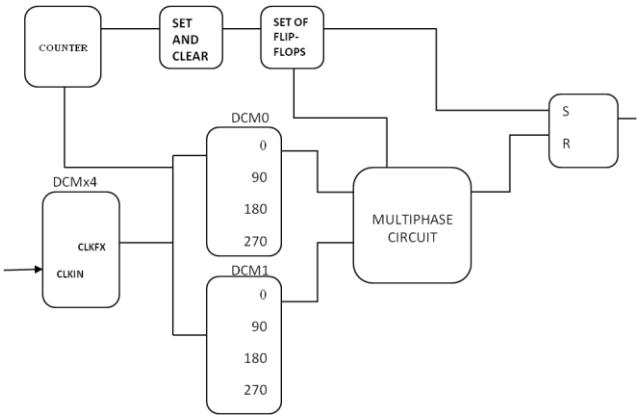


Figure 3: DCM functional block diagram



zigure 4: DPWM architecture

This architecture includes a duty cycle command dc, having x = n + k number of bits, k is the scaling factor and it is greater than 2. The circuit is made of a synchronous n bit counter whose modulus is configurable, p DCM blocks, q = 4 × p edge triggered flip-flops, a q-to-1 multiplexer and an SR latch which gives the PWM output signal. The CLRD and SETD signals generate the set and reset signals to control the SR latch. A common clock is given to the manually placed DCMs and the counter. DCM_0 and DCM_1 are placed manually at DCM_X0Y0 and DCM_X1Y0 respectively to reduce routing delays. The quadrant phase shifted outputs CLK0, CLK90, CLK180, CLK270 from DCMs generate a set of phase shifted clocks $\{CK_i\}$ with $0 \leq i < q$, having same time period T_{CK} WITH 50% duty cycle. The fine phase shifting in fixed mode shifts the phase of DCM output signals by a fixed fraction of input clock period. The implementation is carried out in the Xilinx XC3S500E Spartan-3E FPGA. It is been described in VHDL with n = 8 and k = 3.
This approach is found to be efficient acquiring a resolution of 625 ps.

4. Comparative analysis.

The above described DPWM architectures are quite reliable with respect to the sources used to improve the resolution. This section presents the comparative study of the above mentioned architectures. The basic difference arises due the two families of FPGA used for implementation. The greatest advantage of the carry chain based approach is that almost all

the implementation is carried out without manual placement or routing. Also a high resolution is acquired with excellent linearity and monotonicity. It is basically demonstrated through a 1 MHz clock frequency and 14 bit DPWM. But in accordance with (2), the DCM resources are also used in order to match the clock period to the delay line of 2^M elements. So taking into account the frequency limit of DCM, a 178 MHz clock is experimentally tuned to well match the delay elements. Besides all these advantages there are certain parameters that must be taken into account.

Although the carry chains or the delay line is auto-placed using the FPGA programming tools, the decoding logic still require very careful manual placement and routing which increases complexity and development time. Moreover including an asynchronous circuit makes the static timing analysis harder to perform and may result in glitching due to routing and controlling of logic.

Table 1: Delay line and DCM comparison

Delay line based DPWM	*DCM based DPWM*
Implemented in Xilinx Virtex 4 FPGA	Implemented in Xilinx XC3S500E Spartan-3E FPGA
Architecture include both synchronous and asynchronous parts	Fully synchronous
Internal logic blocks used for implementation.	Implemented using a single embedded resource i.e. DCM
1 MHz clock frequency	50 MHz clock frequency (maximum 200 MHz limited for DCM)
Resolution obtained -90ps	Resolution obtained – 625ps

The second approach i.e. the DCM based DPWM is a fully synchronous architecture. A synchronous design improves the reliability of circuit and eases the design process. Besides it makes the design more independent and improves the design portability.

As compared to the delay line approach the DCM implementation is much simpler and efficient, since various logic blocks has to be used if a large bit carry chain is required. Further, even the delay line approach makes use of the DCM resource in order to improve the resolution. Although the DCM approach utilize the manual placement or routing method, the placement is made close such as a minimum routing delay is observed. The comparative analysis is summarized in table 1.

5. Conclusion

Several architectures are presented till date regarding the high resolution DPWM and each comprised of certain advantages and disadvantages. In the continuing effort to improve the results the proposed paper reviews the two recent architectures of DPWM which are implemented in two families of FPGA. It has been observed that the delay line method eases the implementation by excluding the manual placement methods, whereas the DCM provides a high resolution PWM in a simpler way being a low cost device. Hence it would be preferred to carry out a more enhanced architecture using the DCM blocks in order to achieve a high coarse resolution leading to an efficient application for digital control.

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