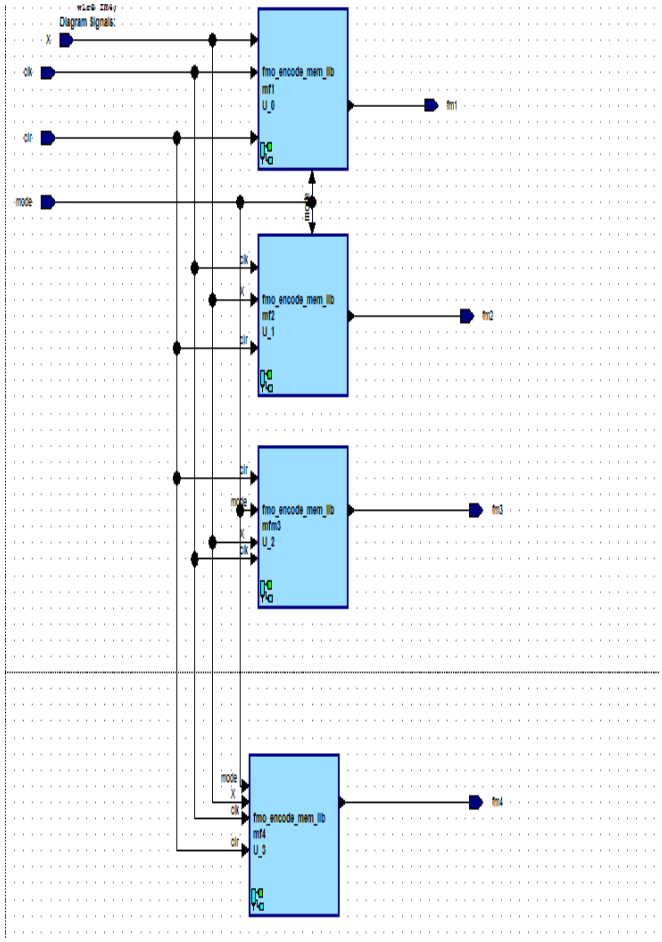

Figure 5: FM0 encoder modules

Here the 1 bit input data is encoded into the 16 bit data and sent to the memory controller block

.

2. Pseudo Random Sequence Generator: It is an algorithm for generating a sequence of numbers whose properties approximate the properties of sequences of random number. Here it generates sum random 4 bit numbers and sends it to linear feedback shift register (LFSR).

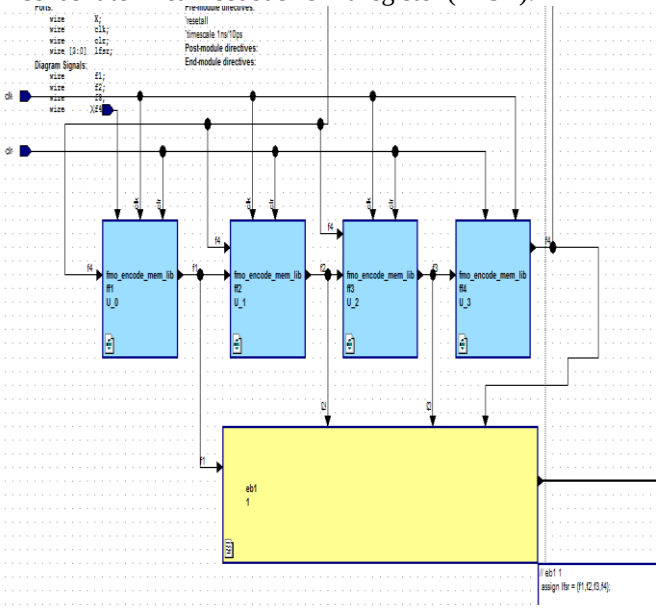

Figure 6: Block diagram of PRSG

3. Linear Feedback Shift Register (LFSR) : LFSR gives the address location where the 16 bit encoded data has to be stored in memory controller. The PRSG sends the 4 bit input i.e. nothing but the address location to the LFSR, where encoded data has to be stored.

4. Memory Controller : In memory controller , firstly the 4 bit encoded data from 4 modules of FM0 encoder are concatenated into 16 bit encoded data. This 16 bit encoded data is stored into a particular address location sent by LFSR.

5. Decoding block: Now the 16 bit encoded data stored in memory is XOR with the address location of LFSR. If the MSB bit of the XOR output is at logic 1 , then in only that condition the data will be decoded back into 1 bit, Because that is the condition we have designed for.

5. Experimental Results

Here the block diagram shown in the fig 4 is simulated using Modelsim and by giving the following data as input
X= 1, Clock = clock, Clear=1, Mode = 1, Memory input= 1010
We obtain the following results shown in below figures

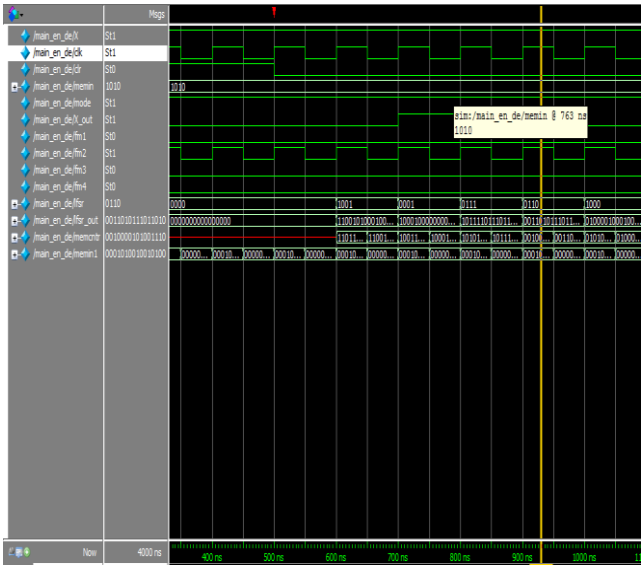

Figure 7: Experimental Results 1

Here from the above figure 7, by analysing the data
LFSR out = 0011010111011010 and
Memory input= 0001010010010100.
Now by performing the XOR operation we get the output of Memory controller = 0010000101001110.As the MSB bit of this 16 bit data is 0, the encoded data is not decoded.

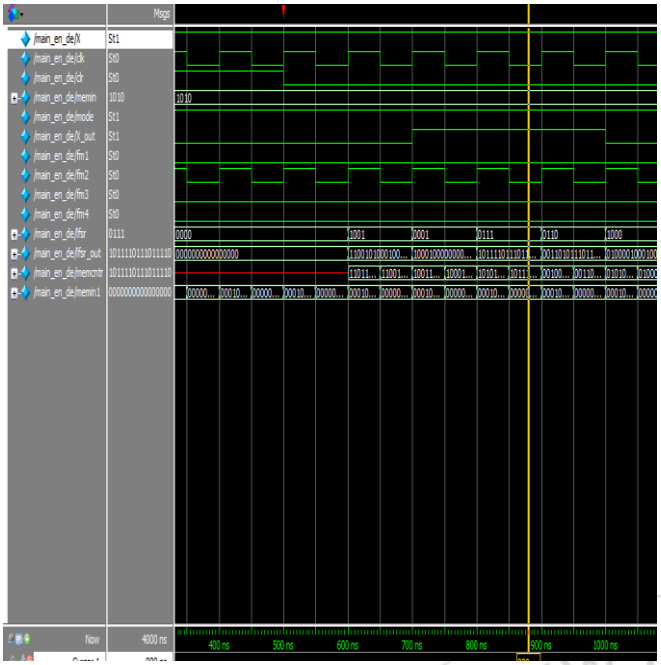

Figure 8: Experimental Results 2

Here from the above fig 8, by analysing the data

LFSR out=1011110111011110 and

Memory input= 0000000000000000.

Now by performing the XOR operation we get the output of memory controller= 1011110111011110. As here the MSB bit of this 16 bit encoded data is "1" the encoded data is decoded back into 1 bit.

6. Conclusion

The fully reused VLSI Architecture of FM0/Manchester encoder for memory applications is effective and powerful in securing the data, as compared to the other encoding techniques.FM0/Manchester encoder are easy to perform operations and faster. Hence these encoding techniques are efficient.

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Author Profile

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