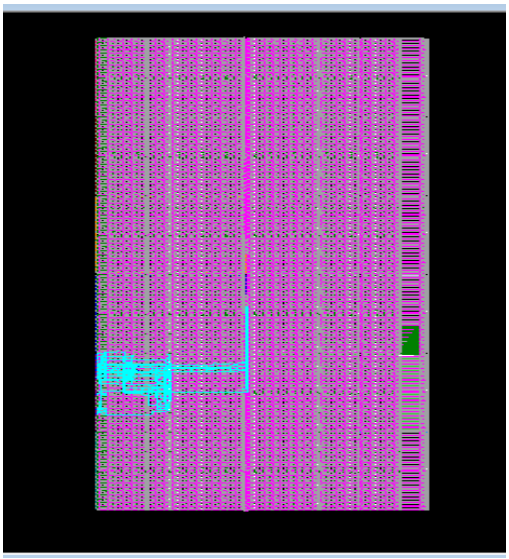

**Figure 6**: Floorplan Design View of ROM Based LUT

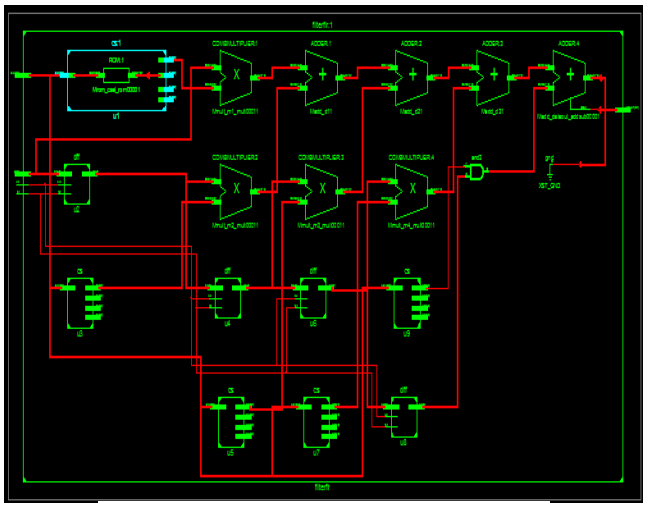

**Figure 7**: RTL View of ROM Based LUT

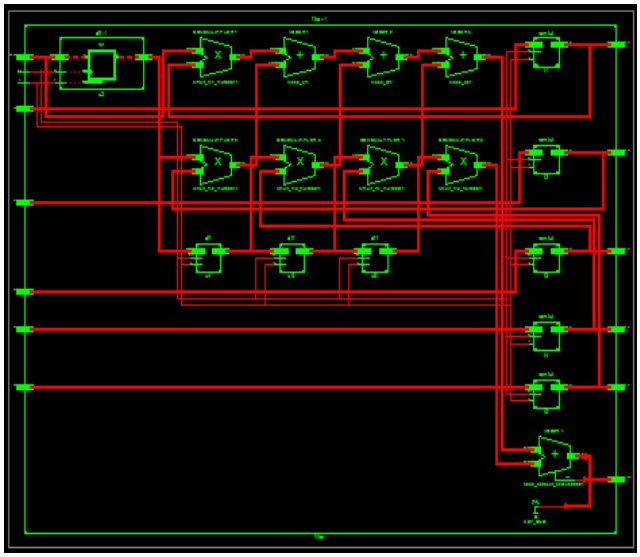

**Figure 8**: RTL view of RAM Based LUT

In figure 6 and 7 shows that the floorplan design view and RTL view of ROM based LUT. The RAM based LUT is best one compared with ROM based LUT. The RTL view and floorplan design view of RAM based LUT shown in figure 8 and 9.

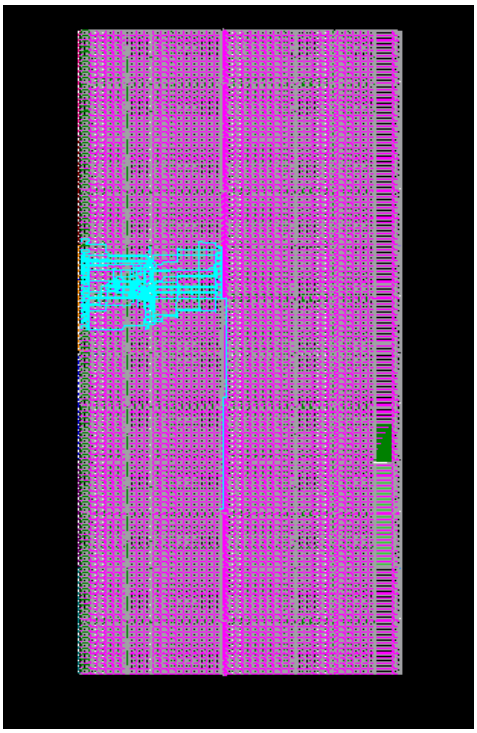

**Figure 9**: Floorplan Design View of RAM based LUT

## 5. Conclusion

Since ROM based LUT's reduces the complexity of multiplier structures, due to the linearity between coefficients and filter order, it increases the memory requirement. And also during the run time the FIR filter coefficients changing. For that we proposed the high throughput reconfigurable FIR filter using modified DA method. In reconfigurable DA based FIR filters the Look up Tables are implemented in RAM. A shared LUT design is suggested for the implementation of RAM which substantially reduces the hardware cost. Since RAM is an erasable one, it reduces the memory as well as bit slices (nearly 40%). The bit slice is a basic building block of a processor. The proposed approach supports beyond MHZ sampling rate. It is found to produce high throughput than the existing approach.

In future it can be implemented with fault toleration techniques. The idea is to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. An error-correcting code is an algorithm for expressing a sequence of numbers such that any errors which are introduced can be detected and corrected (within certain limitations) based on the remaining numbers. Hamming codes can detect up to two-bit errors or correct one-bit errors without detection of uncorrected errors.

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