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Design of Bi-directional Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code Using Single Electron Device Based Threshold Logic Gates

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Abstract: ***Single electronics, an incipient arena of swiftly rising interest has received noteworthy attention equally in academia and industry in regard to applications in modern and future electronics. Single electronics practices the 'transfer of single electron phenomena' or more conveniently the 'electron charge transport' to characterize binary data values. The intrinsic gain of the single electron devices lies in the fact that it requires considerably less amount of power than any orthodox technologies while functioning at much greater speed. We first propose the implementation of a novel switching circuit to generate odd parity bits for decimal numbers expressed in BCD code. Then after the threshold logic realization concept has been incorporated in the design spec. The unit device consists of twenty tunnel junctions and operates as an IC that can switch with every frequent single electron transport. The proposed model is a simple schematic using 'SIMON', it is a single electron circuit simulator based on a Monte Carlo technique.***

Keywords: SET, SIMON, Bi-directional Switch, Threshold Logic, BCD Code.

1. Introduction

Conventional electronics are governed by the continuous charge of the electron. The two major shortcomings of the conventional CMOS transistors are the increase in power consumption and the dwindling down in dependability. In recent times, there is a substantial progression in nanotechnology. Researchers have demonstrated the modus operandi to isolate, control and exploit the properties of a single electron empirically. Such evolutions have augmented the realization of classical logic gates; the ideology is to signify the binary bits by the presence or absence of a single electron or a few numbers of electrons. Thus Single electronics is an auspicious future electronics that reveals new physical effect of charge transport. It carnivals plentiful rewards over existing bulk semiconductor devices. Single Electron Tunneling technology offers a leeway of achieving ultra-high functional density and extremely low power dissipation equated to conventional CMOS technology. This tunneling based device is low powered and is blessed with having high potential for size reduction compared with silicon based CMOS technology. Single electron technology (SET) is distinguished by its less than 30 nm feature device size, enormously fast and high interaction and substantially low power dissipation. Moreover, SET made devices or SEDs pageant a switching behavior that differs from conventional CMOS. The SET devices proposed for gates, adder, memory, Inverter, latching switches, analog-to-digital converter etc. have been reported in decade long reputed scientific journals [1-8]. The most admiring piece is that the switching function of most of these circuits involves merely one or a few number of electrons.

Additionally, SEDs are robust and operate using modest principle; and owing to such, their maneuver is never compromised even when device size is reduced to molecular level. Rather the size reduction enhances their performances. Such prosperities are considered 'constructive' for VLSI or ULSI designs. SEDs can toil as single switches, but also possess high functionality. Many notional researches [9-12] have been reported to consider the possibility of building SEDs made LSIs and fundamental computational capability by now have been evidenced. This is why SET devices are central rudiments in Nano-electronic meadow and its incorporation in designing the circuits such as memory [13], logic circuits [14], electron pumps [15] etc. has received greater appreciation. The authors here would like to refer to some previous research in designing different logic gates, flip-flops, addition, multiplication, division and also design of sequence generator, ALU etc. using SEDs[16-19].

The authors in persuasion of generating odd parity bits for decimal numbers do largely emphasize in using BCD code. Such circuits have categorically demonstrated greater significance in communication engineering. Thus previously it was attempted to design CMOS based hardware for such topologies. With modernization in device research, present day Researchers accentuate SET technology as a replacement of CMOS technology in assembling such designs. This has motivated the authors to take up the challenge of designing advanced bi-directional switching circuit to generate odd parity bits for decimal numbers expressed in BCD code.

In this letter, the authors concisely talk over the basic physics of Single Electron Devices in section 2 and review the Basic Simulation of NOT Gate in Section 3. The Section 4 discourse an advanced bi-directional switching circuit to generate odd parity bits for decimal numbers expressed in BCD code, which is further implemented using SET device

based Threshold Logic Gates. Analysis of the proposed model is deliberated in this section.

2. The Basic Physics of Single Electron Device

SET expertise on tunneling of electrons where tunnel junctions embrace an ultra-thin insulating layer in a conducting material [20]. Customarily, electron flow is clogged through an insulator. But then again, electron transport or tunneling of charge is feasible meticulously with one electron at a time provided that the tunneling layer is thin enough. The datum is that the SET technology render the facility to control the motion of individual electrons in the small vicinity [6, 21]. Eventually the electrons are considered to tunnel through a tunnel junction in sequence [22]. An individual electron tunneling is likely to yield a charge e/C across the tunnel junction (where C is total capacitance and e = 1.602 x 10^{-19} C). The critical voltage $\mathbf{V}_c$ derived at the tunnel junction is given by

$$V_c = \frac{e}{2(C_e + C_j)} \quad (1)$$

Where C_j denominates the junction capacitance and C_e is the corresponding capacitance for residue circuit. The voltage through the tunnel junction is V_j and the critical voltage at the tunnel junction is V_c which is prerequisite for threshold voltage. Tunnel event occurs by the side of the tunnel junction if and only if $|V_j| \geq V_c$; or else the tunnel event is ceased to exist. The circuit stabilizes if $|V_j| < V_c$.

The SET technology instigated here is based on the mechanism of the threshold logic gate (TLG). TLGs are endowed to reckon several linear discrete Boolean functions, thus it is quite potent than conventional Boolean logic gates. It calculates a function given by

$$Y = \text{sgn}\{F(x)\} = \begin{cases} 0 & \text{if } F(x) < 0 \\ 1 & \text{if } F(x) \geq 0 \end{cases} \quad (2)$$

$$F(x) = \sum_{i=1}^{n} \omega_i x_i - \psi \quad (3)$$

Considering x_i as the n no inputs and ω_i as the analogous n no integer weights the TLG execute a comparison amongst the weighted sum of inputs $\sum_{i=1}^{n} w_i x_i$ and the threshold value ψ. Then after if the resulted sum is higher than threshold, the TLG output will be logic 1, otherwise output will be logic 0.

Symbol and structure of TLG is shown in figure 1(a) and 1(b). As revealed that the electron tunneling is stochastic in nature. Furthermore, the switching delay (t_d) for each transported electron is determined by

$$t_d = \frac{-\ln(P_{error}) R_t}{|V_j| - V_c} \quad (4)$$

Here R_t represents the junction's resistance, whereas the P_{error} is the probability defining that the desired charge transport has not occurred after t_d seconds [20].

3. The Single Electron NOT Gate

The SET based NOT gate [26] as depicted in fig. 3 comprises of three islands N_1 – N_3 circumscribed by four tunnel junctions J_1 - J_4 and five capacitors C_1 – C_5. The tunnel junctions J_1 and J_4 are indistinguishable. The junction's resistance and capacitance is 10^5 Ω and 0.1 aF respectively in the SIMON designed NOT gate. The resistances of tunnel junctions J_2 and J_3 are kept 10^5 Ω and capacitance is 0.5 aF respectively. The input voltage is mobilized through the capacitor C_1 and C_2 and its value are limited to 0.5 aF. The constant voltage V_b is 16mV. The simulation results of NOT gate using SIMON 2.0 is depicted in Fig.4; it illustrations the time variation of input voltages and in Fig. 5 the time deviation of the charge at the output node N2 is confirmed. As manifested, the charge at N2 is positive if the input is zero only. Both the waveforms characterizes the NOT gate. 0.0V was given at the input to perform the logic '0' and 16 mV was fetched for logic '1'.

4. Proposed Model of Bi-directional Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code Using Single Electron Device Based Threshold Logic Gates

SIMON based design has been depicted in Fig.6. The circuit consists of twenty Tunnel Junctions. The parity bit is likely to be the fifth bit to the 4-bit word. As evident that the parity bits are to be generated, as soon as the BCD number corresponds to decimal numbers 1, 2, 4, 7, 8. Among others some state of parity bits for prohibited combinations of variables has to be treated as don't care conditions. One can take up any of the two possible values of '1' or '0'. For simplification K-map was constructed for 'P-odds' along with the don't care conditions. The P odd as derived from K-map can be rewritten as:

$$\begin{aligned} P_{odd} &= \overline{A}.\overline{C}(B.D) + A.\overline{C}(B \oplus D) \\ &\quad + \overline{A}.C(B \oplus D) + A.C(B.D) \\ &= (A \oplus C).(B + D \end{aligned} \quad (5)$$

The same is reused to obtain 'P-even'

$$P_{even} = A \oplus B \oplus C \oplus D \quad (6)$$

5. Conclusion

This paper reconnoitered the employment of Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code based on single electron encoded logic gates. The circuit eventually operates with the transportation of single electron. Simulation is accomplished using SIMON 2.0. For easement and robustness a step-wise procedure was followed. Entire simulation runs on Monte-Carlo equation. The output resembles high speed because of the internal structure. Thus it shows substantial acceptance in near future.

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Author Profile

Dr. Jayanta Gope, PhD (Engg.), & Chartered Engineer has received his PhD Degree in Nanotechnology from Jadavpur University, Kolkata and is presently associated with Camellia School of Engineering and Technology. His field of interest includes Nano device modeling, Single Electronic devices, Spintronic Devices, Hybrid CMOS-SET. He has already published around 40 International research articles in this category. He is nominated as Editorial Board Member and Reviewer of some esteemed Journals and is guiding 4 PhD Scholars in the field of Nanotechnology. He is a life Member of 'CE'& 'ISCA'.

Mr. Krishnendu Saha is a final year student of B.Tech in Electrical and Electronics Engineering Department of Camellia School of Engineering and Technology, West Bengal, India.

List of Figures

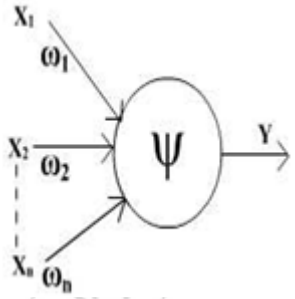

Figure 1: (a) TLG symbol

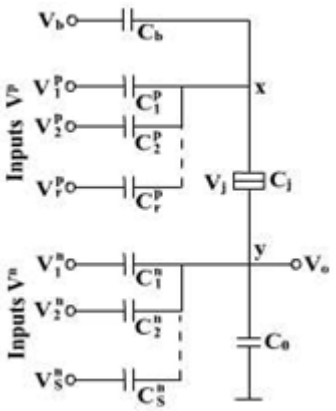

Figure 2: TLG structure.

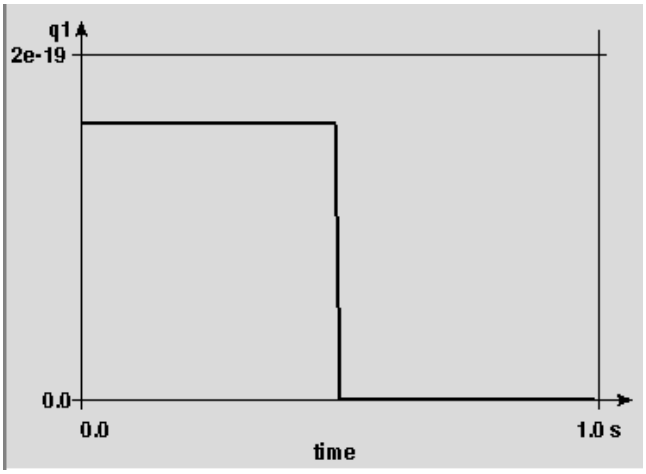

Figure 3: SET based NOT gate circuit

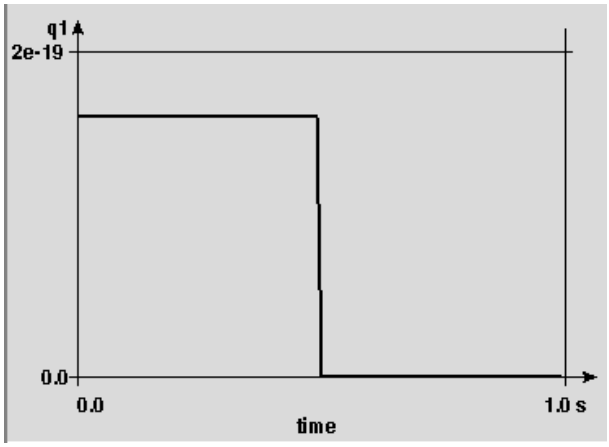

Figure 5: SET based NOT gate output.

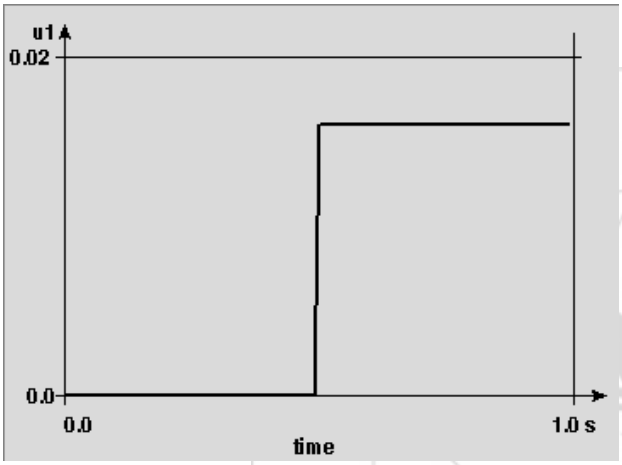

Figure 4: SET based NOT gate input.

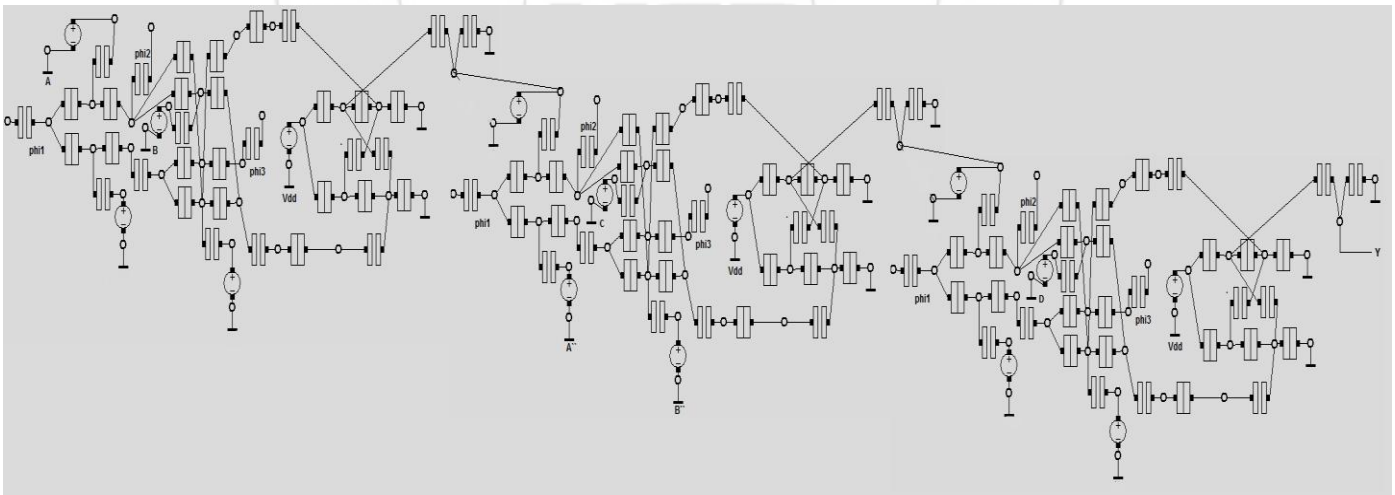

Figure 6: Proposed Model of Bi-directional Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code Using Single Electron Device Based Threshold Logic Gates.