

based Threshold Logic Gates. Analysis of the proposed model is deliberated in this section.

2. The Basic Physics of Single Electron Device

SET expertise on tunneling of electrons where tunnel junctions embrace an ultra-thin insulating layer in a conducting material [20]. Customarily, electron flow is clogged through an insulator. But then again, electron transport or tunneling of charge is feasible meticulously with one electron at a time provided that the tunneling layer is thin enough. The datum is that the SET technology render the facility to control the motion of individual electrons in the small vicinity [6, 21]. Eventually the electrons are considered to tunnel through a tunnel junction in sequence [22]. An individual electron tunneling is likely to yield a charge e/C across the tunnel junction (where C is total capacitance and $e = 1.602 \times 10^{-19}$ C). The critical voltage V_c derived at the tunnel junction is given by

$$V_c = \frac{e}{2(C_e + C_j)} \quad (1)$$

Where C_j denominates the junction capacitance and C_e is the corresponding capacitance for residue circuit. The voltage through the tunnel junction is V_j and the critical voltage at the tunnel junction is V_c which is prerequisite for threshold voltage. Tunnel event occurs by the side of the tunnel junction if and only if $|V_j| \geq V_c$; or else the tunnel event is ceased to exist. The circuit stabilizes if $|V_j| < V_c$.

The SET technology instigated here is based on the mechanism of the threshold logic gate (TLG). TLGs are endowed to reckon several linear discrete Boolean functions, thus it is quite potent than conventional Boolean logic gates. It calculates a function given by

$$Y = \text{sgn}\{F(x)\} = \begin{cases} 0 & \text{if } F(x) < 0 \\ 1 & \text{if } F(x) \geq 0 \end{cases} \quad (2)$$

$$F(x) = \sum_{i=1}^n \omega_i x_i - \psi \quad (3)$$

Considering x_i as the n no inputs and ω_i as the analogous n no integer weights the TLG execute a comparison amongst the weighted sum of inputs $\sum_{i=1}^n \omega_i x_i$ and the threshold value ψ .

Then after if the resulted sum is higher than threshold, the TLG output will be logic 1, otherwise output will be logic 0.

Symbol and structure of TLG is shown in figure 1(a) and 1(b). As revealed that the electron tunneling is stochastic in nature. Furthermore, the switching delay (t_d) for each transported electron is determined by

$$t_d = \frac{-\ln(P_{error})R_t}{|V_j| - V_c} \quad (4)$$

Here R_t represents the junction's resistance, whereas the P_{error} is the probability defining that the desired charge transport has not occurred after t_d seconds [20].

3. The Single Electron NOT Gate

The SET based NOT gate [26] as depicted in fig. 3 comprises of three islands $N_1 - N_3$ circumscribed by four

tunnel junctions $J_1 - J_4$ and five capacitors $C_1 - C_5$. The tunnel junctions J_1 and J_4 are indistinguishable. The junction's resistance and capacitance is $10^5 \Omega$ and 0.1 aF respectively in the SIMON designed NOT gate. The resistances of tunnel junctions J_2 and J_3 are kept $10^5 \Omega$ and capacitance is 0.5 aF respectively. The input voltage is mobilized through the capacitor C_1 and C_2 and its value are limited to 0.5 aF . The constant voltage V_b is 16 mV . The simulation results of NOT gate using SIMON 2.0 is depicted in Fig.4; it illustrates the time variation of input voltages and in Fig. 5 the time deviation of the charge at the output node N_2 is confirmed. As manifested, the charge at N_2 is positive if the input is zero only. Both the waveforms characterizes the NOT gate. 0.0 V was given at the input to perform the logic '0' and 16 mV was fetched for logic '1'.

4. Proposed Model of Bi-directional Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code Using Single Electron Device Based Threshold Logic Gates

SIMON based design has been depicted in Fig.6. The circuit consists of twenty Tunnel Junctions. The parity bit is likely to be the fifth bit to the 4-bit word. As evident that the parity bits are to be generated, as soon as the BCD number corresponds to decimal numbers 1, 2, 4, 7, 8. Among others some state of parity bits for prohibited combinations of variables has to be treated as don't care conditions. One can take up any of the two possible values of '1' or '0'. For simplification K-map was constructed for 'P-odds' along with the don't care conditions. The P odd as derived from K-map can be rewritten as:

$$\begin{aligned} P_{\text{odd}} &= \bar{A}.\bar{C}(B.D) + A.\bar{C}(B \oplus D) \\ &+ \bar{A}.C(B \oplus D) + A.C(B.D) \\ &= (A \oplus C).(B + D) \end{aligned} \quad (5)$$

The same is reused to obtain 'P-even'

$$P_{\text{even}} = A \oplus B \oplus C \oplus D \quad (6)$$

5. Conclusion

This paper reconnoitered the employment of Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code based on single electron encoded logic gates. The circuit eventually operates with the transportation of single electron. Simulation is accomplished using SIMON 2.0. For easement and robustness a step-wise procedure was followed. Entire simulation runs on Monte-Carlo equation. The output resembles high speed because of the internal structure. Thus it shows substantial acceptance in near future.

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Author Profile



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List of Figures

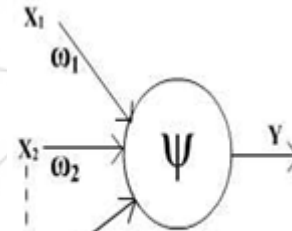


Figure 1: (a) TLG symbol

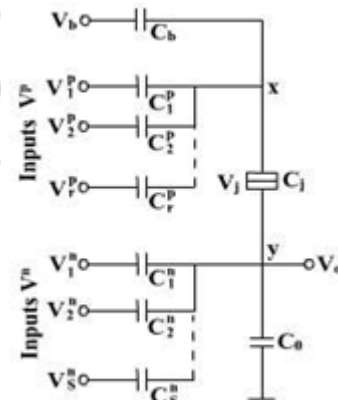


Figure 2: TLG structure.

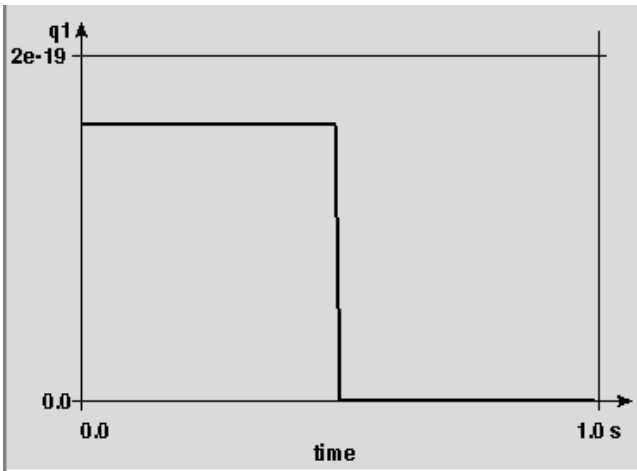


Figure 3: SET based NOT gate circuit

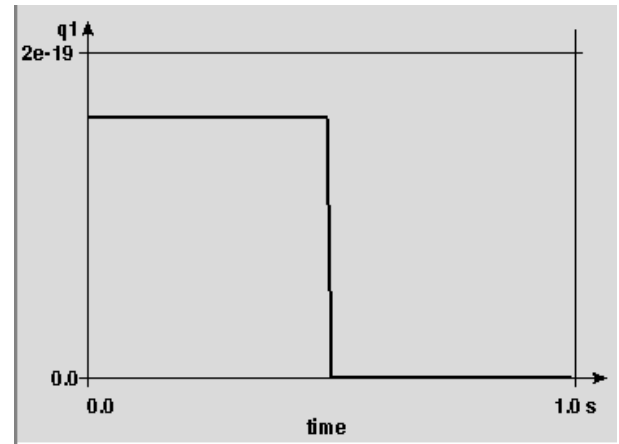


Figure 5: SET based NOT gate output.

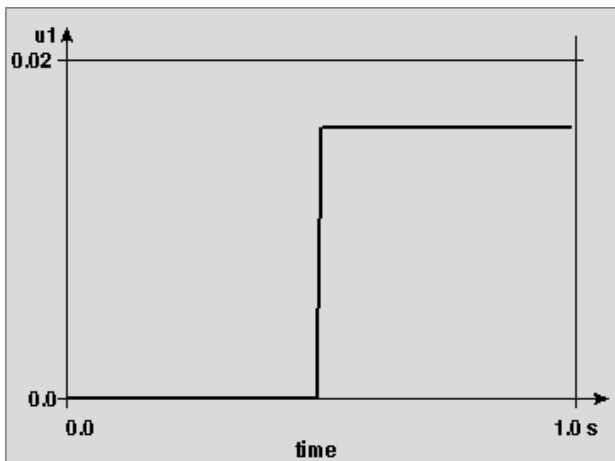


Figure 4: SET based NOT gate input.

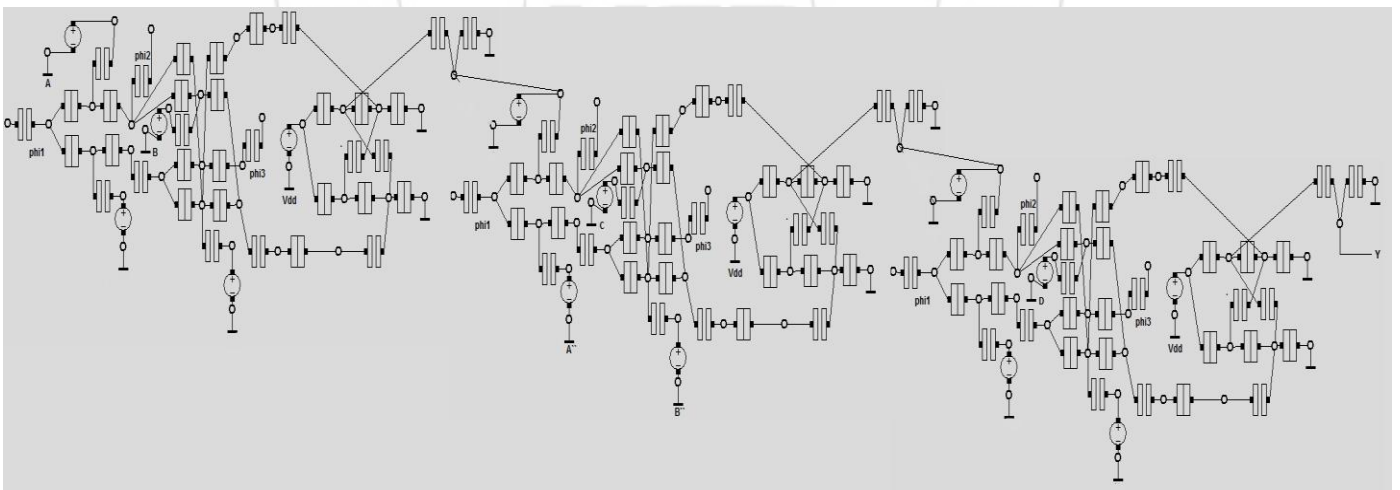


Figure 6: Proposed Model of Bi-directional Switching Circuit to Generate Odd Parity Bits for Decimal Numbers Expressed in BCD Code Using Single Electron Device Based Threshold Logic Gates.