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Comparative Study on Logic Gates Using Bulk Transmission Gate and Double Gate Transmission Gate

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Abstract: ***In VLSI technology, field effect transistors are promising candidate to extend moor's law in coming years its stated that the number of die or the number of chip will be double in every 18 month. Recently double gate MOSFET has been demonstrated to allow better performance in means of power and delay as power and performance have become the predominant concern for chip designer. In this paper, we are represent the study on logic gates using bulk transmission gate and double gate transmission gate and compare the results in between the two in the form of power i.e leakage power, static power and dynamic power in 45nm technology. So we characterized and validate arithmetic logic gates that are AND gate, XOR gate using the platform cadence virtuoso in 45 nm technology. And the experimental results show that using double gate transmission gate we get the better performance that means low leakage power dissipation.***

Keywords: Transmission Gate, Double gate MOSFET, Bulk transmission gate, Double Gate Transmission gate**.**

1. Introduction

Arithmetic logic is the most basic building block in today's integrated circuits. The logic gates are the basic data path that forms the reasoning core of the logic applications in silicon. In 1990 the majority worry of the chip designers in the area constraint that is optimization of design to reduce chip area. However the continuous scaling of the device to minimize the feature size and advancement in computer aided design tools, area constraint has faded away, tens of millions of transistor can be fabricated in a single chip so the worry of today's chip designer is power that is low power consumption. It is become the predominant concern now days. The power dissipation in a CMOS semiconductor device is classified as static and dynamic .the static power dissipation is due to the reverse saturation, sub threshold and leakage current and occurs especially when the device is in idle mode. The dynamic power dissipation occurs due to the charging and discharging of load capacitance when both the nMOS and pMOS device remain on for short time duration. So the most required feature of modern electronics low power energy efficient building block that enables the implementation of the long lasting battery operated systems. So in this paper a comparative study on logic gate is done by using transmission gate considering both BULK MOSFET and Double gate MOSFET, so transmission gate is defined as electronic element that will selectively block or pass a signal level from the input to output. This solid state switch is compared with a pMOS and nMOS transistor. When using double gate nMOS nd double gate pMOS transistor then performance is better in the form of low power dissipation. The control gates are complementary manner so that both transistors are either on or off.

2. Relation to Prior Work

Previous work describes the speed of the design is limited by size of the transistor, delay and parasitic capacitance in the critical path. Power consumption and speed are two important aspects. Hence a better metric to evaluate circuit performance is power delay product. The driving capability of a full adder is very important because full adder is mostly used in cascade configuration [1]. Now a day's power consumption is the major concern in VLSI circuit design technology. High power consumption leads to a reduction in battery life in the case of battery powered application and affects the reliability of the system [2]. With the continuous scaling down of the MOSFET devices, the voltage which can applied to the gate must be reduced to maintain reliability, threshold voltage of the MOSFET has to be reduced when the gate oxide thickness reduces to 1.20nm or less than that, the electron tunneling occur between the channel and the gate due to high electric field. So power consumption goes high because of increase in sub threshold leakage current [3]. Gate diffusion is a novel technique for low power design in VLSI digital circuits; this technique reduces the power dissipation, propagation delay, area of the digital circuits and it maintains low complexity of the logic design by using pass transistor, transmission gate and gate diffusion input [4]. The adder is the most commonly used building block in central processing unit (CPU) and digital signal processing (DSP). So its performance and power optimization is an important issue. In realizing very large scale integration (VLSI) circuits, low power and high speed are the two predominant factors which need to be considered. So previous works shown the three diff rent types of $-bit transmission based gate based adders namely ripple carry adder, carry select adder and carry look ahead adder and compare the different adder on the basis of no of transistors, the average power consumption and delay [5]. The most required features of the modern VLSI technology is low power energy efficiency building block that enables the implementation of the long lasting battery

operated systems. There are no single types of 1 bit adder which can be use for this type of application, so different types of logic styles are used for designing a full adder cell to cover a wide range of performance characteristics to satisfy this application [6]. In digital electronics system, it is crucial to have a full adder that is low in power dissipation, high speed, energy efficient and reliable. Compare to bulk MOSFET technology the new FINFET technology can be implemented in 1 bit full adder to prolong silicon downscaling and enhanced the device performance and energy efficiency for the full adder design [7].

3. Basic structure of transmission gate using BULK MOSFET and DG MOSFET

When the voltage on node A is logic 1, the complementary logic 0 is applied to node active low A, allowing both transistor to conduct and pass the signals at INPUT to OUTPUT. When the voltage on node active low A is a logic 0. The complementary logic 1 is applied to node A, turning both transistors off and force a high performance condition on both the INPUT and OUTPUT nodes.

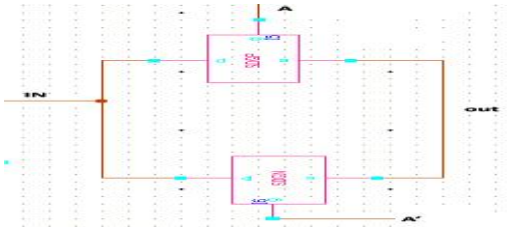

Figure 1: Structure of transmission gate using DG MOSFET

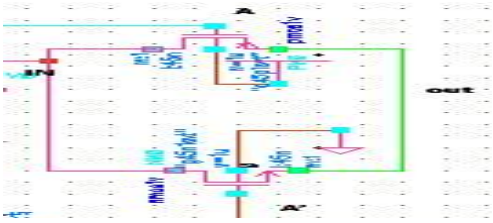

Figure 2: Structure of transmission gate using bulk MOSFET

4. Circuit Analysis

4.1 AND Gate circuit using BULK transmission gate

In fig 3 shows the AND gate using bulk transmission gate. Here a transmission gate made up of two field effect transistor in which in contrast to traditional discrete field effect transistors the substrate terminal (BULK) is not connected internally to the source terminal. The two transistor n channel MOSFET and p channel MOSFET are connected in parallel with this. The gate terminal is connected together via INVERTER to form the control gate. since a transmission gate must block the flow in either direction the substrate terminals are connected to the respective supply voltage potential in order to ensure that a the substrate diode is always operated in the reverse direction. The substrate terminal of the n channel MOSFET is thus connected to the p channel MOSFET to the positive supply voltage potential and the substrate terminal of the n channel MOSFET connected to the negative supply voltage potential.

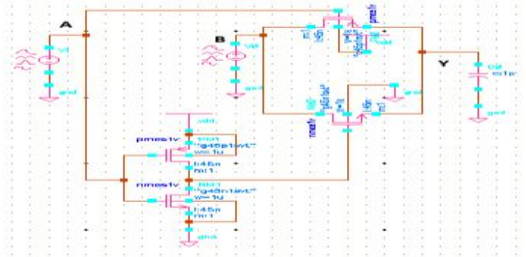

Figure 3: AND gate using BULK transmission gate

So from the truth table we can notice that when one input is at logic high (A=1) then the output(Y) is following the input (B). So it act as a buffer.

Table 1: Truth table of AND gate

Input (A)	Input (B)	Output(y)
0	0	0
0	1	0
1	0	0
1	1	1

4.1.1Waveform

In fig: 4 we can see that the output is not exactly follow the logic high and logic low because of the leakage power. The leakage or static power dissipation is the power dissipated by the circuit when it is in the standby mode and is then

$P_{leakage} = I_{leakage} \times V_{DD}$

So when the input A at logic high then both the MOSFET is off condition. So it is in the standby mode .so in this condition the leakage current is flow. So leakage power is more in this circuit because leakage current is high when using bulk transmission gate. And dynamic power is consumed when transistors are switching. The dynamic power is also high in this condition. As the technology is continuously scaled down a significance portion of the total power consumption is high performance digital circuits are due to leakage current because of reduced threshold voltage and device geometry. Therefore leakage power reduction is the key to a low power design.

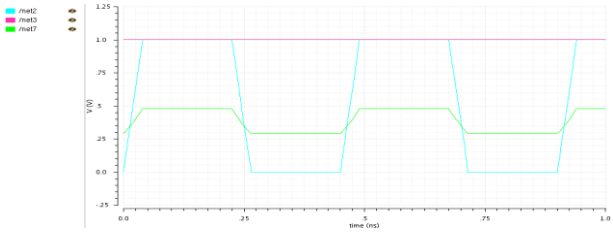

Figure 4: Wave form of the AND gate using BULK transmission gate

4.1.2Leakage power graph

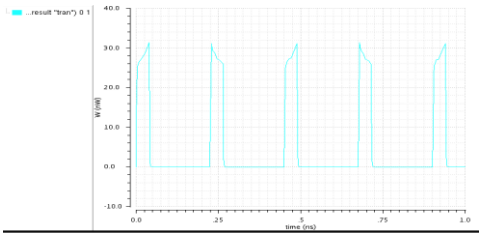

Figure 5: leakage Power of the AND gate using bulk transmission gate

4.1.3Dynamic Power graph

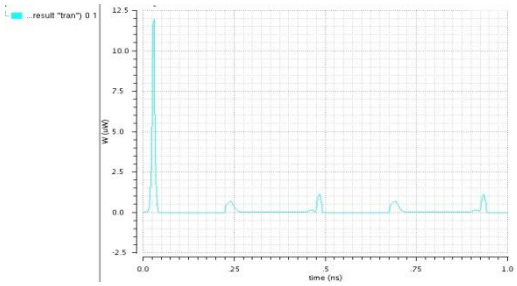

Figure 6: Dynamic power of the AND gate using bulk transmission gate

4.1.4Leakage current graph

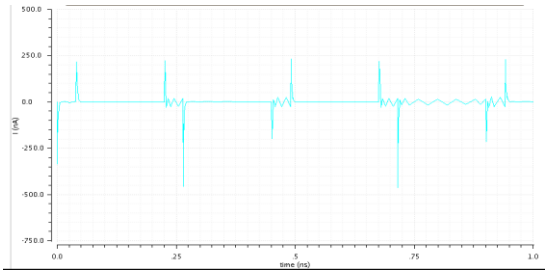

Figure 7: Leakage current of AND gate using bulk transmission gate

4.1.5Dynamic current graph

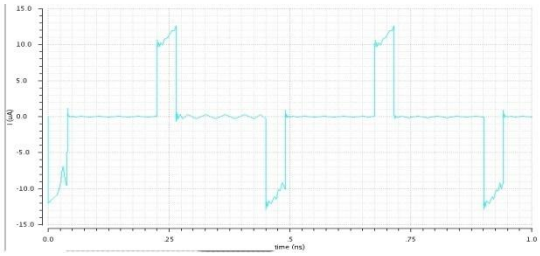

Figure 8: Dynamic current of and gate using bulk transmission gate

4.2 Circuit diagram of DG transmission gate

DG-MOSFET is that when the top and bottom gates are biased simultaneously to establish the equal substrate potentials: that is V_{G1}=V_{G2} for identical gate oxide that means V_{G1}=V_{G2} (t_{ox2}/t_{ox1}) to compensate for the difference in front and back oxide thickness. In fully depleted transistors with thin enough film, controlled the channel from the both sides and forces most of the carriers to flow in the middle of the film. In fig 9 shows the AND gate using double gate transmission gate .so its performance is much then the conventional transmission gate. Using double gate transmission gates the leakage current and dynamic current has reduced with a great extent. So it has better performance.

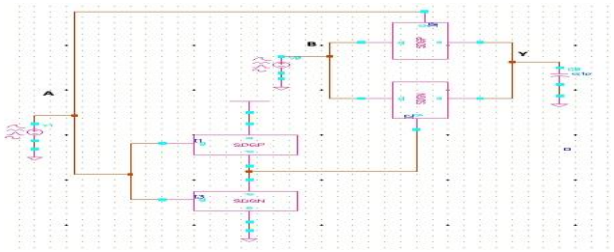

Figure 9: Circuit diagram of AND gate using double gate transmission gate

4.2.1Waveform

Fig 10 shows that it is exactly follow the logic "1" and logic "0". Because it has reduced leakage power .using double gate transmission gate the leakage current is reduced and one time leakage power is become zero.

$P_{leakage}$ =$I_{leakage}$× V_{DD}

As $I_{leakage}$ is reduced then the power is also reduced when supply voltage is 1v. That's why it became a better choice in deep submicron technology.

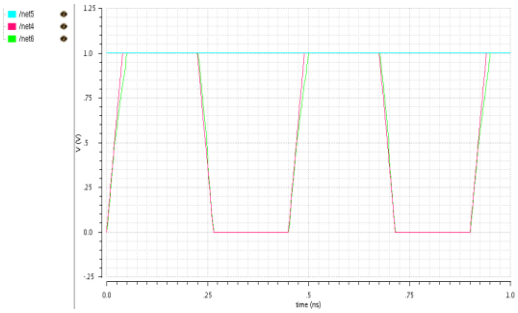

Figure 10: Wave form of the AND gate using Double gate transmission gate

4.2.2Leakage Power graph

In fig 11 shows that when one input is "1'' then the output is exactly following the input and in this steady state condition leakage power flowing. Here the leakage power is zero. So it has a better performance.

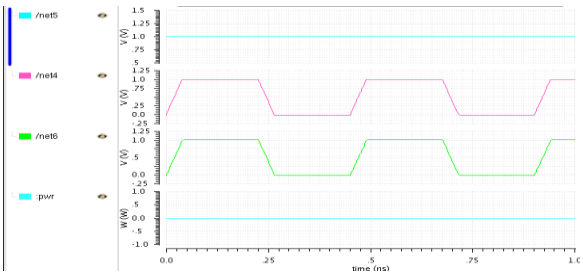

Figure 11: leakage power in double gate transmission gate

4.2.3Dynamic power graph

In fig: 12 when one input is transition from 0 to 1 and 1 to 0, that time the dynamic power is occur. And this is 0 for the double gate transmission AND gate.

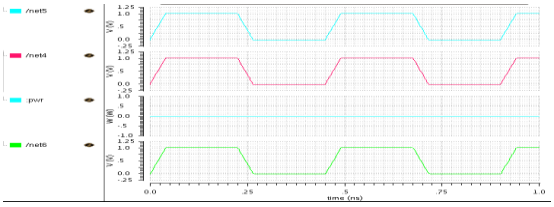

Figure 12: Dynamic power dissipation of AND gate using double gate MOSFET

4.2.4Leakage current graph

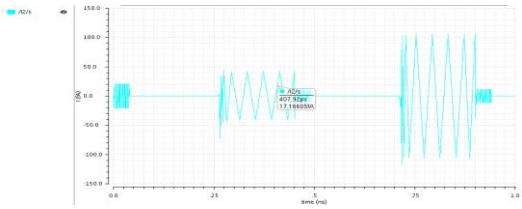

Figure 13: leakage current in AND gate using DG MOSFET

4.3 Comparison of power

Leakage may refer to a gradual loss of energy from a charged capacitor. It is caused by electronic devices attached to the capacitors, like transistors or diodes, which conducts small amount of current even when the transistors are turned off. Even though this off current still slowly is an order of magnitude less than the current through the device when it is switched on, the current still slowly discharges the capacitor. Another contributor to leakage is from a capacitor which form the undesired imperfection of some dielectric materials used in capacitor also known as dielectric leakage. The power is depends on the leakage current and supply voltage. So when leakage current is reduced then leakage power is also reduced. So here compare the leakage and dynamic power of the AND gate.

Table 2: comparison study of AND gate using double gate and bulk transmission gate

Power	AND gate using Double gate Transmission gate	AND gate using BULK transmission gate
Leakage power	0	5.431×10^{-9}
Dynamic power	0	185×10^{-9}
Leakage current	205×10^{-33}	517×10^{-9}
Dynamic current	2.88×10^{30}	402×10^{-9}

4.4 Circuit diagram of XOR using bulk transmission gate

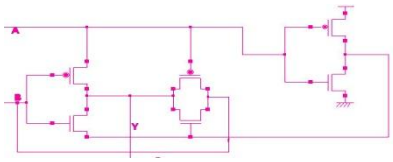

Figure 14: XOR gate using BULK transmission gate

4.4.1Waveform

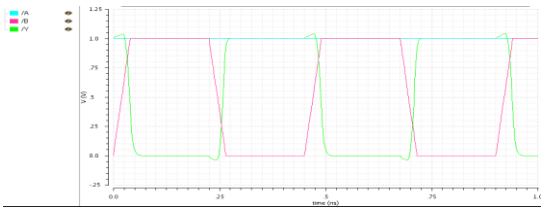

Figure 15: Wave form of the XOR gate using BULK transmission gate

4.5 Circuit diagram of XOR using Double gate transmission gate

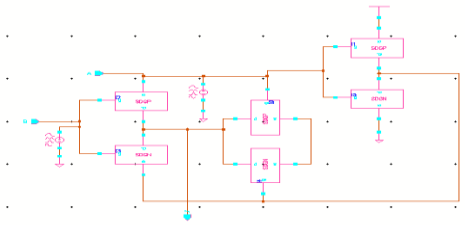

Figure 16: XOR gate using double gate transmission gate

4.5.1Waveform

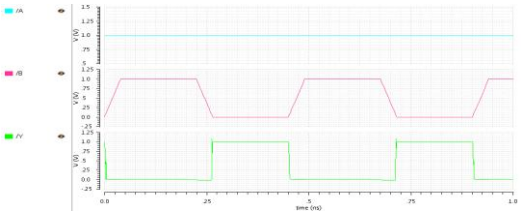

Figure 17: Wave form of the XOR gate using Double gate transmission gate

4.6 Leakage and dynamic power comparison

Table 3: Comparison study of XOR gate using double gate and bulk transmission gate

Power	XOR gate using double gate transmission gate	XOR gate using bulk transmission gate
Leakage power	18.25×10^{-33}	493×10^{-9}
Dynamic power	203×10^{-30}	121.9×10^{-9}
Leakage current	18.25×10^{-33}	493×10^{-9}
Dynamic current	203×10^{-30}	121.9×10^{-9}

5. Conclusion

Low power design is the most required nowadays to continuous scaling down the technology where the minimizing the voltage level is most effective way to minimizing power consumption. The leakage current and leakage power of logic gates using double gate transmission gate and the bulk transmission gate have been studied and the analytical result shows that the AND gate and XOR gate using double gate MOSFET gives low power and low leakage current than the AND gate using bulk transmission gate. So logic gates using double gate transmission gate exhibits high performance to design low leakage logic circuits

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