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12Bit, 80MHz, 230mW Pipeline ADC using 3Bit Flash ADC

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Abstract: ***This work describes a 12-bit multibit-per-stage pipeline analog-to-digital converter (ADC) by using 3bit flash type ADC. Pipeline ADCs are the architecture of choice for ADCs used in such wireless communication systems. The Supply voltage for this Pipelined ADC is ±3.3V for 0.18µm Technology. The Characterization of Pipelined ADC is done in terms of SNDR, ENOB, INL, DNL, Power dissipation. The Simulation Result shows that the Sampling Rate is 80MS/s with power Dissipation of 230mW was achieved in 0.18µm technology. The measured SNDR is 62.21dB, ENOB is 10.041bit, DNL is 0.2049LSB and INL is 0.4067LSB 0.18µm Technology.***

Keywords: Analog to Digital (ADC), Flash ADC, Digital Correction Block, Pipeline**.**

1. Introduction

Analog-to-digital converters (ADCs) are very important building blocks in modern signal processing and communication systems. Many good ADC architectures have been invented to satisfy different requirements in different applications. To name some: flash ADC, two-step ADC, pipeline ADC, successive-approximation-register (SAR) ADC, delta-sigma ADC, integrating ADC etc. Among various ADC architectures, the pipelined ADC has the attractive feature of maintaining high accuracy at high conversion rate with low complexity and power consumption. The goal of this project is to build a Pipeline ADC architecture, which generates 3-bits per stage, with sampling frequency as high as 100+MHz**.** Successive Approximation Register based ADC still holds that section of applications which requires lower sampling rates and applications requiring sampling rates (a few hundred MS/s or higher) are still obtained using flash ADCs. Nonetheless, pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power consumption in recent years. Gigabit Ethernet and code conversion for flat panel displays [6] are few applications that require sampling rate of about 100MS/s or above. For such application it is very crucial to reduce power consumption along with maintaining high speed of operation [1]. Figure 1 shows basic building blocks used in an 12-Pipeline ADC. It consists of 5 identical stages producing 3 bits output, followed by a final high resolution 3-bit flash ADC. This stages in total produces 18 bits output which is feed to the Time Alignment and Digital correction block, which in turn produces final 12-bit digital data.

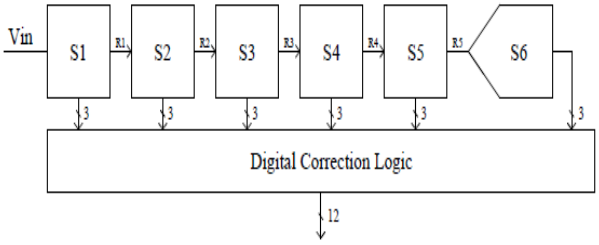

Figure 1: Block diagram of 12-bit pipeline ADC

A survey present A/D converter research reveals that a majority of effort has been directed to four different types of architectures [2], [4]:
a) Flash-type / Parallel ADC,
b) Successive approximation ADC
c) Oversampled / Sigma-Delta ADC
d) Pipeline ADCs

Each has its own benefits and span the spectrum of high speed and resolution. Flash ADCs are the fastest of all but uses series of comparators (OPAMP). An n-bit flash ADC, uses 2^n comparators and hence as no of bits increases, hardware needed for flash ADC increases and hence becomes difficult to use flash ADCs for higher no. of bits.

On the other end, Sigma-Delta ADCs uses oversampling technique to achieve higher resolution but are relatively slower because of the same reason of oversampling the input signal. SAR based ADCs are best suited for higher resolution applications but has tradeoff with accuracy of the data produced by it.
An pipeline ADC combines the advantages of all above mentioned ADCs to produce a higher resolution output with good conversion speed and accuracy. Divide and Rule is the concept behind Pipeline ADC architecture.

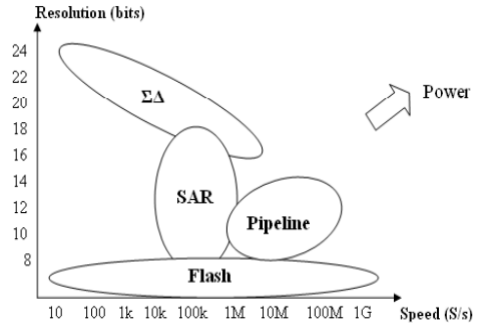

Figure 2: Comparison graph of various ADCs

2. Architecture of 12-BIT Pipeline ADC

The ADC incorporates 6 stages; each one (except for stage 6) consists of a sample and hold, DAC, subtraction and amplification circuitry (all of which known as multiplying DAC or MDAC) and a low resolution but high speed flash ADC. Stage 6 is a 3-bit flash ADC. Inside each stage input voltage is converted to 3 raw bits by the high speed flash ADC and then reconstructed back to analogue by the DAC. The reconstructed signal is subtracted from original sampled signal and the difference is multiplied by the amplification factor, producing the residue signal. The residue signal is applied to the next stage to be processed and the current stage starts sampling the incoming signal and processing on the sampled and held data. The pipelining operation produces latency to the digital data production but after that there will be one conversion per clock cycle. So the result of this concurrency conversion rate of the ADC is independent of the number of stages.

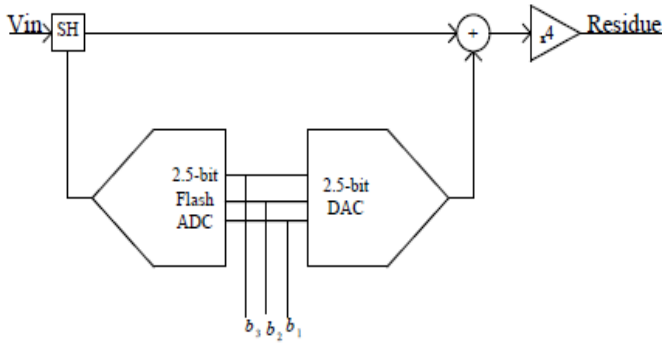

Figure 3: 1st Pipeline Stage

3. Implementation of the 12-BIT Pipeline ADC

3.1 12- Bit Single Stage of Pipelined architecture

In Pipeline ADC each stage is divided into two main parts. The first is the gain-stage. The gain-stage contains the operational trans-conductance amplifier (OTA) and the sample and hold (S/H) block. The second part is the combination of a sub-ADC and the sub-DAC. Both sub-ADC and sub-DAC are low-resolution A/D and D/A converters respectively. An analog signal input to a stage is given onto the S/H circuitry at the front end. The analog signal is sent to the sub-ADC and gain-stage simultaneously. The sample is then converted into a digital word by the sub- ADC. The sub-DAC then converts this digital word into an analog signal. This analog signal is subtracted from the initial sample creating a residue. This residue is sent to the following stage and the process is repeated. Each stage provides a 3 bit digital word which is sent to the digital correction block.

Each single stage consists of following sub modules:
A) Sample and Hold.
B) 3 bit ADC
C) Sub DAC
D) Mixer and gain-amplifier
Operational Transconductance (OTA) is used in all of the above sub-modules and it is very much important component in the design and utmost proiroty must be given to build a OTA.

3.2 Design of Sample and Hold Circuit

We build an sample and hold circuit with the help of an hold capacitor and a switch which operates at sampling frequency. Here I have used Transmission gate(TG) as switch and an hold capacitor of 10pF value. The idea behind using TG as switch is that we can get maximum sampling frequency. Generally, upper limit on sampling frequency is depended on the type of switch used, and with TG as switch we can get to around 100-200Mhz of sampling frequency without affecting the output much.
The effect of hold capacitor and sampling frequency on the sampled output is shown.

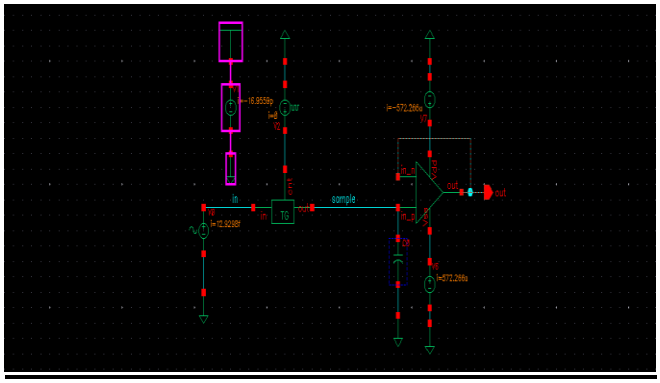

Figure 4: sample and hold circuit Schematic

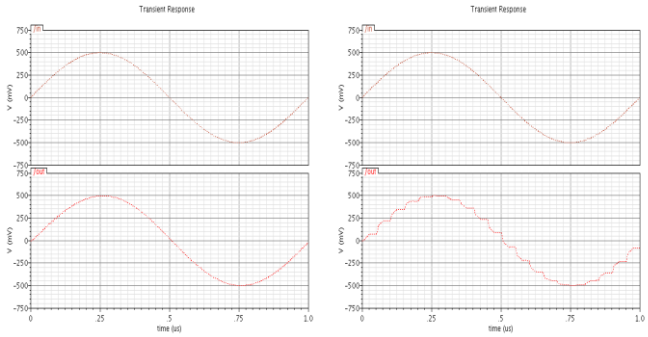

Figure 5: SNH output (left image Fs=100MHz, right image Fs=20MHz)

3.3 Sub 3-Bit ADC

Flash type ADC uses a series of comparators whose output is either high(logic high (V_{DD})) or logic low(ground) depending upon the relation between input signal and the reference

voltage at a given point of time. If Vref is smaller then Vin then logic high value is outputed by comparator else a logic low vaule is obtained.

For n-bit flash ADC, we need $2^{(n)}$-1 comparator and 2^n resistors of same value. So for 3-bit flash, 7 comparators and 8 resistors of 1KΩ are used. 7 comparators produces 7 output bits. This 7 bits are called thermometric codes, just because it consists of consecutive '1's followed by consecutive '0's at a perticular instant of time.An thermometric to binary encoder is designed using 4, 2:1 multiplexer. We can also build the same using 4- 1 bit full adder block.

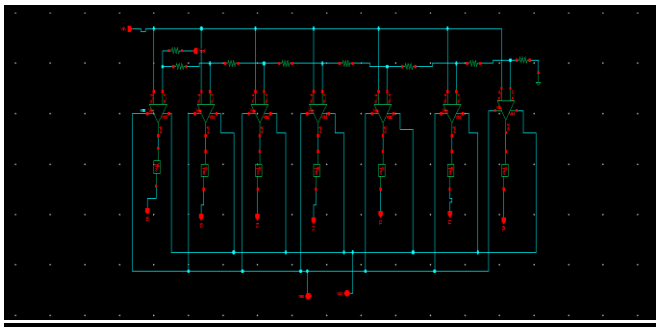

Figure 6: Bank of Comparator Schematic

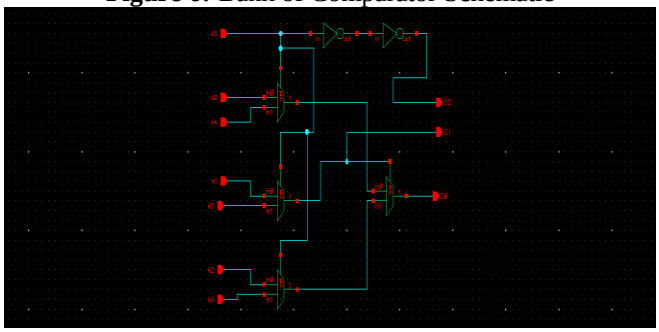

Figure 7: Thermometric to binary Encoder Schematic(Using MUX)

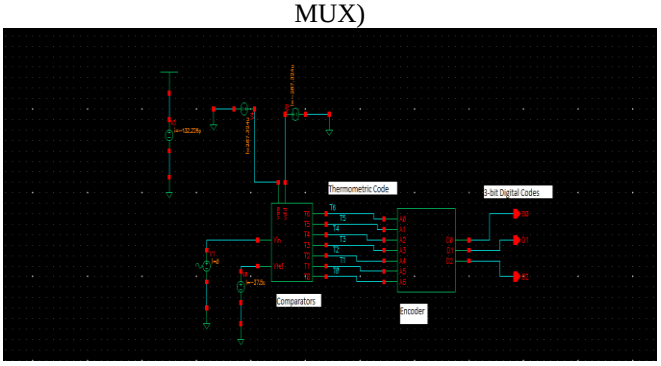

Figure 8: 3-bit Flash ADC Schematic

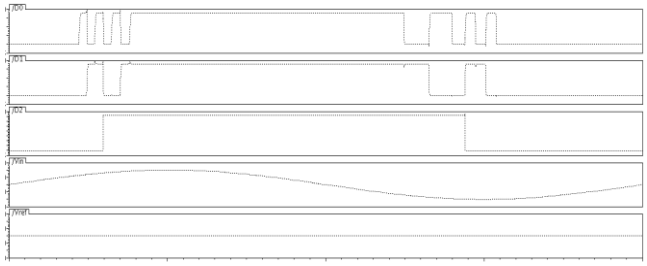

Figure 9: 3-bit Output of sub-ADC

3.4 Digital Correction Block

The bits from each stage are not resolved at the same time. As a result the output bits from 6 different stages that correspond to the same input sample are ready at different point in. The bits from each stage are not resolved at the same time. As a result the output bits from 6 different stages that correspond to the same input sample are ready at different point in.

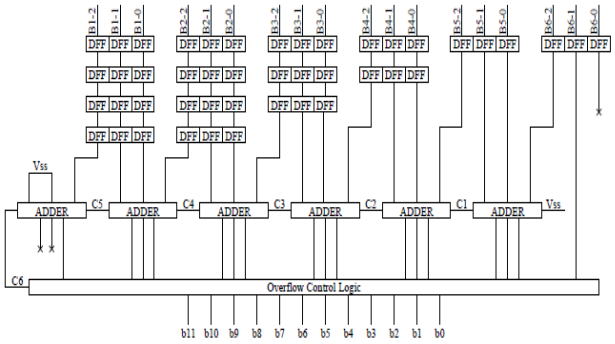

Figure 10: Time Alignment and Digital Correction Logic

The number of DFF in each shift register to pick the correct data is determined by clocking scheme and verified by simulation. The output bits from 6 stages, after being aligned, enter digital correction process which uses digital adders to overlap one bit from each stage with one bit from its neighbors.

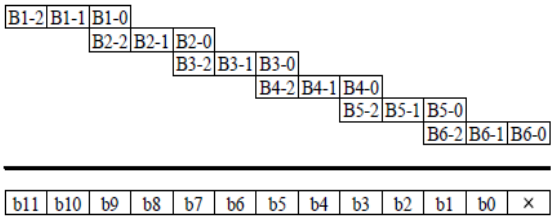

Figure 11: Digital Correction Logic

3.5 12-Bit Pipeline ADC Result

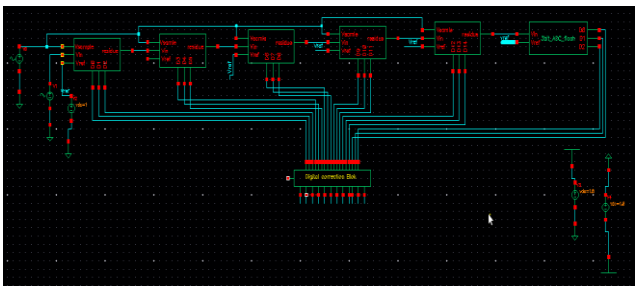

Figure 11: 12Bit Pipeline ADC schematic

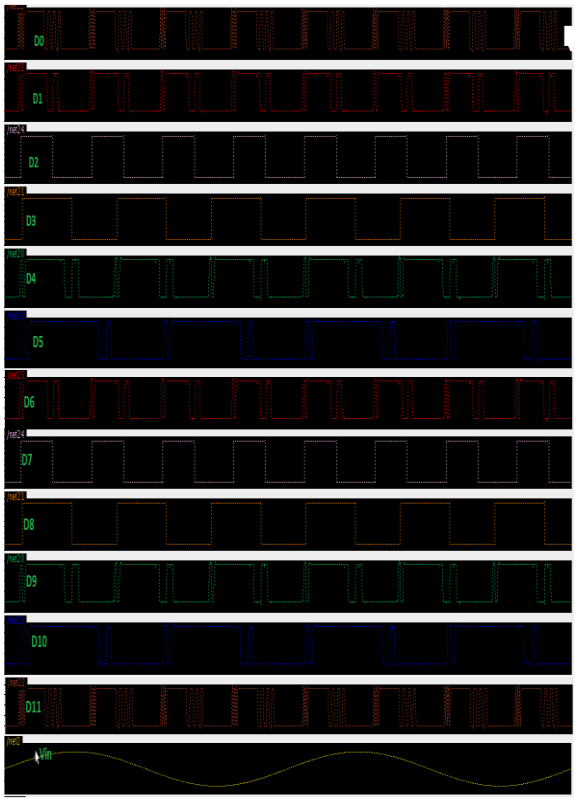

Figure 11: 12Bit Pipeline ADC

Table 1: Different measured parameter in 180nm

Parameters	Present Work
Resolution	12Bit
Power consumption	230mW
INL	0.4067LSB
DNL	0.2049LSB
SNDR	62.21 dB
ENOB	10.041bit

4. Conclusions

The paper describes the design a 12-bit pipelined ADC. The different ADC architectures were analyzed to determine the optimal topology for the given performance specifications with minimum power consumption. Few blocks used is each stages of pipeline is being designed and implemented in Cadence Virtuoso IDE Environment in 180nm technology. Sample and Hold and Sub-ADC (Flash) are the two blocks being simulated and cross checked for correct operation. Sub DAC and a residue amplifier is to be built so as to complete a single stage of ADC. The Characteristic of Pipelined ADC is measured consummation power is 230m, DNL and INL of 0.2049LSB and 0.4067LSB respectively and the SNDR is 62.21db.The supply is given to pipeline ADC is 3.3V.

5. Acknowledgment

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