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Space Vector Pulse Width Amplitude Modulation for Boost Voltage Source Inverter

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Abstract: ***This paper proposes a space vector pulse width amplitude modulation (SVPWAM) method for a boost voltage source inverter. For a VSI, the switching loss is reduced when compared to a conventional sinusoidal pulse width modulation (SPWM) method. The output harmonic distortion of SVPWAM is lower than that of the SPWM, by using only one-third of the switching frequency compared to the latter one. As a result, it is feasible to use SVPWAM to make the boost inverter suitable for applications that needs high power density, high efficiency and low cost. The application includes DC power source utilization, power grid, induction heating and electric vehicle motor drive.***

Keywords: Boost, SVPWAM, switching loss reduction, SPWM, harmonic distortion.

1. Introduction

In recent days the grid tie inverter technology has a vast development. Here the solar power which is a dc is converted to ac for tying with the grid. The inverter is required to inject low harmonic current to, in order to increase the efficiency. For this purpose, the switching frequency of the inverter is designed within a high range from 15 to 20 kHz, resulting in the increase in switching loss in the switching device.

To rectify this problem, different types of soft-switching methods have been proposed in [1]–[3].A diode rectifier with small DC link capacitor have been proposed in [4], [5], [8]–[12]. various types of modulation techniques have been proposed previously such as optimized pulse-width-modulation in [13], improved Space-Vector-PWM control for different optimization targets and applications [14]–[16], and discontinuous PWM (DPWM) [17]. Different switching sequence arrangement can also affect the harmonics, power loss and voltage/current ripples [18]. DPWM has been widely used to reduce the switching frequency, by selecting only one zero vector in one sector. It results in 50% switching frequency reduction. However, if the same output THD is required, DPWM cannot reduce switching loss compared to SPWM. It will also worsen the device heat transfer because the temperature variation. A double 120 flattop modulation method has been proposed in [6] and [7] to reduce the period of PWM switching to only 1/3 of the whole fundamental period. In addition to that, the method is only specified to a fixed topology, which cannot be applied widely.

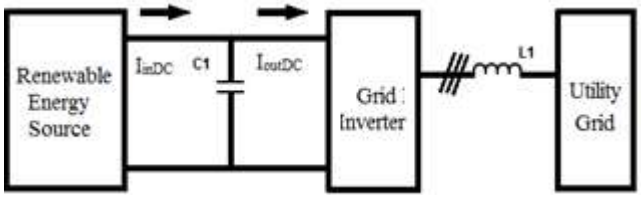

Figure 1: Typical configuration of a series power grid connection

This paper proposes a novel generalized space vector pulse width amplitude modulation (SVPWAM) method for the boost voltage source inverter (VSI). By eliminating the conventional zero vector in the space vector modulation, two-third switching frequency reduction can be achieved in VSI. If a unity power factor is assumed, an 87% switching loss reduction can be implemented in VSI.

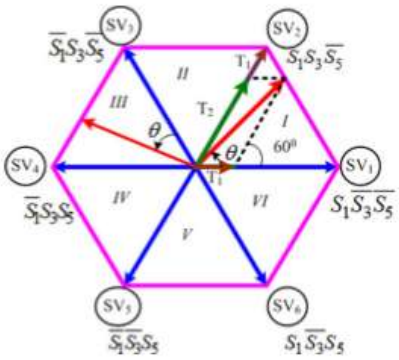

Figure 2: SVPWAM for VSI

2. SVPWAM for VSI

A. Principle of SVPWAM Control in VSI

The principle of an SVPWAM control is to eliminate the zero vectors in each sector. The modulation principle of SVPWAM is shown in Fig.2. In each sector, only one phase leg is doing PWM switching; thus, the switching frequency is reduced by two-third. This imposes zero switching for one phase leg in the adjacent two sectors. For example, in sector VI and I, phase leg A has no switching at all.

The dc-link voltage thus is directly generated from the output line-to-line voltage. In sector I, no zero vector is selected. Therefore, S_1 and S_2 keep constant ON, and S_3 and S_6 are doing PWM switching. As a result, if the output voltage is kept at the normal three-phase sinusoidal voltage, the dc-link voltage should be equal to line-to-line voltage V_{ac} at this time. Consequently, the dc-link voltage should present a 6ω varied feature to maintain a desired output voltage. A dc–dc conversion is needed in the front stage to

generate this 6ω voltage.The original equation for time period T_1 and T_2 are

$$T_1 = \frac{\sqrt{3}}{2} m \sin\left(\frac{\pi}{3} - \theta\right)$$

$$T_2 = \frac{\sqrt{3}}{2} m \sin(\theta)$$

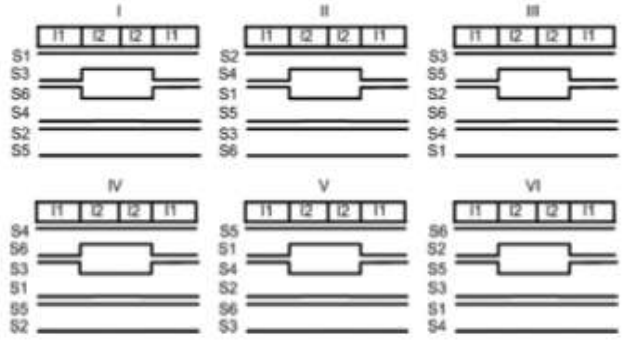

Figure 3: Vector placement in each sector for VSI

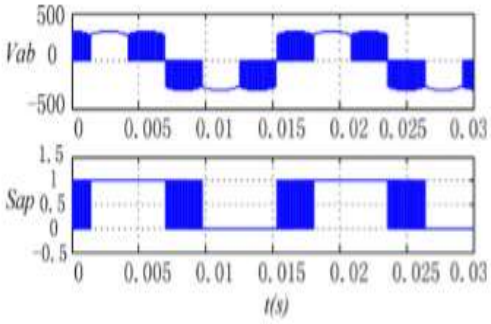

Figure 4: Theoretic waveforms of dc-link voltage, output line-to-line voltage and switching signals

where θ ∈[0, π/3] is relative angle from the output voltage vector to the first adjacent basic voltage vector like in Fig. 2. If the time period for each vector maintains the same, the switching frequency will vary with angle, which results in a variable inductor current ripple and multi frequency output harmonics. Therefore, in order to keep the switching period constant but still keep the same pulse width as the original one, the new time periods can be calculated as

$$\frac{T_{1'}}{T_s} = \frac{T_1}{(T_1 + T_2)}$$

The vector placement within one switching cycle in each sector is shown in Fig. 3 and 4 shows the output line-to-line voltage and the switching signals of S_1.

B. Inverter Switching Loss Reduction for VSI

For unity power factor case, the inverter switching loss is reduced by 86% because the voltage phase for PWM switching is within [−60°, 60°], at which the current is in the zero-crossing region. In VSI, the device voltage stress is equal to dc-link voltage V_{DC}, and the current stress is equal to output current i_a. Thus the switching loss for each switch is

$$P_{SW\_I} = \frac{1}{2\pi}\int_{-\pi/6}^{\pi/6} E_{SR}\frac{|I_m \sin(\omega t)|V_{DC}}{V_{ref}\, I_{ref}} f_{sw}\, d\omega t + \int_{5\pi/6}^{7\pi/6} E_{SR}\frac{|I_m \sin(\omega t)|V_{DC}}{V_{ref}\, I_{ref}} f_{sw}\, d\omega t$$

$$P_{SW\_I} = \frac{2-\sqrt{3}}{\pi}\left(\frac{I_m V_{DC}}{V_{ref}\, I_{ref}}\right) E_{SR} f_{sw}$$

where E_{SR},V_{ref}, I_{ref} are the references.

Since the SVPWAM only has PWM switching in two 60◦ sections, the integration over 2π can be narrowed down into integration within two 60°

$$P_{sw\_I} = \frac{2\sqrt{3}}{\pi}\left(\frac{I_m V_{DC}}{V_{ref}\, I_{ref}}\right) E_{SR} f_{sw}$$

The switching loss for a conventional SPWM method is

$$P_{sw\_I'} = \frac{2}{\pi}\left(\frac{I_m V_{DC}}{V_{ref}\, I_{ref}}\right) E_{SR} f_{sw}$$

In result, the switching loss of SVPWAM over SPWM is f = 13.4%. However, when the power factor decreases, the switching loss reduction amount decreases because the switching current increases. As indicated, the worst case happens when power factor is equal to zero, where the switching loss reduction still reaches 50%. In conclusion, SVPWAM can bring the switching loss down by 50–87%.

Topologies for SVPWAM

Basically, the topologies that can utilize SVPWAM have two stages: dc–dc conversion which converts a dc voltage or current into a 6ω varied dc-link voltage or current; VSI for which SVPWAM is applied. One typical example of this structure is the boost converter inverter discussed previously.

The front stage can also be integrated with inverter to form a single stage. Take current-fed quasi-Z-source inverter as an example. Instead of controlling the dc-link current I_{pn} to have a constant average value, the open zero state duty cycle D_{op} will be regulated instantaneously to control I_{pm} to have a 6ω fluctuate average value, resulting in a pulse type 6ω waveform at the real dc-link current I_{pn}, since I1 is related to the input dc current I_{in} by a transfer function.

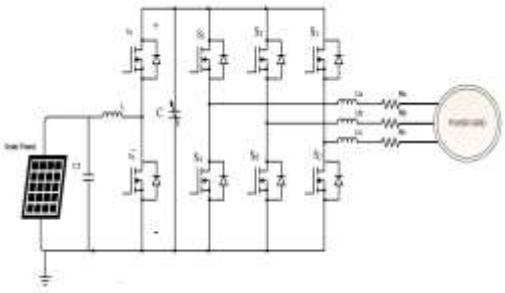

Figure 5: SVPWAM - based boost-converter –inverter power grid connection

3. Case Study: Boost Converter Inverter for Power Grid Application

A. Basic Control Principle

The circuit schematic and control system for a boost converter inverter for a power grid system is shown in Fig.9. A 6ω dc-link voltage is generated from a constant dc voltage by a boost converter, using open-loop control. Inverter then could be modulated by a SVPWAM method. The specifications for the system are input voltage is 39.2V; the average dc-link voltage is 78.6V; output line-to-line voltage rms is 89V.

B. Variable DC-Link SPWM Control at High Frequency

When the output needs to operate at a high frequency, between 120 Hz and 1 kHz, it is difficult to obtain a 6ω dc-link voltage without increasing the switching frequency of the boost converter. It is because the controller does not have enough bandwidth.

Also, increase in boost converter switching frequency would cause a substantial increase of the total switching loss, because it takes up more than 75% of the total switching loss. This is due to, the boost converter switches at a complete current region. Also a normal SPWM cannot be used in this range because the capacitor is designed to be small that it cannot hold a constant dc link voltage.

Therefore, its optimum option is to control the dc link voltage to be 6ω and do a variable dc link SPWM modulation. In this variable dc-link SPWM control, in order to obtain better utilization of the dc-link voltage, an integer times between the dc-link fundamental frequency and output frequency is preferred.

When the output frequency is in [60 Hz, 120 Hz], a 6ω dc link is chosen; when the frequency is in [120 Hz, 240 Hz], a 3ω dc link is chosen; when the frequency is in [240Hz, 360Hz], a 2ω dc link is chosen.

C. Experiment Results

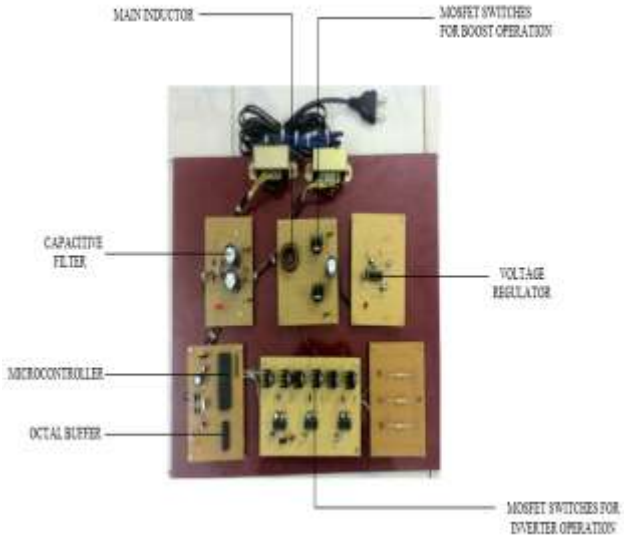

Figure 6: Prototype of SVPWAM - based boost-converter – inverter power grid connection

Output Waveform

Parameter	Value	Unit
Main Inductor	1	mH
Switches	MOSFET	IRF840
Microcontroller	ATMEL	AT89C51
Buffer	Octal buffer	74ALS244A
Filter Capacitor	2200	µF
Load Resistance	1	kΩ
Input Voltage	39.2	V
Boosted Voltage	78.6	V
Output Voltage	89	V

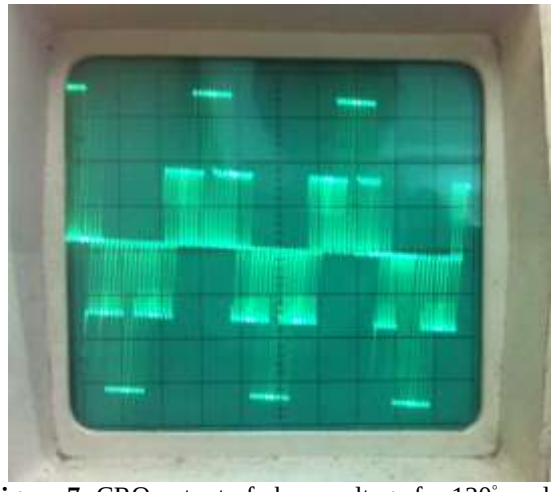

Figure 7: CRO output of phase voltage for 120° mode.

D. Simulation Results

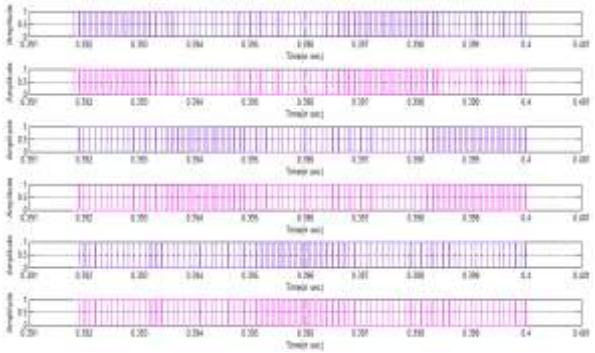

Figure 8: Gate Pulses to Switches.

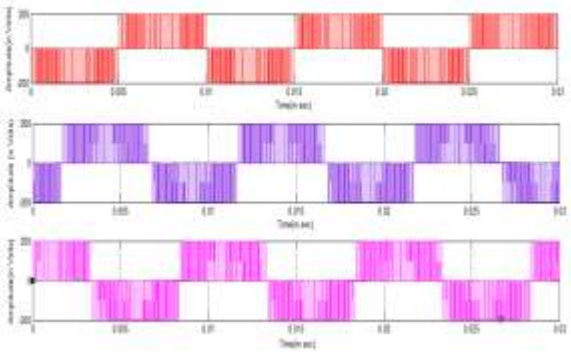

Figure 9: Line Voltage Waveform

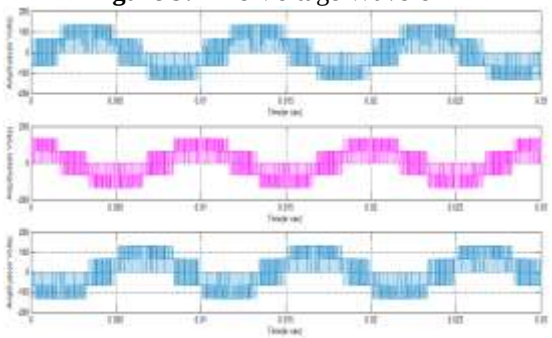

Figure 10: Phase Voltage Waveform.

4. Conclusion

Hence the SVPWAM control method has the following advantages over the SPWM method.
1) The switching loss is reduced compared to the conventional SPWM inverter system.

2) The overall cost is reduced by 30% because of reduced value of passive elements, usage of heat sinks.

The efficiency of the proposed method in the reduction of power losses has been tested by the experimental results that were obtained from the prototype model developed.

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