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Design of Low Power Phase Frequency Detectors and VCO using 45nm CMOS Technology

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Abstract: ***Phase locked loop (PLL) is one of the most crucial devices in almost all the electronic systems. PLLs are commonly used as clock generator or frequency synthesis in electronic applications. Phase noise represents the phase variations of a PLL output signal. Since Phase noise reflects the stability of the PLL systems it is considered the most important characteristic. For any electronic device in today world, it is considered best when it consumes low power and delivers maximum efficiency. To reduce the delay a PFD is designed using XOR and NAND gate. To increase the delay and decrease the frequency a Ring oscillator is designed with odd number of invertors and Noise immunity is increased by using a differential amplifier as it has double ended configuration which removes the common mode noise. The voltage control circuit is a cascade current mirror circuit. The PLL is designed using 45nm CMOS technology for high performance with 1.0 V power supply***

Keywords: PLL, Voltage controlled oscillator, PFD, Tanner Tool

1. Introduction

A phase-locked loop (PLL) is an electronic feedback system which generates a signal whose phase is locked to the phase of an input reference signal. Common uses of PLLs are radio, telecommunication, computer and other electronic systems. The common applications of PLLs include:

- Clock generation: All the electronic systems which operate over 100MHz, their clocks are generated by PLLs, which multiply a lower frequency up to the required operating frequency. The multiplication factor can be quite large where the operating frequency is in terms of GHz and the reference crystal is just in terms of MHz.
- Frequency synthesis: In wireless communication and satellite communication systems, PLLs are used to generate the radio frequency (RF) signals.
- Clock recovery: Few data streams like high speed serial data streams are transmitted without any accompanying clock. The receiver generates a clock from an approximate frequency reference, and then phase-aligns to the transitions in the data stream with a PLL. In high speed serial data an application, the clock is usually generated when the references clock with a PLL are multiplied. The phase noise of the PLL is proportional to the clock jitter, which means the phase noise at the crossing time. Jitter causes errors when the timing of a signal transition fluctuates horizontally across the sampling point. Large jitter reduces the signal-to-noise ratio (SNR) and results in high bit-error-ratio (BER). PLL designs are mostly focused on achieving low phase noise.

2. PLL Working Principles

A PLL consists of four basic functional blocks:

1. Voltage-controlled oscillator (VCO): The output frequency of this device is an increasing function of its input voltage.
2. Phase detector (PD): Compares a periodic input signal with the frequency divider output signal. The output voltage is proportional to the phase difference between the two signals.
3. Loop filter (LF): This is a lowpass filter that smoothenss the PD output signal and applies it to the VCO input.
4. Frequency divider (FD): The output of the frequency divider is a signal with a frequency equal to the VCO output frequency divided by a division factor N [1].

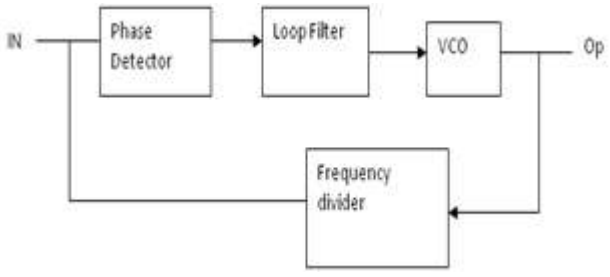


Figure 2: Block Diagram of PLL

The PLL is a servo-controlled system. If its loop gain is high enough and the loop is stable, the system will reach a stable condition where two PD inputs have the same phase and thus the same frequency (the angular frequency is the derivative of the phase with respect to time). In this condition, the output frequency equals the input frequency multiplied by N.

$$f_{out} = N.f_{in} \quad (1)$$

3. Phase Frequency Detector

A phase-frequency detector (PFD) compares the two input signals, the output of the frequency divider and the input reference signal, and generates the output signals that correspond to the phase difference between the two input signals[5]. PFDs are usually implemented with digital circuits. PFD using Different Gates are also implemented.

A. PFD Implementation Using Logic Gates

Fig 2 shows the block diagram of PFD using NOR gate. The circuit has two resettable nobe and the edge triggered D flip of input is tied to the logic 1 and NOR is used in reset path.

REF and VCDL are used as a clock to the circuit. PFD has four states UP=0 and DN=0,UP=1 and DN=0,UP=0 and DN=1and UP=1 and DN=1. Inputs are given to the circuit by using UP and DN. When REF goes high than VCDL then UP goes low because UP and DN are not NOR together so RESET is set to be high and its resets the PFD into the initial stage [1].

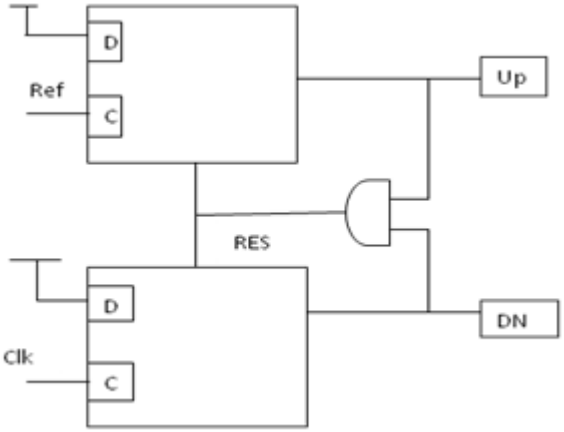


Figure 3.2: AND gate based PFD

Likewise NAND gate PFD is also implemented. In above fig NOR gate is replaced by NAND gate. NAND Gate in the reset path [3]. At initial stage both UP and DN are set to be low or set REF and Deviation signals to be high. During falling edge the output is transmitted to the UP. Once UP and DN is goes high the system is set to be reset. AND gate PFD implementation is similar to above two. Two FFs are set to be reset. UP remains in same state until the transition occurs in the circuit. When reset goes high PFD goes to the initial state. The below figures show the simulation results of PFD using various logic gates.

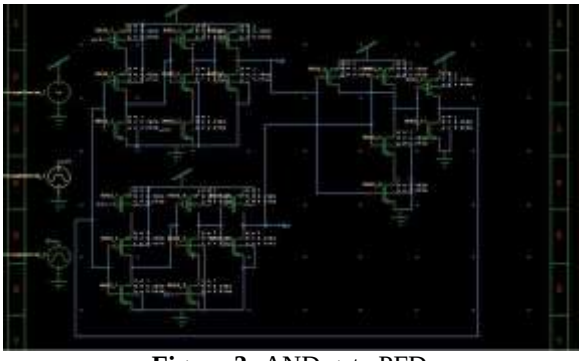


Figure 3: AND gate PFD

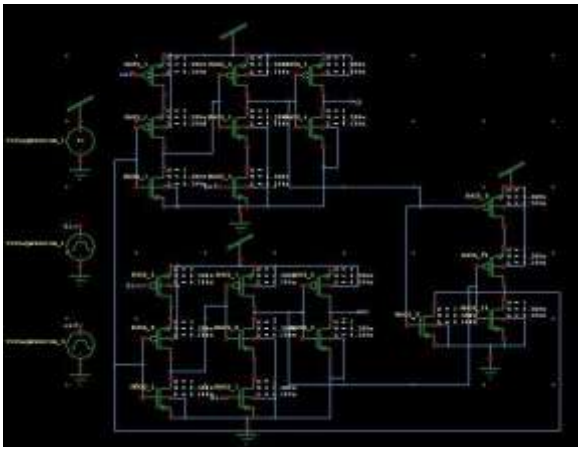


Figure 4: NOR gate PFD

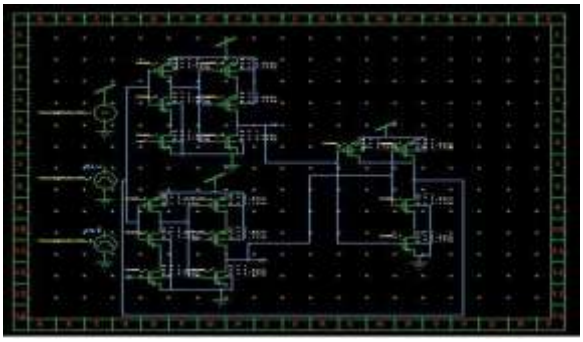


Figure 5: NAND gate PFD

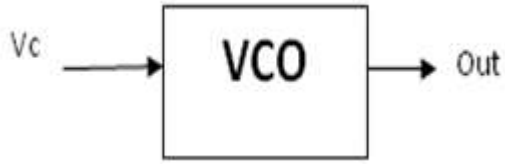
It is seen that NAND based PFD consumes lower amount of power and occupies less area than other two. They all have the same range of operating frequency. Dead Zone problem is also negligible for the NAND Based PFD.

4. Voltage Controlled Oscillator

Voltage controlled oscillator is a part of PLL that produces oscillatory output. The level of control is related to the periodic signal that applied to the VCO. Output frequency of the VCO is directly propositional to the applied voltage.

A. Working of VCO

An oscillator may also used in the feedback circuit to route sufficient amount of input to the output to maintain the oscillations. Gain of VCO is measured by using the ratio of input voltage frequency to the output frequency [4]. Depends on the control voltage input is produces reliable frequency at the output. It may be adjustable to control the period output frequency. It has more than one capacitor to adjust the frequency oscillation. Tuning is done by using varactor diode. To minimize the tuning rang programmable capacitors are used. Narrow band oscillator gives better performance than wideband VCO. But for application purpose wide band VCOs are used like radars.



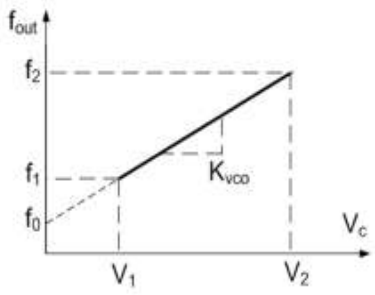


Figure 6: Voltage Controlled Oscillator

Centre frequency is the middle value of minimum and maximum. Tuning range its depends on two parameters namely middle frequency and its temperature Gain it should be high to accomplish the need of tuning requirement. Noise in the input frequency will affect the performance of the VCO. To minimize the noise Kvco must be small. Even though noiseless input is applied the electronic components produces noise in the frequency output.

B. Ring oscillator

A ring oscillator is a collection of Odd number of NOT inverters is connected together to produce output between two voltage ranges like true and false. All the NOT gates are connected in a chain model with feedback at the last. It has number of loop gain stages. Because a single inverter computes the logical NOT of its input, it can be shown that the last output of a chain of an odd number of inverters is the logical NOT of the first input[7]. The last output is declared after the first input is applied this feedback produces the oscillation. Even number of inverter should not be used in the oscillator because last output is same as the input.

5. Properties of Ring Oscillator

Oscillation occurs due to multiple poles and multiple stages. 2. The number of inverter must be Odd so that we can avoid latch up. 3. The number stages in the oscillator is depends on power, speed and noise. 4. Reliable results is achieved by using three or more stage. 5. Its also a member of delay oscillator. 6. It used more than one inverter to produce gain more than one. 7. It increases the delay in the circuit due to more number of stages thereby it decreases the oscillation in the circuit. 8. Delay is decreased by increasing the voltage level.

6. Design Consideration

1. Differential Amplifier

Differential amplifier has four pmos and two nmos. P1 and P2 are the input to the circuit. Its biased in linear region so that its act as a active resistor. P3 and p4 are the main driver for the system. Both nmos are controlled by tuning voltage its also behave like a current biasing circuit. Current is controlled by using tuning voltage.

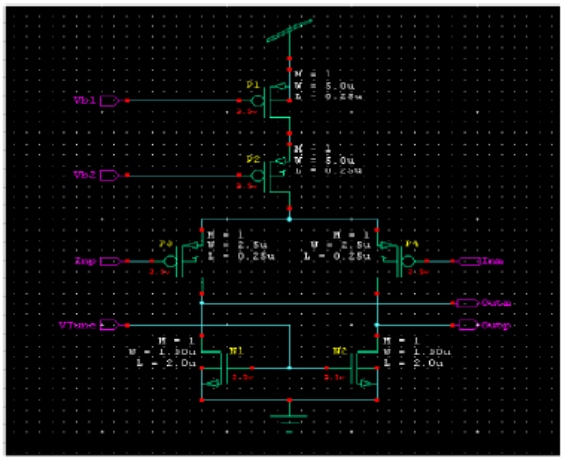


Figure 7: Differential Amplifier

7. Control Circuit

Control circuit is shown in fig.8. This basically discloses the importance of current mirror in giving constant current to the circuit. The main purpose of the control circuit in VCO is that to differentiate from other VCO circuits. It has two pmos and one nmos in each side [8]. Voltage controls the current in the circuit. Cascade current mirror circuit is used. When biasing voltage is increased the current flow is decreased. Because the gate depends on the gate to source and drain to source.

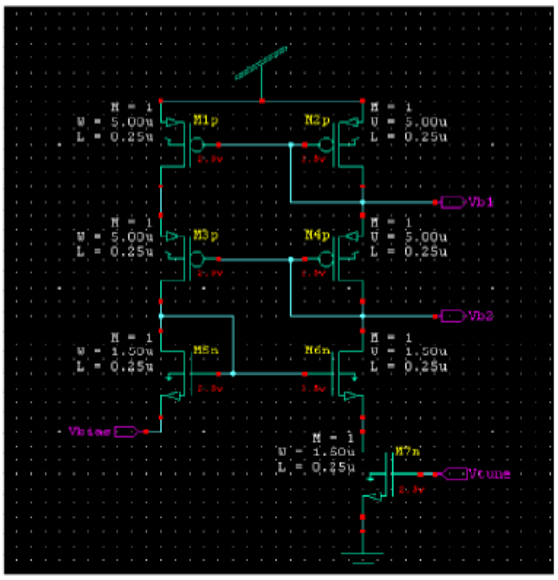


Figure 8: Control Circuit

8. Ring Voltage Controlled Oscillator

Differential amplifier based VCO is best choice for design low power oscillator. Five differential amplifiers is shown in fig.9 here all the stages are connected in series and last output is connected to the first stage. Each stage is connected with the control circuit. Two biasing voltages are used for the control blocks. Delay is equal to RC time delay. When number stages increases delay also get increased. While changing the biasing voltage resistance value also changed. Capacitance is not possible to change. The simulation result of VCO is shown in fig. 10. The proposed

differential amplifier ring VCO is implemented in 90nm CMOS technology. The supply voltage required for this design is 1V. From circuit simulations; the low power consumption is achieved.

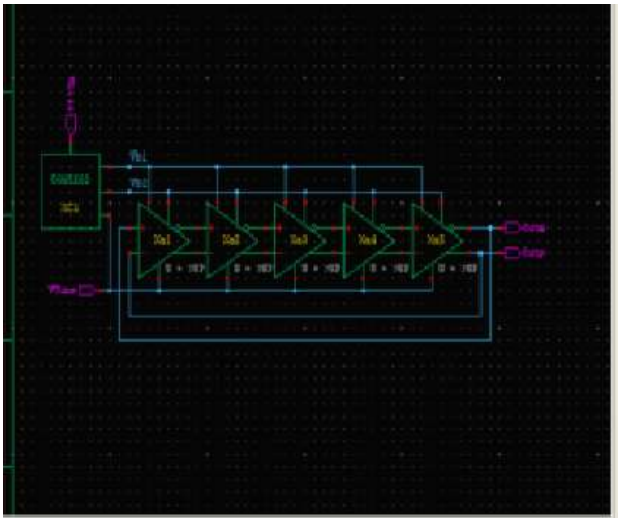


Figure 9: Ring oscillator

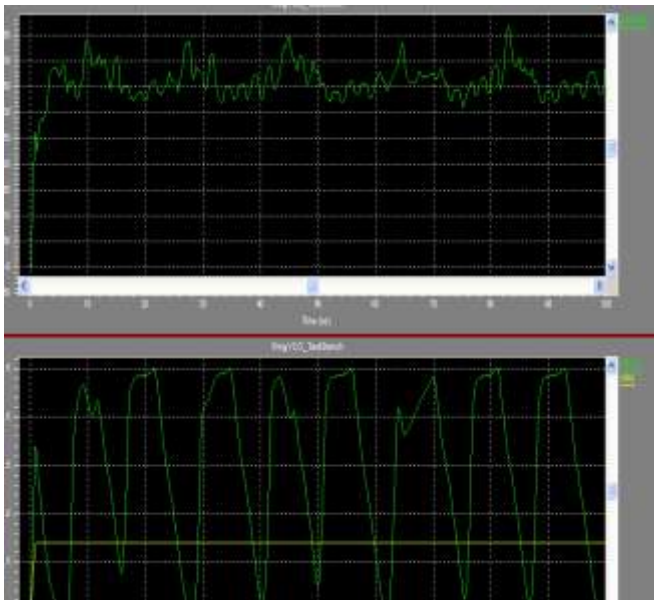


Figure 10: Simulation Waveform

9. Source Coupled VCO

To design low power VCO source coupling technique is used. Its shown in below fig the transistor M3 and M4 are used in output side and M5 and M6 behave as a current source. M1 and M2 are used as a switch. M1 is Off and M1 in On stage terminal voltage out1 is longer than others. So the capacitor is in charge mode due to M6. When X and Y are same the capacitor is fully charged. While M1 turn and M2 turns off the capacitors starts discharging.

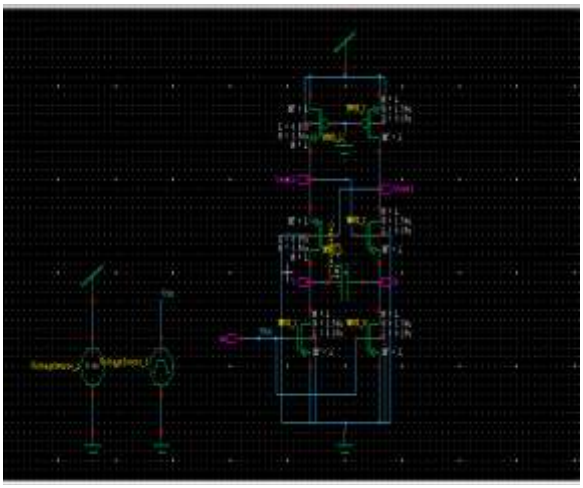


Figure 11: Source couple VCO

10. Conclusion

This chapter compares the performance of Phase Frequency Detectors by different Logic Gates .As can be seen from the simulation results AND based PFD consumes maximum amount of power among all the PFDs and has highest delay. NOR based PFD consumes more area and power compared to the NAND based PFD. Therefore, in order to have low power consumption and smaller area we use NAND based PFD which is also having approximately zero Dead Zone problem. A differential amplifier based ring VCO and source coupled VCO is designed which has low power and high speed.

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