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Review on Design of PWM Controller Using FPGA

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Abstract: ***Pulse width modulation (PWM) has been widely used in power converter control. Most high power level converters operate at switching frequencies up to 500 kHz, while operating frequencies in excess of 1 MHz at high power levels can be achieved using the planar transformer technology. The contribution of this paper is the development of high-frequency PWM generator architecture for power converter control using FPGA and CPLD ICs. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution requirements.***

Keywords: Pulse width modulation, Power converters, Field programmable gate array, CPLD

1. Introduction

The pulse width modulation (PWM) principle iswidely used in power electronics applications forcontrolling power converters (DC/DC, DC/AC,etc.) The PWM signal is generatedby comparing an adjustable reference voltage, Vref, with a triangular wave of constantamplitude and frequency, as shown in Fig. 1(b).

The DC output voltage is regulated to the desiredvalue by adjusting the reference voltage value, thusmodifying the PWM signal duty cycle, as follows:

$$Vo = D.Vin = \frac{ton}{Ts}.Vin = \frac{Vref}{Vtr}.Vin$$

where Vin is the converter DC input voltage, D is thePWM signal duty cycle ($0 \le D \le 1$), ton is the PWMsignal ON time, Ts is the converter switching periodand Vtr is the triangular wave amplitude.

The Sine Wave is used as a reference to generate PWM, because many AC Motors runs at 50 Hz supply, the 50 Hz Sine Wave (Vm) is generated using FPGA controller as shown in figure 1.1. The high frequency Triangular wave (Vc) shown in figure 1.2 is used as a carrier signal. This high frequency Triangular wave carrier signal is compared with a Sinusoidal reference signal. The crossover points are used to determine the switching instants such that if Vreference is greater than Vcarrier then output is high otherwise output is low. The PWM output is shown in figure 1.3.

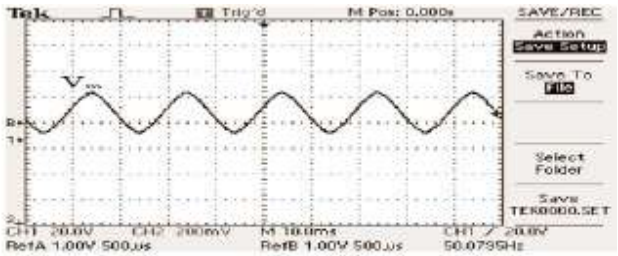

Fig.1.1: Sine wave

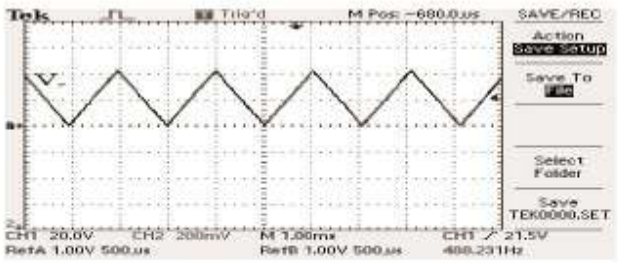

Fig.1.2: Triangular wave

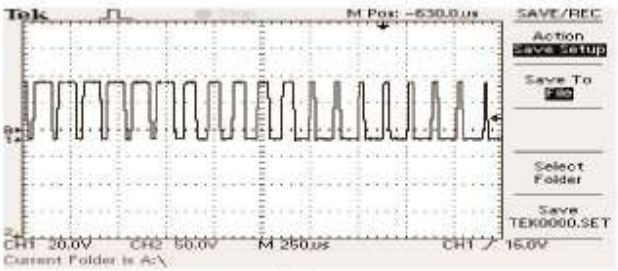

Fig.1.3: SPWM wave

2. Important Terminology

2.1 Pulse Width Modulation (PWM)

In PWM, the time period of the square wave is kept constant and the time for which the signal remains high is varied or modulated. The duty cycle and average DC value of the signal can be varied. PWM provides a powerful method for controlling analog circuits with the help of an output from a digital system.

A PWM circuit works by making a pulsating DC square wave with a variable on-to-off ratio. The average on time may be varied from 0 to 100 percent. The widths of the pulses are proportional to the input signal. When the signal is small, a series of narrow pulses is generated. When the signal is large, a series of wide pulses is generated.

2.2 FPGA

FPGAs are a semiconductor device containing programmable logic components called "logic blocks", and programmable interconnects [2]. Logic blocks can be programmed to perform the function of basic logic gates such as AND and XOR, or more complex combinational functions such as decoders or simple mathematical functions. FPGAs are also known as reconfigurable devices. These

reconfigurable FPGAs are generally favored in prototype building because the device does not need to be thrown away every time a change is made. This allows one piece of hardware to perform several different functions. Of course, those functions cannot be performed at the same time. Besides that, FPGAs are standard parts, they are not designed for any particular function but are programmed by the customer for a particular purpose [2].

The development of field programmable gatearray (FPGA) and complex programmable logicdevice (CPLD) ICs during the last years providesan alternative solution for the implementation ofdigital power converter control units. They havethe advantage of flexibility due to their reprogramming capability, while their operating frequency can be as much as hundreds of MHz FPGAs have been used in power electronics applications.

The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required.

The proposed PWM architecture is described inSection 3, while the simulation and conclusion are presented in Sections 4 and 5, respectively.

3. The Proposed PWM Architecture

The block diagram of the proposed architectureis shown in Fig. 2. The system input is an N-bit dataword, corresponding to the desired PWM duty cycle.The N-bit register output,containing the N-bit data input, is compared with the output value of an N-bit free-running synchronous counter, by means of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition at the end of a PWM period. Also, the counter overflow signal is used to load the N-bit data input to the input register,so that the PWM output duty cycle change is performed at the new PWM wave.

The PWM frequency is given by Eq. (2), while its duty cycle is given from the equation:

$$D = \frac{Data\_Value}{2^N}$$

where Data_Value is the input data word integervalue If an 8-bit input is used, then the duty cycle isin the range $0 \le D \le \frac{255}{256} = 99.6\%$

Since the PWM duty cycle has 2^N different states, the generator resolution, α , is defined as

$$\alpha = \frac{1}{2^N}.100\%$$

In order to achieve high PWM frequencies, resulting in high clock rates, a fast counter is required.

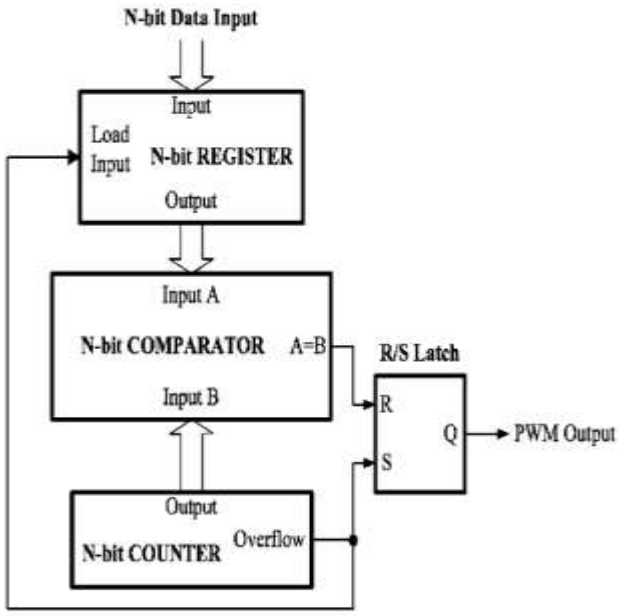

Figure 2: Block Diagram of the proposed PWM Generator.

4. Simulation Results

A software program using the VHDL languagewas developed, for synthesizing the architecture presented in the previous section, using the Xilinx ISE Design Suite 13.1 software. The FPGA or CPLD device type is selected according to the digital control system implementation area and cost requirements.

The result of each block in fig.2 is shown in form of waveforms in fig 3,4,5,6.

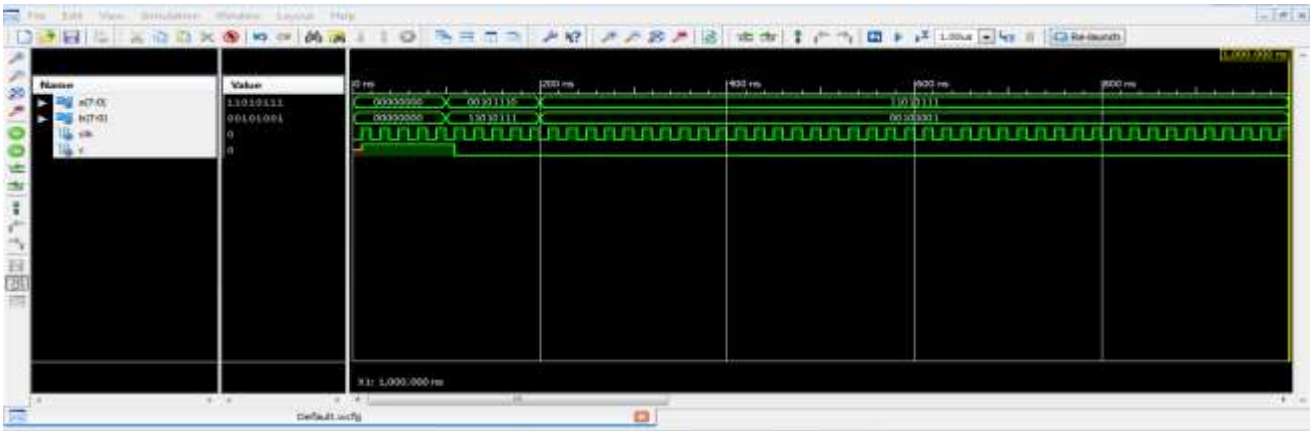

Figure 3: Waveform of comparator

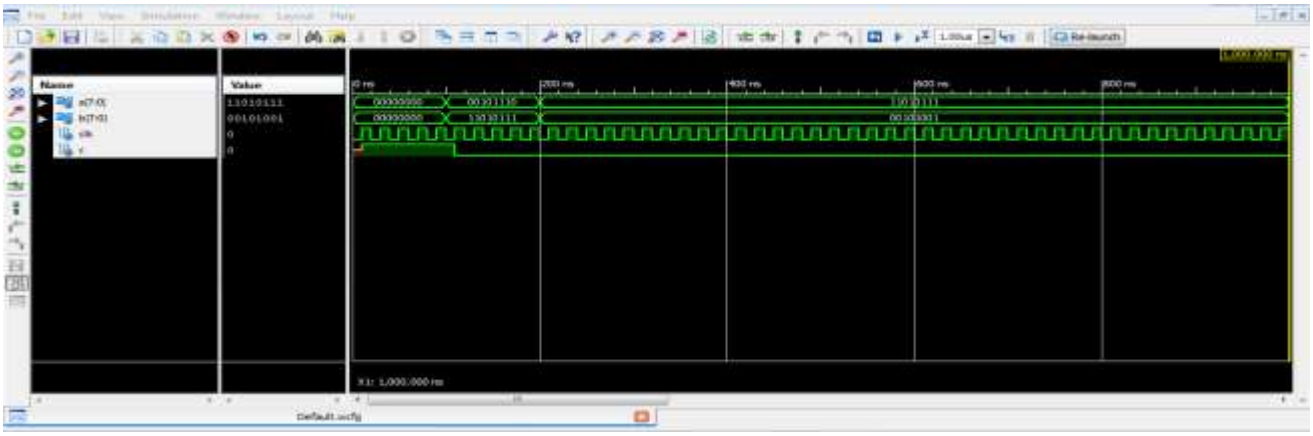

Figure4: Waveform of Register

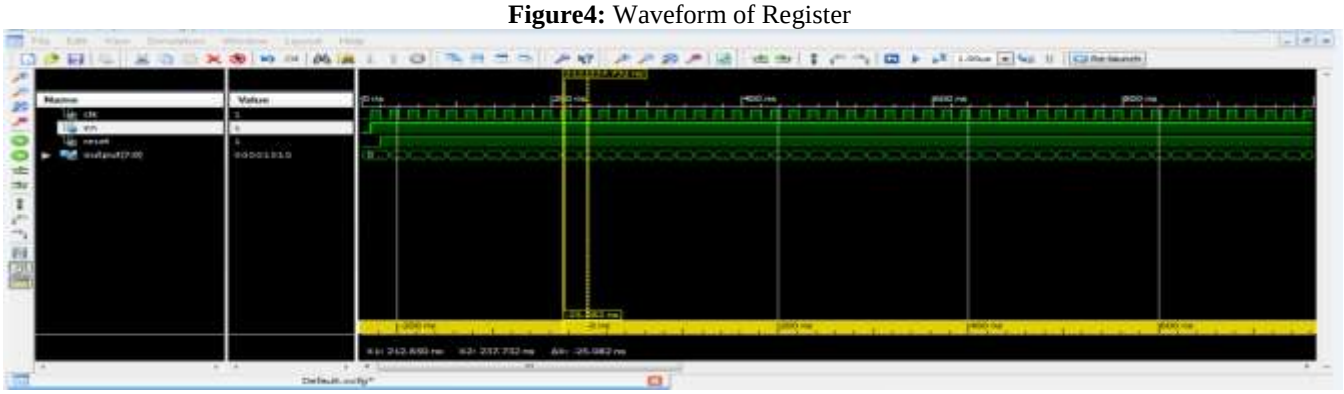

Figure 5: Waveform of counter

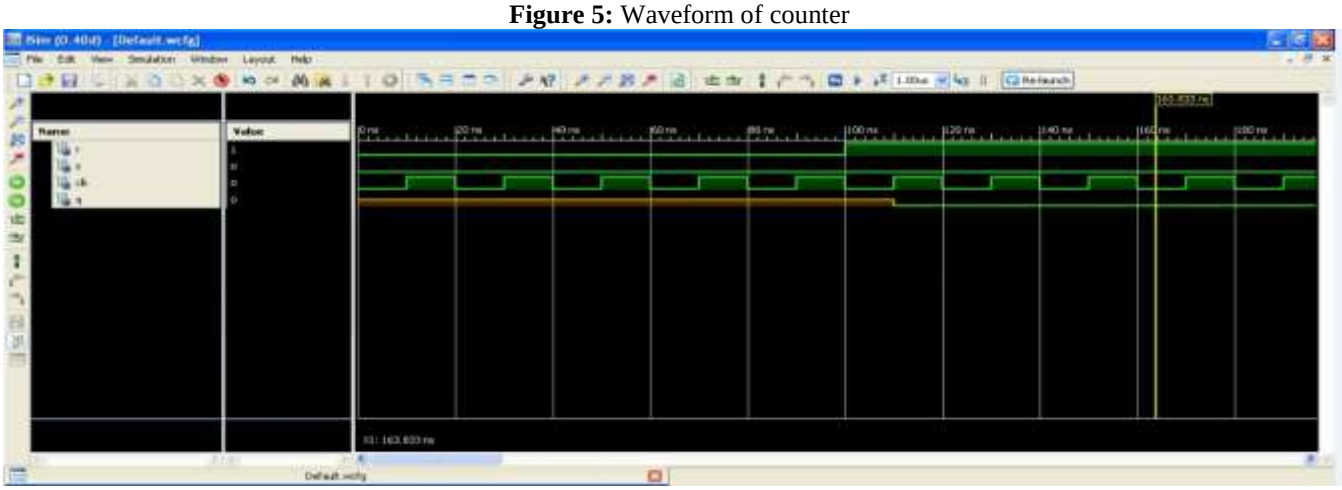

Figure 6: Waveform of R S Latch

From fig.3, the N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit counter, by means of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave

From fig.4, register stores the input to be processed .So when load signal is '1' the register provides input to output.

From fig.5, counter used is 8 bit up-counter.

From fig.6, R S latch is used to set or reset the output. When 'r' signal is '1' output is reset to '0'.When's' signal is '1' output is set to '1'.

5. Conclusions

In this paper, high-frequency PWM generator architecture for power converter control, using FPGA and CPLD ICs, has been presented. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required. The selection of the target device depends on the system cost and resolution requirements.

References

[1] Jakirhusen I. Tamboli, Prof. Satyawan R. Jagtap, Amol R. Sutar , pulse Width Modulation Implementation using FPGA and CPLD ICs, International Journal of Scientific & Engineering Research Volume 3, Issue 8, August-2012 5 ISSN 2229-5518

[2] Wolf Wayne,*"FPGA-Based System Design",* Pearson Education, Inc., USA, 2004.
[3] Massimiliano Luna,, Marcello Pucci,Gianpaolo Vitale and Giuseppe Abbate. Regular paper on 'FPGA-based Random PWM Control of a Buck DC/DC Converter', J. Electrical Systems 6-3 (2010): 323-338.
[4] Eftichios Koutroulis, Apostolos Dollas, Kostas Kalaitzakis" High-frequency pulse width modulation implementation using FPGA & CPLD ICs" accepted 7 September 2005
[5] Anupama, Design of High Resolution DPWM for Power Converters Using General-Purpose FPGAs International *Journal of Research in Advent Technology, Vol.2, No.2, February 2014*
[6] Palmer J.E.., Perlman D.E.,"Introduction to digital system", McGraw Hill.
[7] Nelson, Nagale, Caroll, Irwin, "Digital Logic Circuit Analysis &Design" Prentice Hall.
[8] Brown, Vranesic 'Fundamentals of Digital Logic with VHDL Design', Tata McGraw Hill.

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