reconfigurable FPGAs are generally favored in prototype building because the device does not need to be thrown away every time a change is made. This allows one piece of hardware to perform several different functions. Of course, those functions cannot be performed at the same time. Besides that, FPGAs are standard parts, they are not designed for any particular function but are programmed by the customer for a particular purpose [2].

The development of field programmable gatearray (FPGA) and complex programmable logicdevice (CPLD) ICs during the last years providesan alternative solution for the implementation ofdigital power converter control units. They havethe advantage of flexibility due to their reprogramming capability, while their operating frequency can be as much as hundreds of MHz FPGAs have been used in power electronics applications.

The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required.

The proposed PWM architecture is described inSection 3, while the simulation and conclusion are presented in Sections 4 and 5, respectively.

3. The Proposed PWM Architecture

The block diagram of the proposed architectureis shown in Fig. 2. The system input is an N-bit dataword, corresponding to the desired PWM duty cycle.The N-bit register output,containing the N-bit data input, is compared with the output value of an N-bit free-running synchronous counter, by means of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave. The R/S latch output is set when the counter reaches an overflow condition at the end of a PWM period. Also, the counter overflow signal is used to load the N-bit data input to the input register,so that the PWM output duty cycle change is performed at the new PWM wave.

The PWM frequency is given by Eq. (2), while its duty cycle is given from the equation:

$$D = \frac{Data\_Value}{2^N}$$

where Data_Value is the input data word integervalue If an 8-bit input is used, then the duty cycle isin the range $0 \le D \le \frac{255}{256} = 99.6\%$

Since the PWM duty cycle has 2^N different states, the generator resolution, α , is defined as

$$\alpha = \frac{1}{2^N}.100\%$$

In order to achieve high PWM frequencies, resulting in high clock rates, a fast counter is required.

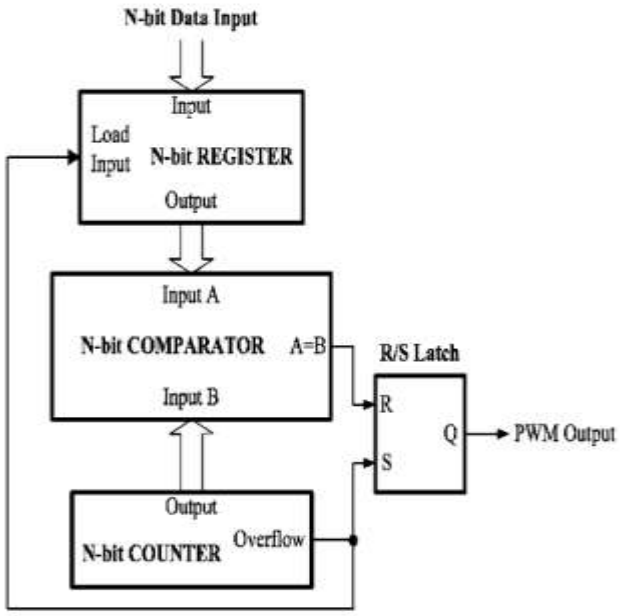

Figure 2: Block Diagram of the proposed PWM Generator.

4. Simulation Results

A software program using the VHDL languagewas developed, for synthesizing the architecture presented in the previous section, using the Xilinx ISE Design Suite 13.1 software. The FPGA or CPLD device type is selected according to the digital control system implementation area and cost requirements.

The result of each block in fig.2 is shown in form of waveforms in fig 3,4,5,6.

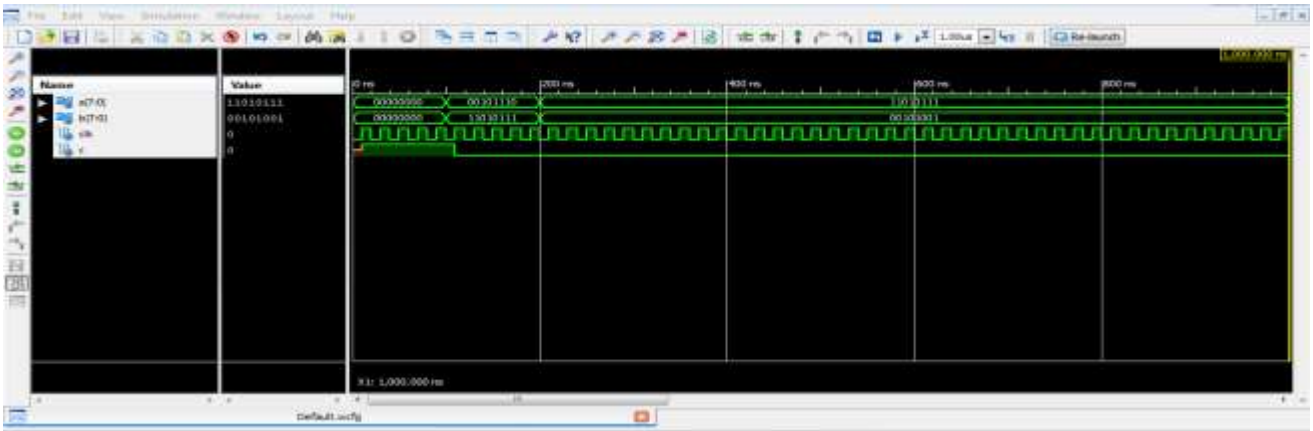

Figure 3: Waveform of comparator

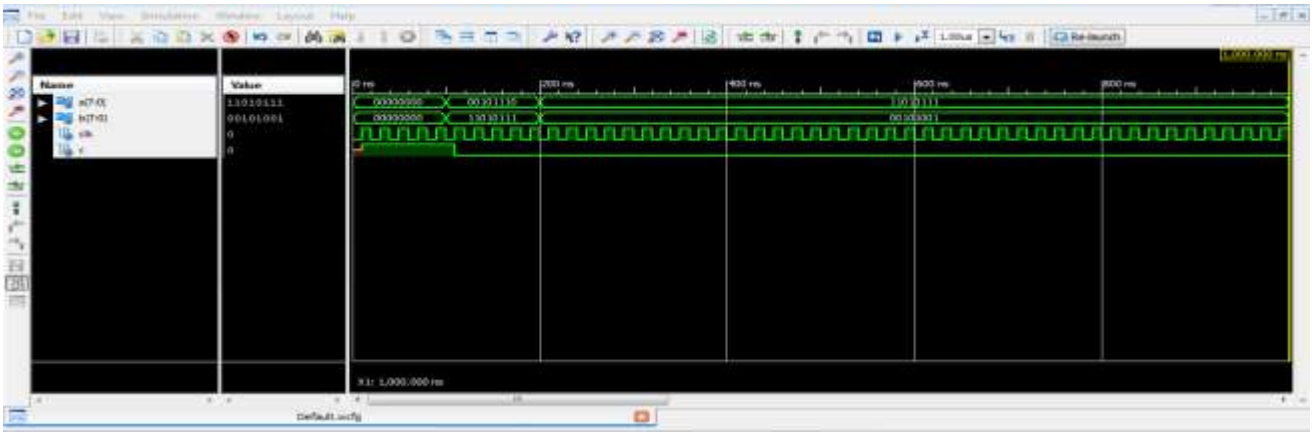

Figure4: Waveform of Register

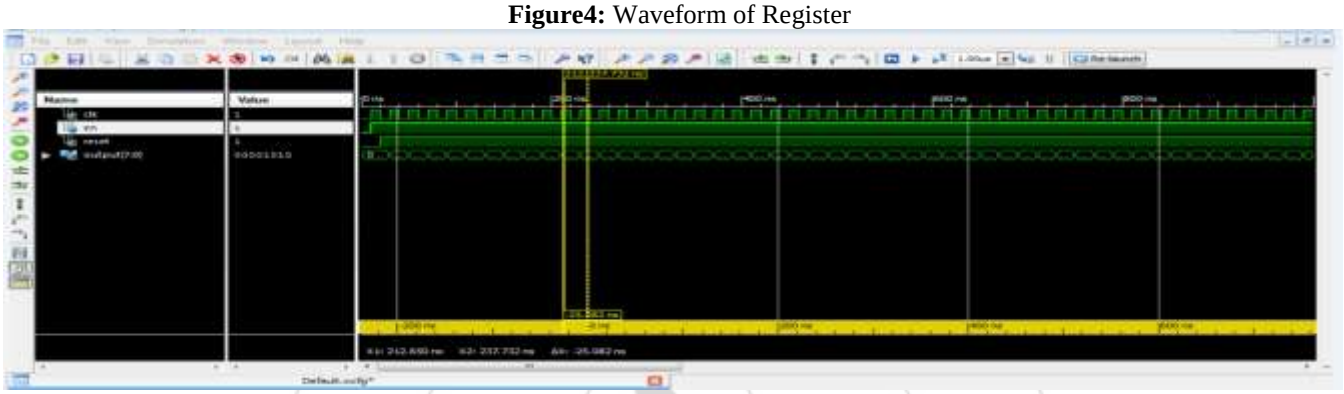

Figure 5: Waveform of counter

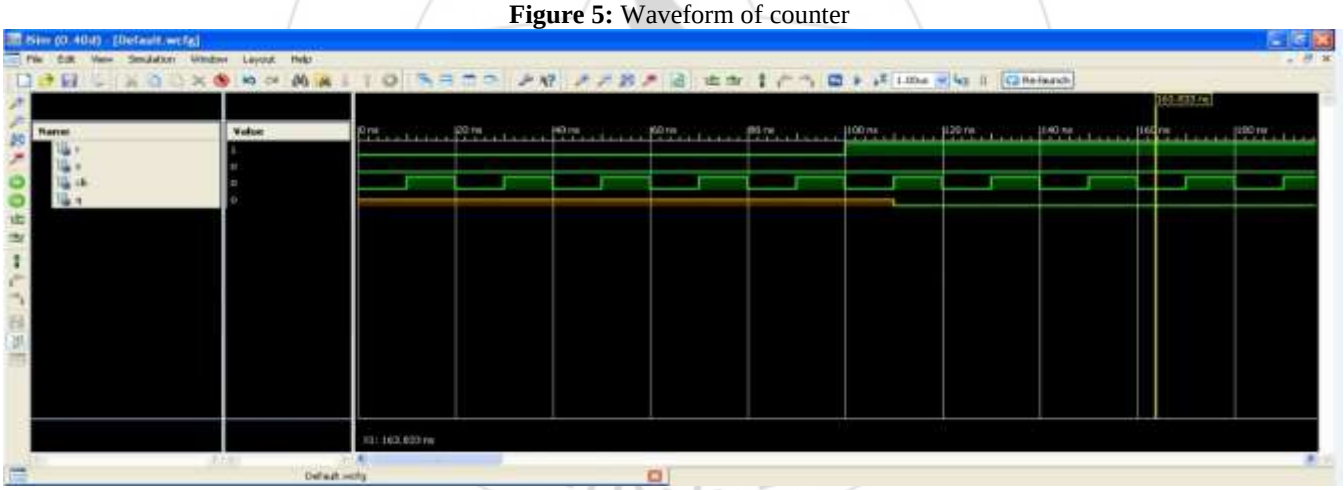

Figure 6: Waveform of R S Latch

From fig.3, the N-bit register output, containing the N-bit data input, is compared with the output value of an N-bit counter, by means of a comparator. When these two values become equal, the comparator output is used to reset the R/S latch output which produces the PWM wave

From fig.4, register stores the input to be processed .So when load signal is '1' the register provides input to output.

From fig.5, counter used is 8 bit up-counter.

From fig.6, R S latch is used to set or reset the output. When 'r' signal is '1' output is reset to '0'.When's' signal is '1' output is set to '1'.

5. Conclusions

In this paper, high-frequency PWM generator architecture for power converter control, using FPGA and CPLD ICs, has been presented. The resulting PWM frequency depends on the target FPGA or CPLD device speed grade and the duty cycle resolution required. The selection of the target device depends on the system cost and resolution requirements.

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Author Profile

Sneha Kirnapure received her B.E. in Electronics from R.C.E.R.T., Chandrapur, India in 2009.Currently she is pursuing M.Tech in Electronics from A.C.E., Wardha, India.

Prof. Vijay R. Wadhankar receivedhis B.E. in Electronics from B.D.C.O.E., Wardha, India and M.Tech in VLSI from G. H. Raisoni College, Nagpur, India. He is working as Head of Dept. in A.C.E., Wardha, India.