



Figure 3: Schematic view of Level 1 trigger system

At the same time, real detector data recorded that can be computationally regenerated are also read as input. These inputs will be read and processed to find other relevant information like angle of hit, centroid of hit etc. These will be then processed to find the output that the FPGA processor expects.

The FPGA takes the input as binary at each clock tick. VMM is measuring Time Over Threshold (TOT). Each clock signal is 5ns and for each clock if the value is high i.e. above a threshold the signal will count high and in all other case low. So the output will be having only 0s and 1s for low and high respectively. In each clock a bit of all the pad and strips set will be outputted.

5. Methodology

To test the FPGA trigger processor the input that processor accept should be fed into the processor input track. The processor input is a Gaussian like pattern generated from the signals that the strip and the pad get when the particle hit on them. While creating pattern it is done for both real time data and simulation.

For the real time data the charge response of the detector will be stored in files. In the case of real time data only the relevant data is stored. Since there are 4 pad layers, 2 even layer and 2 odd layer, in a quadruplet there are four pad files. The overlapping area of even and odd layer is called a tower. There will be 64 strips running out of a pad layer. The strips will be running horizontally to these pads. The signals greater than a threshold value is accepted and for those signals pattern is created by putting 1 for the bits corresponding to signal position.

In the case of simulation file the data created by simulation is a digitalized file. From the digitalized RDO data, this is a root file and gives the response of the detector as charge on the detector. The event reading in this uses the TFile concept in ROOT to read and store the data. To store large quantities of same-class objects, some methods that can access and handle large quantity data at same time should be used. The TTree in ROOT is optimized to reduce disk space and enhance access speed. It can handle large amount of data at same time and in a single line. Ttuple is a specialized kind of TTree especially for float data type.

These tuples are the response of all the points in the detector. The most challenging portion is to filter the data, since it shows the signal from the non relevant portion also. This is done by mapping the charge to the corresponding pad and the strip coordinate system. Only the portion where the pad and strip signal overlaps are read and stored for further process. Once the data are read from the digitalized file and relevant data are stored then the pattern creation for the FPGA trigger processor can be preceded like the real test beam data. In which only the value above the threshold are only taken and other are discarded. For those selected value the corresponding bit position are filled with ones and others are filled with zero.

6. Experimental Result

The input for the FPGA trigger processor is prepared in two tracks. The first track in which the real test beam data is read and stored in files. Since there are 4 pad layers four file are there. These files are read and those charge value above threshold are found. For those above threshold values the pattern is creates as per the format of the FPGA.

For the simulation the digitalized files are read and stored to TFile as tuple. The tuple help to handle data as row. Data that are read by the tuple are stored in a file and processed as in the case of real test beam data.

7. Conclusion

The Phase II up gradation of ATLAS detector which is main detector in LHC experiment in CERN to find the Higgs Particle is going to conduct. As part of this the Level 1 trigger system need to be reconstructed to remove 75 percent of the fake trigger. For that the sTGC is implemented and it consists of pads and strips. To create a new trigger algorithm FPGA processors are used. In order to develop and test these trigger algorithm test data should be fed into its input track. This data can be taken from both simulation and from data read by some program.

This paper proceeds in two track on for reading the events from test beam and other for the simulation. In the case of events from test beam, 8 files (4 for pads and 4 for strips) are read and from the 8 files input for the FPGA trigger processor is created. So there will be 4 resulting files with pattern for pads and 16 for strips, since strips has 4 band in each pad layer. Form the simulation charge for all the points in the detector are read and only the relevant points are stored and processed like the test beam data.

8. Acknowledgment

First I would like to thank God Almighty for all the blessings. I would like to place on record my deep sense of gratitude to **Dr. C.G Sukumaran Nair, Head of Department, Ms. Sudha S.K., Associate Professor, Computer Science and Engineering, SIST.** I would like to thank **Mrs. Reshmy. V. R., Associate Professor, Department of Computer Science and Engineering, SIST** for her support and guidance. A special thanks go to **Ms. Julia**

Narevicius (Engineer) for helping me and especially, the discussion with her was very much helpful for this project.

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