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VLSI Implementation of an Optical OFDM Transmitter Using 180nm Technology

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Abstract: ***Orthogonal Frequency Division Multiplexing (OFDM) is a modulation technique which is used in broadband wired and wireless communication systems because it has an effective solution to inter symbol interference and inter carrier interference. As per the latest survey, OFDM is also a promising solution for optical communication. An OFDM transmitter architecture is described in this paper and explained how it handles efficiently to achieve high speed, good performance in optical system. Even though it has been suitable for the optical system, OFDM does have drawbacks like low peak to average power ratio (PAPR) and high sensitivity to frequency and phase noise. A novel transmission technologies are intensively studied to exploit optical bandwidth more efficiently. High-speed optical transmission systems are impaired by inter channel and intra channel nonlinearities, chromatic dispersion, polarization mode dispersion and require precise dispersion compensation techniques. Narrower channel spacing is pursued to increase the transmission capacity and a novel modulation formats are investigated.***

Keywords: ASIC, Demodulation, Modulation, Multiplexing, Multicarrier Transmission, PAPR

1. Introduction

In the virtually infinite broad electromagnetic spectrum, there are only two windows that have been largely used for modern-day broadband communications. The first window spans from 100 kHz to 300 GHz in frequency and the second window lies from 30 THz to 300 THz in frequency. Applications using in our daily lives is provided by the first window, including TV and radio broadcasting, wireless local area networks (LANs), and mobile phones. These applications offer the first meter or first mile access of the information networks to the end user with broadband connectivity or the mobility in the case of the wireless systems. Most of the data rates are capped below gigabit per second (Gb/s) primarily due to the lack of the available spectrum in the RF microwave range. Due to the enormous bandwidth over several terahertz (THz) in the 2nd window, the lightwave systems can provide a staggering capacity of 100 Tb/s and beyond. The optical communication systems, or fiber-optic systems, have become indispensable as the backbone of the modern-day information infrastructure. There has been a worldwide campaign in the past decade to push the fiber ever closer to the home. Despite the fact that the Internet "bubble" fizzled out in the early 2000s, Internet traffic has been increasing at an astounding rate of 75% per year.[1], [2] The new emerging video-centric applications such as IPTV will continue to put pressure on the underlying information infrastructure.

In Radio Frequency domain, OFDM has emerged as the leading modulation technique, and it has evolved into a fast-progressing and vibrant field. It has been triumphant in almost every major communication standard, including wireless LAN (IEEE 802.11 a/g, also known as Wi-Fi), digital video and audio standards (DAV/DAB), and digital subscriber loop (DSL). It is not surprising that the two competing fourth-generation (4G) mobile network standards, Worldwide interoperability for Microwave Access (WiMAX, or IEEE 802.16) from the computing community and Long-Term Evolution (LTE) from the telecommunication community, both have adopted OFDM as the core of their physical interface. Although the arrival of optical OFDM has been quite recent, it does inherit the major controversy that has lingered more than a decade in the wireless community—the debate about the supremacy of single-carrier or multicarrier transmission. It has been claimed that OFDM is advantageous with regard to computation efficiency due to the use of fast Fourier Transform (FFT), but the single carrier that incorporates cyclic prefix based on blocked transmission can achieve the same purpose. Perhaps the advantage of the OFDM has to do with the two unique features that are intrinsic to multicarrier modulation. The first is scalable spectrum partitioning from individual subcarriers to a sub-band and the entire OFDM spectrum, which provides tremendous flexibility in either device-, or subsystem-, or system-level design compared to single-carrier transmission. The second is the adaptation of pilot subcarriers simultaneously with the data carriers enabling rapid and convenient ways for channel and phase estimation.

2. Research Motivation

OFDM is using the Multicarrier Transmission (MCT) the basic principle behind the MCT is to split the transmission bandwidth into a number of narrow sub-channels which are transmitted in parallel. Each sub-channel is narrow so that it experiences a flat-fading spectrum. At the same time, as the symbol duration increases it has less significant effect on the time dispersion. In order to achieve the orthogonality between the sub-carriers, it should satisfy two conditions i) Each subcarrier has exactly an integer number of cycles in the FFT interval. ii) The number of cycles between adjacent subcarriers differs by exactly one.

Optical OFDM bears both similarities to and differences from the RF counterpart. Optical OFDM suffers from two well-known problems, namely high peak-to-average power ratio (PAPR) and sensitivity to phase /frequency noise. On the other hand, the optical channel has its own unique set of problems. One of the prominent differences is the existence of fiber channel nonlinearity and its intricate interaction with

fiber dispersion, which is nonexistent in the RF systems. Furthermore, in the RF systems, the main nonlinearity occurs in the RF power amplifier, where a bandpass filter cannot be used to cut off the out-of-band leakage due to unacceptable filter loss. However, in optical OFDM systems, the erbium doped fiber amplifier (EDFA; by far the most prevalent optical amplifier) is perfectly linear regardless of the level of saturation, and it is usually accompanied by a wavelength multiplexor that can remove the out-of-band spectral leakage.

3. Tools Used

For simulating the verilog code, Modelsim Altera6.3g is used and for synthesizing the design, Cadence RTL compiler v9.10 is used. Cadence SOC Encounter is used for layout extraction of the complete design.

4. Archetecture

OFDM is a special case of multicarrier transmission in which a single information-bearing stream is transmitted over many lower rate sub-channels. Using Fast Fourier Transform (FFT), OFDM offers good spectral efficiency and efficient elimination of sub-channel and symbol interference for modulation and demodulation, which does not require any type of equalization. These features and its high immunity to dispersion and burst-errors make OFDM an intriguing candidate for long-haul optical transmission.

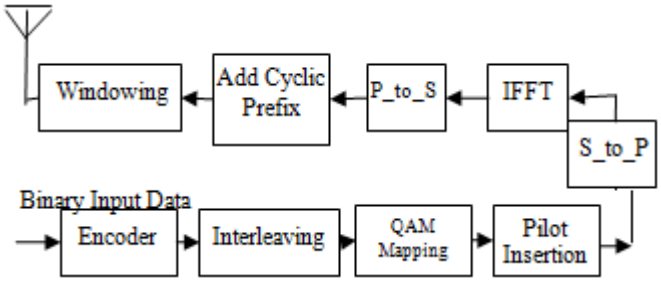

Figure 1: Architecture of an Optical OFDM Transmitter

Fig 1 shows the architecture of an optical OFDM transmitter, In the transmitter side, the binary input data is encoded by a convolutional encoder. An interleaving process is done, and the binary values are converted to QAM values. Few pilot values are added to each data values, resulting in QAM values for each OFDM symbol. The symbol is modulated onto subcarriers by applying the Inverse Fast Fourier Transform (IFFT). The output is converted to serial and a cyclic extension is added to make the system robust to multipath propagation. Windowing is applied after to get a narrower output spectrum. The signal is converted to analog using an IQ modulator, which is upconverted to the 5 GHz band, amplified, and transmitted through the antenna.

5. Implementation

For VLSI or hardware implementation there are two different methodologies. They are ASIC design and FPGA design. For ASIC design the architecture is modeled in VERILOG HDL and the functional simulation is done in MODELSIM, synthesis is carried out in CADENCE RTL COMPILER and the physical design is carried out in CADENCE SOC ENCOUNTER. Following sections describe the implementation methodology and results obtained in ASIC and FPGA.

a) ASIC Design Methodology

Application Specific Integrated Circuit (ASIC) Design, as the name suggests this design focuses on the development of a hardware module which is completely dedicated to a particular application or process. This type of design helps in the economical usage of silicon and also has a good speed compared to the other implementations such as FPGA and CPLD devices. ASIC design flow is as follows.

b) System Partitioning.

This is the first step of the ASIC design flow; here the complex problem statement is decomposed into smaller subsystems. The decomposition is carried out hierarchically until each subsystem is of manageable size.

c) Design Entry.

In any design, specifications are written first abstractly describing the functionality, interface and overall architecture of the circuit. A behavioral description is then created to analyze the design in terms of functionality, compliance to standards, and other high-level issues. Typically behavioral (simulation model) descriptions are created in HDLs. In this paper VERILOG HDL is used for design entry.

d) Simulation

Simulation is carried out at this stage for the written code and this type of simulation is called as behavioral simulation or functional simulation. Here, the simulation is carried out by the help of "testbench", testbench is a piece of code which provide the required stimulus or inputs and control signals to the design, by observing the outputs in a waveform the functionality is confirmed. In this paper, MOELSIM simulator is used for functional simulation.

e) Synthesis

Synthesis means converting the written code into gates and its interconnections. In this stage the conversion of the codes into gates and interconnections is done by mapping to a particular technology i.e., either 0.35µm technology or 0.18µm technology or 90nm technology. The technology here refers to the gate length of the transistors used in this design. The output of this synthesis stage is the "gate level netlist (.v)" and "design constraints (.sdc)" files. Gate level netlist contains information of the gates and interconnections and design constraints contain the information such as the clock frequency, wire-load models used. This is the final stage of the logical flow or the front-end flow. The output files i.e., .v and .sdc are taken as input to the physical or backend flow. In this project TSMC 0.18µm, TSMC 90nm technologies are used also Cadence RTL Compiler is used for synthesis.

f) Floor Planning

This is first step of physical design flow or the backend flow. In this phase sizes is estimated and set the initial relative locations of the various blocks in the ASIC. The floor plan is a physical description of an ASIC. The input to the floor planning tool is the hierarchical netlist from a logic synthesis tool. The goals of floor planning are,

arrange the blocks (flexible and fixed) on a chip, decide the location of the I/O pads, and decide the location and number of power pads, decide the type of power distribution. Its objective is to minimize the chip area and minimize interconnect delay in particular. For physical design flow we used Cadence SOC Encounter tool.

g) Placement

The goal of the placement tool is to arrange all the Standard Cells within the chip. Most commonly used placement objectives are; Minimize the total estimated interconnect length. For critical nets, meet the timing requirements. Minimize the interconnect congestion. Placement is done with the help of CAD algorithms which are the integral part of the tool. Right after the placement the timing check is run to see whether the placed design is meeting timing requirements or not. If not the placement is done again till it meets the timing. This timing analysis is called Static Timing Analysis (STA).

h) Routing

After the placement of standard cells we perform the routing. Routing is of 2 types. 1) power routing, clock routing where the power rails and stripes are routed from the placed standard cells and the clock is routed in an efficient way so as to minimize the skew. 2) Signal routing where the interconnections between the standard cells in the design are routed. The goals of routing algorithms are 100% connectivity of the design, minimization of area and wire length. Now, the final timing check is performed i.e., STA and the optimized routed design is finalized.

i) Extraction

This is the final part of the ASIC flow. From the routed design, the required parameters are extracted here. The parasitic capacitance and resistance associated with each interconnect, via and contact can be calculated. A circuit-extraction tool generates the above data in a standard format called standard parasitic format (SPF). For interconnect delay a file called Standard Delay Format (SDF) is generated. Now, the design rule check (DRC) is performed to check whether the design is obeying layout rules. Subsequently, an Electrical Rule Check (ERC) examines conditions like maximum permitted fan-out, shorts of VDD to ground etc. Lastly, the Layout versus Schematic (LVS) verifies that the logic derived from the physical layout agrees with the logic of the netlist. Finally the physical information of the optimized routed design is stored in Graphical Data Stream (GDS II) file which contains the information on masks for the fabrication of the IC.

6. Results

This section describes the simulation results of various important modules of the design.

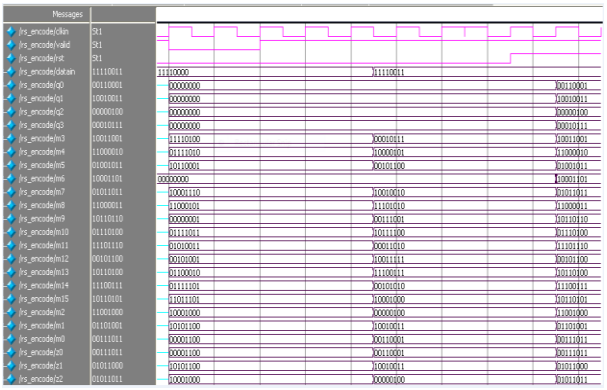

Figure 2: RS Encoder Simulation Results

Fig. 2 shows waveform of the simulation results of the RS Encoder module. The binary values are encoded to ½ to increase the data rate. Reed-Solomon codes are calculated in a finite field of elements, or Galois fields GF(2m). The Galois field is defined by a primitive polynomial P(x). The degree of the primitive polynomial m defines the number of bits per data symbol (m = bits per symbol) and the maximum length of the Codeword (2m-1=maximum Codeword length n). The generator polynomial G(x) further defines the field of Code words that the parity symbols are derived from. The logic symbol of this core is shown in Fig 3.

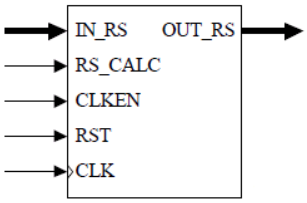

Figure 3: Logical Symbol of RS Encoder

The Reed-Solomon encoder core is partitioned into modules as shown in Fig 4.

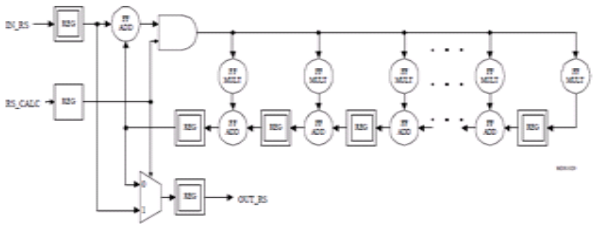

Figure 4: Block Diagram of RS Encoder

In fig 4, all registers are driven by common clock (CLK), clock enable (CLKEN), and asynchronous reset (RST) signals. This provides ultimate flexibility in integration of the core into larger systems. The registers are clocked on the rising edge of CLK, enabled by a high on CLKEN, and asynchronously reset by a high on RST.

The RS_CALC signal controls whether the core is calculating the parity (high) or shifting out the calculated parity (low). Logic external to the core is required to generate this control signal. This allows the user to vary the message block length as desired for shortened codes. The RS_CALC pin must be held at a low for 2t enabled clock cycles to ensure all parity register values are shifted out and the registers are cleared.

FFADD Blocks perform modulo 2 addition of the input symbols.

FFMULT Blocks perform a finite field multiplication, over the Galois field, of a constant and the input symbol.

Various forms of the core have been developed. One supports high data rates where area is a secondary concern. Another supports low data rates where a high-speed system clock is available and area is a primary concern. The cores work for any valid codeword length and can be customized to support either fixed or variable values of parity symbols. The core has been developed in two different approaches. One approach is optimized for encoders with a single value of t. The other approach is optimized for encoders with selectable values of t.

The RSENC-INTELSAT is a pre-customized core that calculates a selectable 14, 16, 18, or 20 parity symbols (t = 7, 8, 9, or 10) and is compliant with the IESS-308 Intelsat standard. The primitive polynomial and generator polynomial implemented is P(x)= x8+x7+x2+x+1 and G(x)= (x-a120)(x-a121)…(x-a119+2t) over a Galois field of GF(256). A 2-bit input control signal selects between four different codeword/message lengths: RS(126,112), RS(194,178), RS(219,201), and RS(225,205). The RSENC-INTELSAT core is delivered as Verilog RTL source code. The RSENC-DVB is a pre-customized core that calculates 16 parity symbols and is compliant with the DVB standard. The primitive polynomial and generator polynomial implemented is P(x) = x8+x4+x3+x2+1 and G(x)=(x-a0)(x-a1)…(x -a15) over a Galois field of GF(256). The core is adaptable to any message/codeword length RS (n,k) where n-k=16. Thus, the largest code supported by this core is RS (255,239). The DVB standards specify a code of RS (204,188).

Table 1: RS Encoder Parameters

Parameter	Symbol	DVB
Primitive Polynomial	P(x)	$x^8 + x^4 + x^3 + x^2 + 1$
Generator Polynomial	G(x)	$(x-\alpha^0)(x-\alpha^1)(x-\alpha^2)(x-\alpha^3)\ldots(x-\alpha^{15})$
Bits per symbol	m	8
Codeword Length	n	204 (Note 1)
Message Word Length	k	188
Parity Symbols (n-k)	2t	16

Notes:
1. Core is adaptable to any RS (n,k) where n-k=16 and largest code being RS(255,239).
2. Selected by 2-bit input control signal for RS(126,112), RS(194,178), RS(219,201), and RS(225,205).

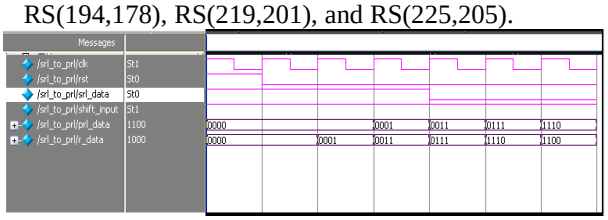

Figure 5: Serial to parallel simulation results

Fig. 5 shows waveform of the simulation results of the Serial to Parallel module. It will convert the serial binary data into parallel.

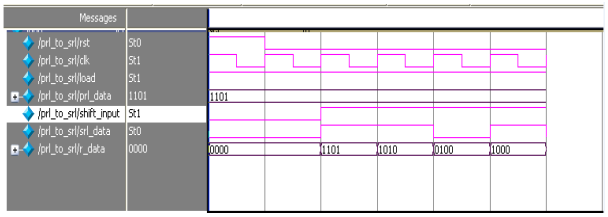

Figure 6: Parallel to Serial simulation results

Fig. 6 shows waveform of the simulation results of the Parallel to Serial module. It will convert the parallel data to serial.

Fig. 7 shows waveform of the simulation results of the cyclic prefix.

Two different sources of interference can be identified in the OFDM system- 1) Inter symbol interference (ISI) is defined as the crosstalk between signals within the same sub-channel of consecutive FFT frames, which are separated in time by the signaling interval T and 2) Inter-carrier interference (ICI), the crosstalk between adjacent sub channels or frequency bands of the same FFT frame.

For the purpose to eliminate the effect of ISI and to combat against multipath fading, the guard interval (or cyclic prefix) is used in OFDM systems. The following condition should be satisfied:

T_G: Guard interval

$T_{\text{delay spread}}$: multi path delay spread

$$T_G > T_{\text{delay spread}} \quad (1)$$

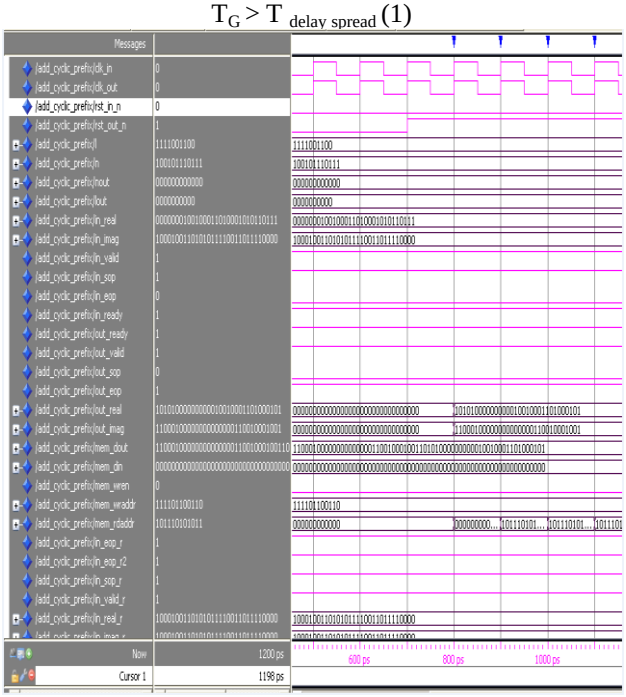

Figure 7: Cyclic Prefix Simulation Results

In that case, however, the problem of inter carrier interference (ICI) would arise as shown in Fig 8. To eliminate ICI, the OFDM symbol is cyclically extended in the guard interval. A part of the symbol is copied and appended at the beginning of the symbol which acts as guard

as shown in Fig 9. This ensures that delayed replicas of the OFDM symbol always have an integer number of cycles within the FFT interval, as long as the delay is smaller than the guard interval.

OFDM is so widely used because, when a CP is used, any distortion caused by a linear dispersive channel can be corrected simply using a 'single-tap' equalizer. To understand why this is true, consider a simple case where there is perfect upconversion and down conversion, but where the received baseband signal is the sum of two versions of the transmitted signal with different gains and delay.

$$y(t) = g_1x(t+\tau_1) + g_2x(t+\tau_2) \quad (2)$$

For the case where OFDM transmission is at pass band, the gains and the signals will be complex; for the case of baseband transmission the gains and signals are real. Inter symbol interference could also be eliminated by preceding each OFDM symbol with a guard interval in which no signal was transmitted, however this would result in a phenomenon called inter carrier interference (ICI).

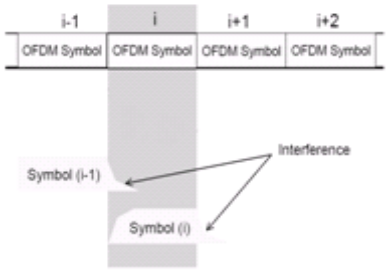

Figure 8: Inter Carrier Interference

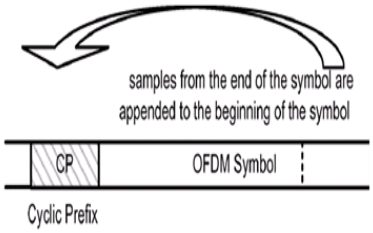

Figure 9: Insertion of Cyclic Prefix

When a CP is used, each OFDM subcarrier is represented by a continuous sinusoid of the appropriate frequency throughout the main symbol period and the associated CP. This is shown in Fig.10.

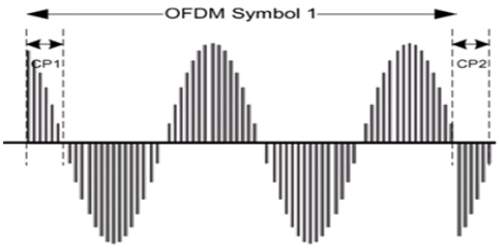

Figure 10: Time Domain of One Symbol with Cyclic Prefix

Further advantage can be obtained by using more than two bands. The required CP is simply the CP duration of a single band's CP, divided by the number of bands. The relative delay between two adjacent bands should equal the CP for each band, and should be calculated from the fiber's dispersion map. Some tolerance to dispersion variations could be obtained by overlapping the CPs of the bands.

A. *Synthesis Results*

This section consists of the synthesis results of the design codes in Cadence RTL Compiler.

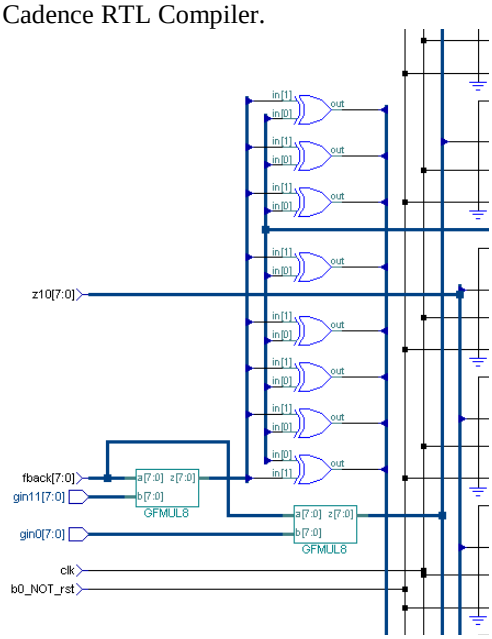

Figure 11: Schematic of OFDM

Figure 11: shows the schematic layout obtained in cadence.

B. *Cadence SOC Encounter*

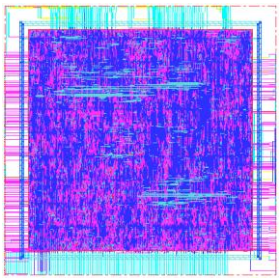

Figure 12: OFDM Layout

Figure 12: shows OFDM layout after Placement and Routing.

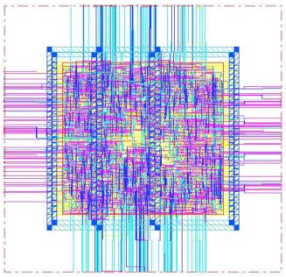

Figure 13: RF Encoder Layout

Fig. 13 shows RF Encoder layout after Placement and Routing

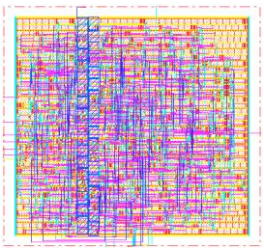

Figure 14: Interleaver Layout

Fig.14 shows Inter leaver layout after Placement and Routing.

7. Conclusion and Future Enhancement

In this paper, a general architecture for an optical OFDM transmitter is proposed. Main idea behind is, to optimize the each and every module of an optical OFDM transmitter. The design is implemented using Verilog HDL and simulated with the help of Modelsim and Cadence NCsim. Synthesis is done by using RTL Compiler and physically designed with SoC Encounter, with the proposed novel architecture, and thus the Optical OFDM transmitters have been demonstrated successfully for 21.4 Gbits/s. The transmitter is potentially capable of supporting much higher data rates, when it uses the higher modulation formats. Area, power, timing, SDC, netlists are found for each and every module of the OFDM transmitter individually. By using the SDC, netlist in the SoC encounter design flow, I obtained the layout for RS encoder, Interleaver and OFDM modules.

The OFDM transmitter is potentially capable of supporting much higher data rates, when it uses the higher modulation formats. Area, power, timing, SDC, netlists are found for each and every module of the OFDM transmitter individually. Optical OFDM transmission has become a fast progressing and vibrant research field in optical fiber communications. Last few years saw experimental demonstrations up to 1 Tb s_1 transmissions, together with rapid advance in real-time demonstrations. With the standardization of 100GbE and prospect of emergence of the Tb/s era, much excitement is growing in the optical communications community for the application of OFDM, the modulation format of choice in RF wireless communications. The introduction of OFDM without doubt has great potential and promise in bringing about the next-generation optical networks that possess high degree of flexibility and scalability. In the meantime, the research in optical OFDM also presents tremendous challenges and opportunities in the areas of novel DSP algorithms, high-speed electronic and photonic integrated circuits.

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