

Complementary Metal-Oxide Semiconductor: A Review

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Abstract: In this paper we have focused on the complementary metal-oxide semiconductor technology. This paper covers overview of power consumption sources and discusses the techniques for reduction of power dissipation in high performance designs. Power dissipation is very serious matter in CMOS technology. The first section contains introduction, second section contains review of CMOS, third section contains overview of power consumption sources and leakage current mechanisms, fourth section contains techniques to reduce power dissipation, and the last section presents the conclusion and references.

Keywords: CMOS structure, Power consumption, Leakage currents, VTCMOS, MTCMOS

1. Introduction

The persistent development of electronics, information technology (IT), and communications has been mainly enabled by nonstop development in silicon-based complementary metal-oxide-semiconductor (CMOS) technology. This non-stop development has been maintained frequently by its dimensional scaling, that results in exponential development in both gadget compactness and production. The decrease in cost-per-function has gradually been increasing the financial efficiency with all new technology generation. Today CMOS ICs are random and indispensable in our life, ranging from moveable electronics to telecommunications and transportation. [3] Now a days VLSI, a key challenge and critical matter in electronics industry is control and management of power consumption. Power consumption is the main problem in VLSI design.[2]. Too much power dissipation in IC's discouraging their use in convenient systems. Much power causes overheating, and decreases the performance and reduces chip natural life.[1] CMOS technology, the supply voltage and threshold voltage had been scaled down to attain quicker performance devices [4]. But leakage current have Increased significantly and have become a major component of the total power consumption [5]. In CMOS design the sources of power consumption mainly due to dynamic power dissipation and leakage power dissipation.

Leakage power dissipation is the power dissipated by the circuit when the circuit is in sleep mode. Leakage power is given by this equation.[6]

$$P_{leak} = I_{leak} * V_{dd}$$

So, I_{leak} is the leakage current that is flows in a transistor when the transistor is in off state, V_{dd} is the supply voltage.

Dynamic power dissipation is the power dissipated by the circuit, when the circuit is switching and it is done due to the charging and discharging of capacitor.

$$P_{dynamic} = \alpha f C V_{dd}^2$$

So, α is the switching activity. f is the operating frequency, C is the load capacitance, V_{dd} is the Supply voltage. Low power design critical technology needed in the Semiconductor in-

dustry today. Simultaneously, we also need to speed up the critical paths of the circuit, while reducing its power consumption [1].

2. CMOS Technology Review

The concept of cmos was introduced in 1963 by FRANK WANLASS AND CHIN-TANG SHAN OF FAIRCHILD.

In CMOS (complementary metal oxide semiconductor) technology both kinds of transistors are used.

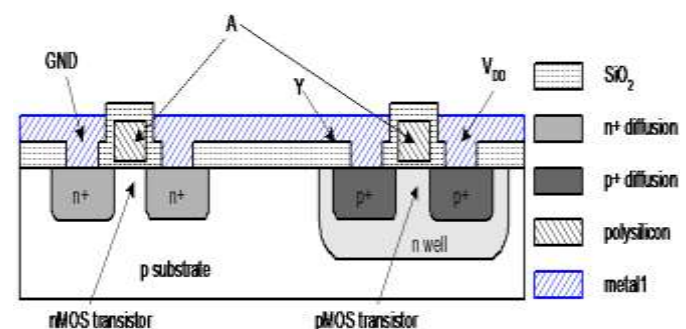


Figure 1: CMOS structure

CMOS is made up of two transistor NMOS and PMOS transistor. P-channel MOSFET and N-channel MOSFET in a complementary way on the same substrate. The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion; N+ diffusion for the N device & P+ diffusion for the P device (illustrated in fig1). The output ("out") is connected together in metal (illustrated in fig1). Connections between metal and polysilicon or diffusion are made through contacts and these contacts called source, drain and gate point. complete CMOS structure are shown below.

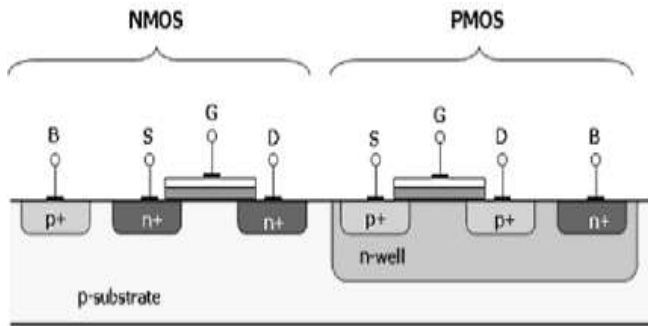


Figure 2: CMOS N-well structure

Besides, CMOS technology is used in the fabrication of conventional microchip. .since it is less expensive than BiCMOS and SOI technologies and offers high performance, high density and low-power dissipation .CMOS reduce complexity of circuit. because in this CMOS two transistor are fabricated on a single chip. CMOS used in logic circuit design. Switching speed is faster as compare to other logic families. CMOS structure is ratio less .because output of CMOS is not depends upon the transistor size.[7]

2.1. CMOS - based logic circuit

As the time passed, the advancements in CMOS were also done. Later on it was used for logic gates like inverter, AND gate, NAND gate, NOR gate etc. It is also used in the designing of SRAM cells. A new logic called ternary logic is also developed. Ternary logic design functions are used in CMOS. The main advantage of it is that it reduces the number of computational steps required.[8] To evaluate the performance of a CMOS, various simulation models have been proposed. The CMOS tanner tool model is widely used in circuit design and simulation.

Using this Eda tanner tool 14.1 version 32 bit , we can draw the circuit design in s-edit of tanner tool of CMOS as a inverter using 32nm,45nm,90nm CMOS technology and Model parameters are extracted from BSIM4.6.1 user manual [10]. These windows are given below.

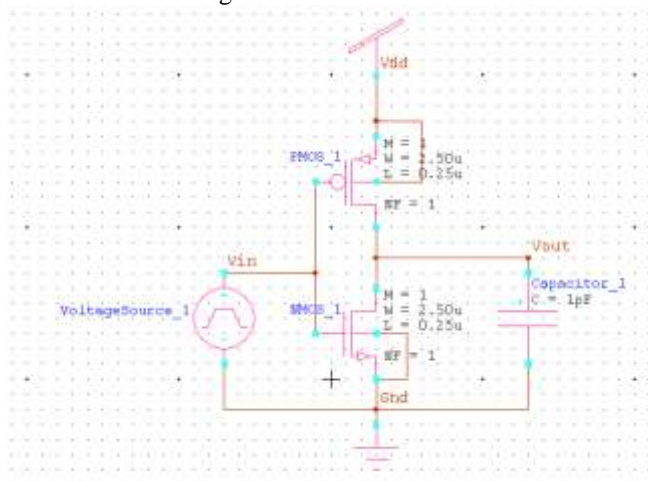


Figure 3: Schematic diagram of CMOS Inverter [11]

This fig.3 shows the snapshot of CMOS inverter which is taken from EDA Tanner simulation tool.

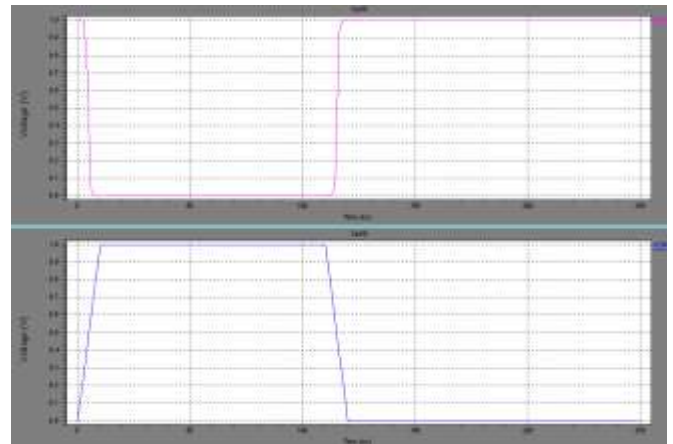


Figure 4: Transient Characteristics of CMOS Inverter [11]

Transient response of CMOS inverter is showing in Fig-4 i.e. input and output waveform w.r.t time in ns.[11]

3. Overview of Power Consumption Sources

The average power consumption in conventional CMOS digital circuits can be expressed as the sum of three main components (i) dynamic (switching) power consumption (ii) short-circuit power consumption(iii) Leakage power consumption.

Dynamic power consumption: This represents the power dissipated during a switching. This power depends upon the charging and discharging of capacitor.

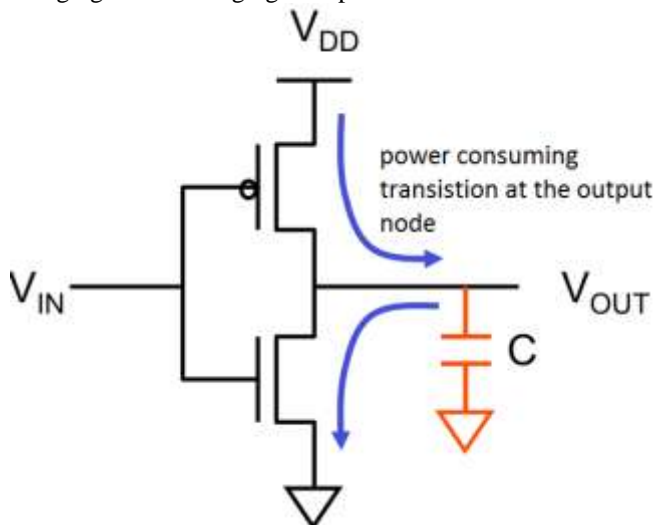


Figure 5: CMOS logic gate for dynamic power calculation

This transition can be represented by PMOS and NMOS networks. The average power dissipation of the CMOS logic gate, driven by a periodic input voltage waveform with ideally zero rise-time and fall-times, can be calculated from the energy required to charge up the output node 0 to V_{dd} and charge down the total output load capacitance to ground level.

$$P_{avg} = 1/TC_{load} V_{dd}^2$$

$$P_{avg} = C_{load} V_{dd}^2 F_{clk}$$

So, F is the operating frequency, C is the load capacitance, V_{dd} is the supply voltage. Note that the average switching power dissipation of a CMOS gate is essentially independent

of all transistor characteristics and transistor sizes as long as a full voltage swing is achieved. [12]

Short circuit power consumption: CMOS inverter (or a logic gate) is driven with input voltage waveforms with finite rise and fall times, both the NMOS and the PMOS transistors in the circuit may conduct *simultaneously* for a short amount of time during switching, forming a ground, as shown in fig.5

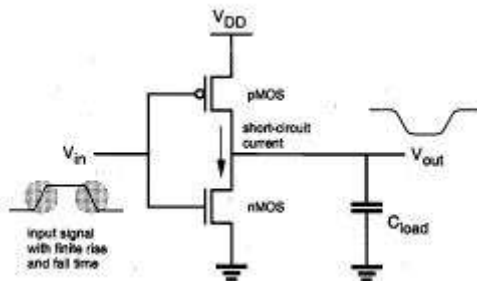


Figure 6: NMOS and PMOS transistor conduct (simultaneously) a short circuit current during switching [12]

The current component which passes through both the NMOS and the PMOS devices during switching does not contribute to the charging of the capacitances in the circuit, and hence, it is called the *short-circuit current* component. For a simple analysis consider a symmetric CMOS inverter with $K_n=K_p=K$ and $V_{T,n}=|V_{T,p}|=V_T$, and with a very small capacitive load. If the inverter voltage waveform with equal rise and fall times ($T_{rise}=T_{fall}=T$), time-averaged short circuit current drawn from the power supply is

$$I_{avg}(\text{short-circuit}) = 1/12 K^*T^*F_{clk}/V_{dd}(V_{dd}-2V_T)^3$$

Hence, the short-circuit power dissipation becomes,

$$P_{avg}(\text{short-circuit}) = 1/12 K^*T^*F_{clk}(V_{dd}-2V_T)^3$$

The short-circuit power dissipation is linearly proportional to the input signal rise and fall times, and also to the Trans conductance of the transistors. Hence, reducing the input transition times will decrease short-circuit current component.

Leakage power consumption: power leakage consumption is due to the leakage current. This power is done at that time when the transistor is in sleep mode.

$$P_{leak} = I_{leak} * V_{dd}$$

So, I_{leak} is the leakage current that is flows in a transistor when the transistor is in off state, V_{dd} is the supply voltage.

3.1. Mechanism of Leakage Currents

There are four main sources of leakage current in MOS transistor as shown in Fig.6 which may leads leakage power dissipation.

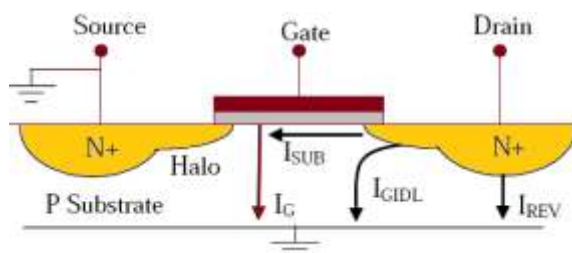


Figure 7: Leakage current in CMOS transistor [2]

Reverse junction leakage current (I_{REV}): I_{REV} is the reverse-bias PN junction leakage. A reverse bias PN junction leakage I_{REV} has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction.[1]

$$I_{REV LEAKAG} = I_S * (e^{(V_{dd}/V_{th})} - 1)$$

Here I_S is the reverse saturation current, V_{dd} is the voltage

Bias, and $V_{th}=kt/q$ is the thermal voltage. For engineering purposes, we can assume that the reverse leakage current is equal to the leakage current is equal to the reverse saturation current. The reverse saturation current is given by:

$$I_S = q n_i^2 A (D_p/N_d W_n + D_n/N_a W_p)$$

Where q is electron charge the intrinsic concentration, A is area of PN junction diode (actually drain area), D_p and D_n are the electron and hole diffusion coefficient, N_d and N_a are the donor and acceptor concentration, W_p and W_n are the width of P and N side of PN junction diode.[1]

Gate leakage tunneling current (I_G): I_G is the oxide tunneling current; Reduction of gate oxide thickness due to this an increase in the field across the oxide. The high electric field coupled with low oxide thickness in tunneling of electrons from substrate to gate and also from gate to substrate through the gate oxide, that is the gate oxide tunneling current.

Gate induced drain leakage (I_{GIDL}): The gate induced drain leakage is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at V_{dd} , significant band bending in the drain allows electron-hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current. Transistor scaling has led to increasingly steep *halo* implants, where the substrate doping at the junction interfaces is increased, while the channel doping is low. This is done mainly to control punch-through and drain-induced barrier lowering while having a low impact on the carrier mobility in the channel. The resulting steep doping profile at the drain edge increases band to band tunneling currents there, particularly as V_{db} is increased. Thinner oxide and higher supply voltage increase GIDL current.[9]

Sub threshold leakage current (I_{SUB}): The sub threshold current, this is due to carrier diffusion between the source and the drain regions of the transistor in weak inversion. The behavior of an MOS transistor in the sub threshold operating region is similar to a bipolar device, and the sub threshold current exhibits an exponential dependence on the gate voltage. The amount of the sub threshold current may become significant when the gate-to-source voltage is smaller than, but very close to, the threshold voltage of the device. In this case, the power dissipation due to sub threshold leakage can become comparable in magnitude to the switching power dissipation of the circuit. In current CMOS technologies, the sub threshold leakage current, I_{SUB} , is much larger than the other leakage current components. This is mainly because of

the relatively low V_T in modern CMOS devices. The source then injects carriers into the channel surface, causing an increase in I_{OFF} .

Let I_{OFF} denote the leakage of an OFF transistor ($V_{GS}=0V$ for an NMOS device.), we know that from equation 2. The I_{OFF} can be expressed:

$$I_{OFF} = I_{REV} + I_{GIDL} + I_{SUB}$$

I_{REV} and I_{GIDL} are maximized when $V_{DB} = V_{DD}$. Similarly, for short-channel devices, I_{SUB} increases with V_{DB} because of the DIBL effect. Note the I_G is not a component of the OFF current, since the transistor gate must be at a high potential with respect to the source and substrate for this current to flow.

4. Leakage reduction techniques of CMOS

Here we discuss two leakage reduction techniques. These are given below.

1. VTCMOS (Variable-threshold CMOS)
2. MTCMOS (Multiple-threshold CMOS) We have seen that using a low supply voltage (V_{dd}) and a low threshold voltage (V_t) in CMOS logic circuits is an efficient method for reducing the overall power dissipation, While maintaining high speed performance. Yet designing a CMOS logic gate entirely with low V_t transistors will inevitably lead to increased sub threshold leakage, and consequently, to higher stand-by power dissipation when the output is not switching. One possible way to overcome this problem is to *adjust* the threshold voltages of the transistors in order to avoid leakage in the stand-by mode, by changing the substrate bias.

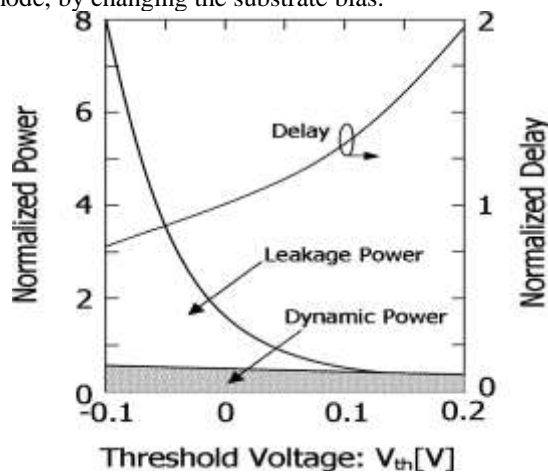
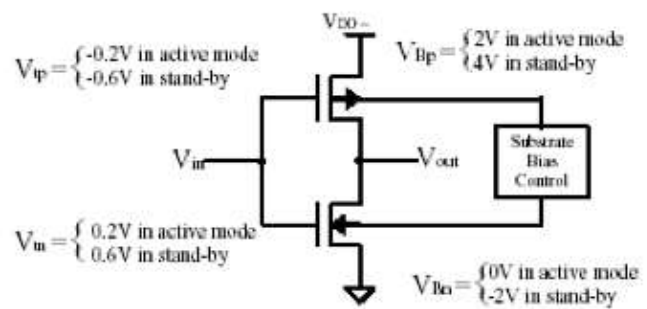


Figure 8: Power dependant on threshold voltage[1]

1)Voltage threshold CMOS circuits (VTCMOS): In VTCMOS circuit technique, the transistors are designed inherently with a low threshold voltage, and the substrate bias voltages of NMOS and PMOS transistors are generated by a variable substrate bias control circuit, as shown in Fig.8



Threshold voltages are controlled separately

Figure 9: A Variable-threshold CMOS Inverter [12]

This circuit is done in two modes

1. Active mode
2. Standby mode

In active mode the substrate bias voltage of the NMOS transistor is $V_{ON} = 0$ and the substrate bias voltage of the PMOS transistor is $V_{BP} = V_{DD}$. Thus, the inverter transistors do not experience any back gate-bias effect. The circuit operates with low V_{DD} and low V_t benefiting from both low power dissipation (due to low V_{DD}) and high switching speed (due to low V_t)

In the *standby* mode, the substrate bias control circuit generates a lower substrate bias voltage for the NMOS transistor and a higher substrate bias voltage for the PMOS transistor. As a result, the magnitudes of the threshold voltages V_{Tn} and V_{Tp} both increase in the stand-by mode, due to the back gate bias effect. Since the sub threshold leakage current drops exponentially with increasing threshold voltage, the leakage power dissipation in the stand-by mode can be significantly reduced with this technique.

The VTCMOS technique can also be used to automatically control the threshold voltages of the transistors in order to reduce leakage currents, and to compensate for process-related fluctuations of the threshold voltages. This approach is also called the Self-Adjusting Threshold-Voltage Scheme (SATS).[12]

2) Multi-threshold CMOS circuit (MTCMOS)

This is the another technique which can be applied for reducing leakage currents in low voltage circuits in the stand-by mode is based on using two different types of transistors (both NMOS and PMOS) with two different threshold voltages in the circuit. Here, low- V_T transistors are typically used to design the logic gates where switching speed is essential, whereas high- V_T transistors are used to effectively isolate the logic gates in stand-by and to prevent leakage dissipation. The circuit structure of the MTCMOS logic gate shown below.

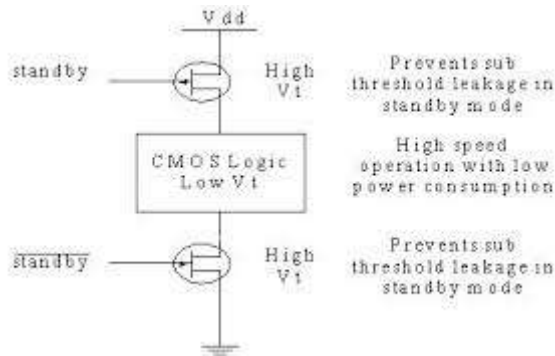


Figure 90: A Multiple-threshold CMOS (MTCMOS) logic gate

This circuit is also have two modes

1. Active mode
2. Stand by mode

In active mode the high-Vt Transistors are turned on and the logic gates consisting of low-Vt transistors can operate with low switching power dissipation and small propagation delay. In standby mode the high-Vt Transistors are turned off and the conduction paths for any sub threshold leakage currents that may originate from the internal low-Vt circuitry are effectively cut off.

5. Conclusion

This paper gives just a review of CMOS Technology. Overall conclusion after analyzing the previous research paper is that CMOS having the low power consumption. Due this low power consumption CMOS technology is used in high performance analysis of digital circuits. The leakage power is of great anxiety for designs in nanometer technologies and is becoming a major supplier to the total power consumption; leakage power has become more dominant as compared to Dynamic power. The gate leakage has become dominant sources of leakage and is expected to increase with the technology scaling. The solutions for leakage power dissipation or reduction of leakage power dissipation have to be required both at the process technology and circuit levels. Here we thoroughly reviewed the techniques for controlling the Leakage current of CMOS circuits in both standby and active modes of circuit operation and increase the speed of CMOS circuits.

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