The figure 5 shows a proposed symmetric design and implementation of Double-Gate Circuit with shorted gate mode which is called as FinFET-Bridge. Full adder is an logical circuit with the three inputs (A, B and Cin) and two outputs that is called Sum and Carry. Full adder is one of the core for the arithmetic processors, therefore by increasing the performance of full adder thereby the performance of processors also increased. The improve in performance which thereby decreasing propagation delay. This design generates Cout and Sum with 20 transistors, the use of two inverters is to improve the driving capability and produce Carry and Sum. Here also the design uses an 24 transistors.

The FinFETs Back gate is used to control the threshold voltage (V T) of the front gate, which is very important for the performance of the circuit. This is very much helpful in optimization of different circuits in terms of delay, area and power. In this paper we have designed FinFET Full Adder in SG-Mode to obtain a minimum delay and power dissipation in comparision with the CMOS. The waveforms are following the truth table1 of full adder. Here the power dissipation of the circuit in FinFET is least and hence preferred over other CMOS models. The time taken is less which means the speed is also improved using FinFET.

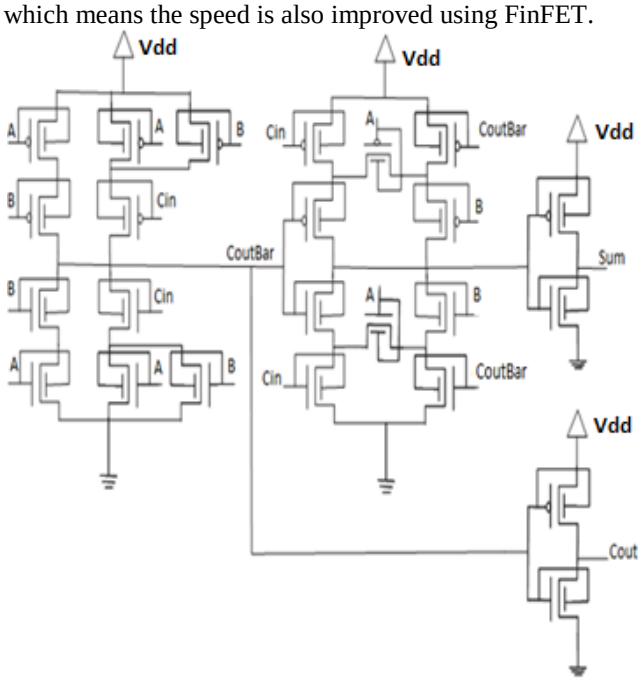

Figure 5: Proposed FinFET-Bridge Full Adder Circuit using Shorted Gate Mode

Table 1: Full Adder Truth Table

Input bit for number A	Input bit for number B	Carry bit input Cin	Sum bit output S	Carry bit output Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

5. Simulation Results and Discussion

The Simulation waveforms for full Adder using FinFET 16nm technology is shown in figure 6. The figure 7 and 8 shows the CMOS 32nm technology graph for different I/O bits of full adder versus the delay measurement. The figure 9 and 10 shows the graph for different I/O bits of full adder versus the delay measurement using Hspice simulation Tool by selecting FinFET 16nm foundry. The delay and power dissipation for CMOS 32nm and FinFET 16nm technology comparisons has been hereby shown through the graphs and tabulated the differences between them in table2. FinFET technology shows very less power dissipation when compared to CMOS technology in table2. The graphs show that the I/O bits are the output bits sum(S) and carry(C) with respects to the input bits (A, B, Cin). From the graphs we can see that the FinFET graphs shows the minimum variations in delay when compared to CMOS. Compare to the non-portable devices, the power consumption is very crucial because of the rising cooling cost and packaging as well as reliability problems. To achieve performance requirements within a power budget was the aims of VLSI (very-large scale integration) designers.

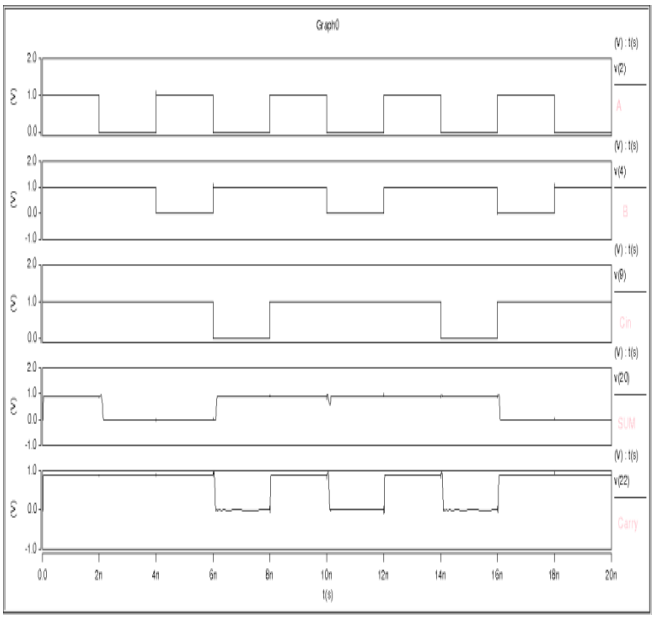

Figure 6: The simulation output for proposed Full Adder using FinFET 16nm technology

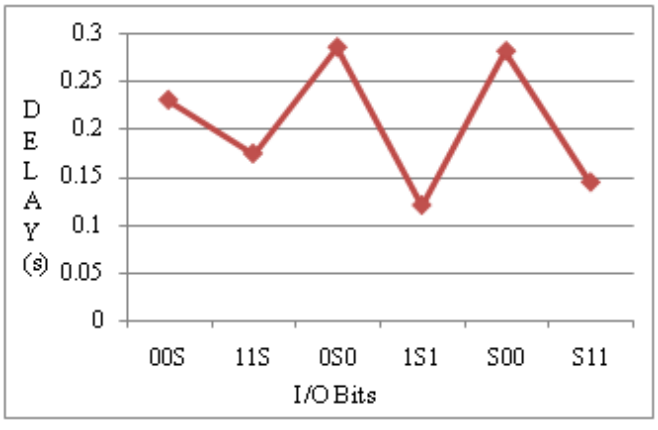

Figure 7: Graph for Full Adder I/O bits versus delay measurement using CMOS 32nm technology

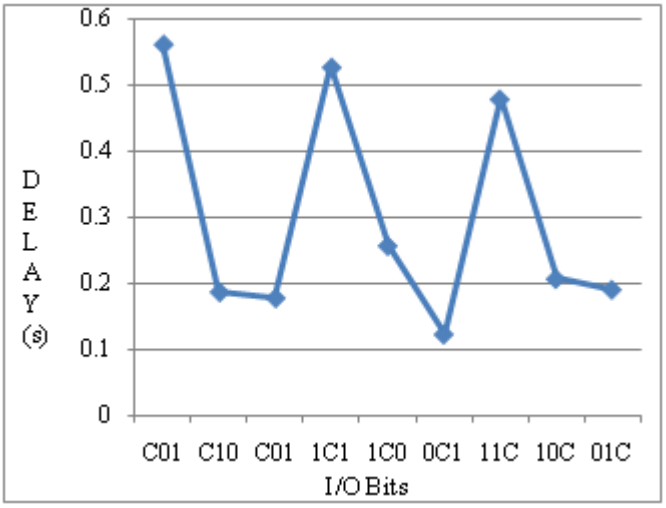

Figure 8: Graph for Full Adder I/O bits versus delay measurement using CMOS 32nm technology

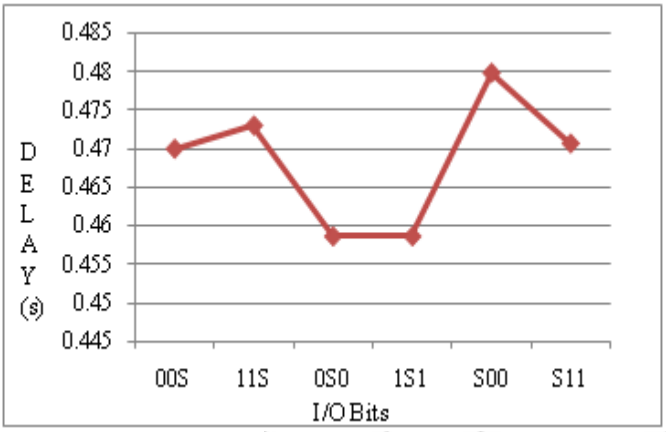

Figure 9: Graph for Full Adder I/O bits versus delay measurement using FinFET 16nm technology

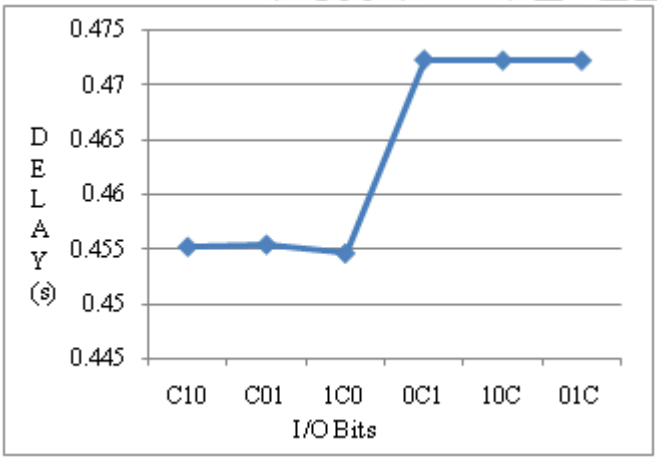

Figure 10: Graph for Full Adder I/O bits versus delay measurement using FinFET 16nm technology

Table 2: Parameter measurements between CMOS 32nm and FinFET 16nm Technology

ABC	Power Dissipation (micro watt) for CMOS 32nm	Power Dissipation (pw) for FinFET 16nm
000	1.1012	11.0337
001	6.208	13.1109
010	6.481	12.0759
011	16.933	11.1652
100	7.0225	10.5927
101	15.4115	11.1273
110	14.9081	12.2739
111	23.396	7.8950

6. Conclusion

FinFET are the new challenge for new material nowadays. This project focussed on the modelling FinFET using a PTM card. Here the FinFET model has been developed by following the parameter from nanoscale design. A new generation of Predictive Technology Model for Multi-gate (PTM-MG) devices has been developed for early-stage design-technology exploration. The DG model of FinFET is successfully constructed and the performance of the device has been analysed. In this paper, FinFET device has been simulated using Hspice tool and waveforms characteristics are plotted. The simulation result shows that with the 16nm FinFET, we can get a minimum delay and power dissipation in SG mode. Proposed Bridge-Full Adder is designed in SG-Mode using FinFET 16nm technology which is shown in the above circuit diagram, simulated waveforms and tables. By using FinFETs in VLSI circuits power dissipation can be reduced and speed can be improved. By using FinFET 16nm technology simulation results like total power dissipation and delay are successfully compared to 32nm CMOS model. Hence we can say that the use of FinFETs in VLSI circuits is essential.

7. Acknowledgment

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