

# Implementation of Delay Measurement System for Small Delay Defect Detection

Supriya Thorat<sup>1</sup>, Snehal Bhosale<sup>2</sup>

<sup>1</sup>Savitribai Phule Pune University, Department of E & TC, R.M.D Sinhad School of Engineering Pune 411052, India

<sup>2</sup>Savitribai Phule Pune University, HOD, Department of E & TC, R.M.D Sinhad School of Engineering Pune 411052, India

**Abstract:** *Large scale integration of LSI has resulted in an increase in small delay defects. Small delay variations are induced by process variation, power supply noise as well as resistive opens and shorts. In this paper we use flip-flop design which is used in performing internal path-delay test and measurement using scan path technique. The proposed method measures delay of the explicitly sensitized paths using on chip variable clock generator. This method produces test patterns using Automatic Test Pattern Generator (ATPG).*

**Keywords:** ATPG, Flip-flop, Measurement system, VLSI (very large scale integration).

## 1. Introduction

Semiconductor technology is highly used in VLSI system. With the rapid development and greater performance the delay testing become a critical problem. This Small delay defects can fails the system if the system is activated more times. Therefore we use delay measurement technique using scan flip flop and signature analysis. The proposed method does not require excepted test vectors because the test response is formed by using signature resistor. The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. This measurement technique is useful in detection and debugging of SDD. The main good point of this system is its more accuracy. The variation of measured Value depends on the clock frequency of clock generator.

## 2. Literature Review

### 2.1 Using Scan path Technique for SDD

In advanced digital electronics they test different digital circuits using scan path technique for SDD the ever increasing density and functional complexity of digital integrated circuits requires more efficient and narrowly focused methodologies for testing them.

Whereas a batch of broadside test patterns might have been sufficient to test most and some VLSI components of recent vintage this is no longer the case for present day VLSI components[2]. There are two major problem of testing modern VLSI components. First, the problem of testing for stuck-at failures which manifest themselves as circuits permanently tied to constant logic levels logic0 or logic1. Disadvantages of the system An optimistic approach to achieving the above described behavior is to perform scan-in to load the internal flip-flops with a pattern other than the desired test pattern, having performed prior circuit analysis to determine that the response of the circuit to a system clock pulse shall transform that pattern into the intended test pattern. However, this is a very difficult approach to implement due to the difficulty of performing the required circuit analysis which, in effect, requires

performing simulation in reverse time flow in order to determine what state the device under test should be placed in (using scan) so that its next state corresponds to the desired test pattern and the state transition between the scanned-in and final states correspond to the precise signal transitions which are required as part of the path-delay test pattern. Furthermore, since this technique allows creating signal transitions only as the combinational logic of the circuit permits, test patterns which appear correct when internal paths are considered on their own may not be applicable when the entire circuit of the IC component is put together. The biggest problem in doing so is the complexity of the algorithmic search necessary to determine the appropriate initial values which can be transformed by the system clock into the desired final values. Furthermore, dependencies among the circuit's inputs may make such a search very costly or prevent a successful outcome.

A clear advantage of using these techniques described here is the ability to store two independent values inside the same flip-flop. This eliminates the need to load initial values into the flip-flops and clock the system such that the system's response is captured and used as the final value for the path-delay test pattern.

### 2.2 Evaluating the Effectiveness of Measured Delay Defects

With the large development of semiconductor technology, small delay testing has become a critical problem. In deep submicron technology (DSM), normally observed breakdown mechanisms such as resistive opens, shorts and interconnects, gate oxide punch through, etc, can all lead to large numbers of delays on signal paths. There is rising concern that many of these small delay defects that often escape detection at test do not go fast effectively in burn-in to be detected, and can cause reliability problems in the field. While traditional delay testing has primarily focused on gross delays, it is becoming clear that "smaller" delay defects, including those on short paths, cannot be ignored [4]. A resistive via that increases the path delay by an additional 15% is a serious defect, even though the 15% increase in delay may be well within the timing margins

employed at test, allowing the defect to pass unobserved. The doubling-up of delay at the output of some gate because of a resistive via implies (based on a simple lumped RC model) via resistance comparable to the powerful transistor resistance, typically 1-3 kohms. Such a large resistive defect is quite likely to disgrace due to metal migration aid cause early life collapse.

Disadvantages of the difficulty in testing for small delay defects in circuits arises from the fact that signal delays are mainly dependent on input conditions, and the internal circuit state. Propagation delays are formed by crosstalk, voltage drop in the power supply grid from switching activity, partial charges on internal nodes, clock skew, etc. Sensitive delay testing requires setting up input conditions to cause worst-case delay propagation through the gate, or along the path being tested, to check if the output switches within the desired period.

### 2.3 Logic design for On-Chip Test Clock Generation

Structural testing of digital integrated circuits already has a long tradition in the semiconductor industry. Scan test in combination with automatic test pattern generation (ATPG) for stuck-at fault and test have been the manufacturing standard for lots of years. For about 20 years based on the gate delay fault model path delay fault model and transition fault model many publications show that at-speed test is able to detect assembly defects that are not enclosed by static tests, functional at-speed tests require a significant effort to develop compared to delay tests that are automatically generated by ATPG tools [5]. Moreover, delay tests have a known as fault coverage because of the handling of ATPG tools. Fault grading is difficult to unfeasible for functional at speed tests. Thus, the fault coverage for functional at-speed tests usually remains unidentified.

Even though the advantages are multifold and well known, delay test is still far from being as well-liked as stuck-at fault test is for SOC (system-on-a-chip) devices. This is due to several challenges that must be addressed for delay test to be implemented as part of the overall production test strategy. The first observation is that the number of patterns needed to achieve high fault coverage for transition fault testing is a number of times larger than the equivalent stuck-at pattern count. This implies, of course, the same increase in production test time and in vector memory usage on automatic test equipment (ATE). In addition, the transition fault coverage is usually noticeably lower than the analogous stuck-at fault coverage, for path delay testing, a small split of structural paths is typically selected to be targeted by an ATPG tool. Thus, path delay fault coverage has only a very imperfect meaning with respect to the overall chip area. Drawback of presented system is if high frequencies are generated on-chip for delay testing, then the ATPG tools need the capability to control the clock generation mechanism for all clock domains. In addition, the at-speed test data needs to be synchronized to the external low-speed tester. Looking at the still partial and growing list of issues, it is privileged that solutions have improved over time and are continuing to improve. With the latest developments in the area of pattern compression, the impact of increased pattern count is significantly reduced.

In our paper presents a delay test concept for soc devices with multiple clock domains. Circuitry for high-speed on-chip clock generation, implemented to avoid expensive test equipment, is described in detail. To the authors' knowledge, this is the first publication that presents implementation details for high-speed on-chip test clock generation. Enhancements to the presented clock generation circuitry, that are meant to improve fault coverage and pattern count, are discussed.

## 3. Implementation

### 3.1 Proposed Measurement System- Scan Based Delay Measurement

This paper presents a delay measurement technique using signature analysis for SDD detection. The proposed method does not require the expected test vector because the test responses are formed using signature registers (shift register) and scan flip-flop. The general area cost is of the order of conventional scan designs for design for test (DFT). These signature registers can be reused for testing, debugging the circuits. This method can be used with traditional, "no-timing" ATPG tools to generate a high-quality delay-fault pattern set. We start with an initial set of patterns and apply our pattern-grading method to calculate output deviations for the each and every pattern. We then sort the patterns according to their capability to detect SDD efficiently. The number of patterns in the final pattern set is determined by the user depending on test-time budget and target fault coverage.

This technique does not use the large-sized multiplexers but use scan chain and limited length of extra wires. Therefore it has less probability of dreadful conditions of the performance of normal operation. The embedded delay measurement approach can measure a path per a test vector. Therefore the measurement time increases as the number of the measured path. In the proposed method, they use variable clock generator, scan flip flop, reconfigurable signature register for small delay detection.

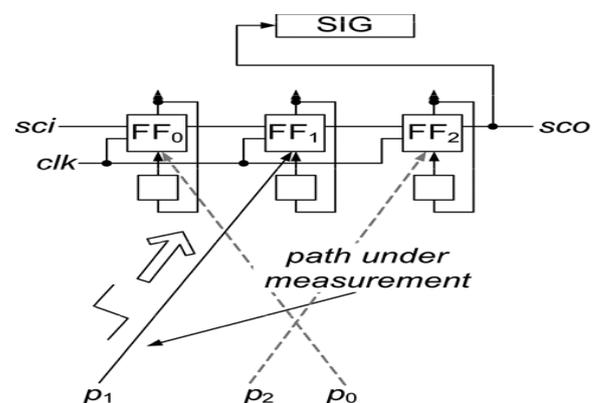


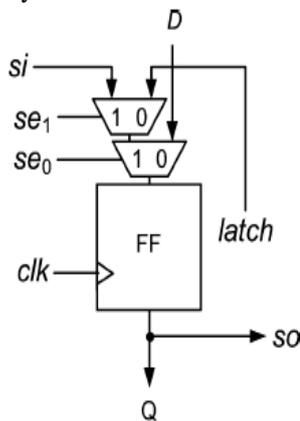
Figure 1: concept of proposed delay measurement

This section explains the proposed measurement system. Basically, the proposed method is scan based delay measurement system.

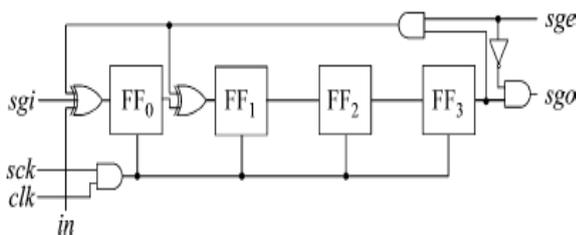
This example having three flip flops FF0, FF1 and FF2. Each flip flop has the input line (bottom), the output line (upper), and the clock line *clk*. Each flip flop is connected to an extra latch. At first, we assume that each flip flop has its own extra latch. The value of each flip flop is stored in the respective latch, and the value of each latch can be loaded to the correspondent flip flops.

In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation.

It minimize the time for multiple sensitization of a path. The horizontal line which connecting these flip flop is known as scan path. The symbols *si* and *so* represent the scan input and scan output respectively. The SIG represents the signature register using the linear feedback shift register as its component. The input of SIG is connected to the output of the last scan flip flop ff2. More detail structures of the scan flip fops and the signature register are shown in Figs. 2 and 3 respectively.



**Figure 2:** Scan flip-flop



**Figure 3:** Four bit reconfigurable signature register

### 1) Scan Flip Flop for Measurement

Fig. 2 is the gate level description of the scan flip flop for the proposed measurement. The lines *sgi*, *sgo*, and *clk* are the input, output, and clock lines of signature register respectively. The line *latch* is connected to another extra latch which provides the test bit to the scan flip flop. The lines *si* and *so* are the input and output for constructing the scan path. The input *si* is connected to *so* of an adjacent scan flip flop. The output *so* is connected to *si* of an adjacent scan flip flop or the scan output. The scan flip flop contains two multiplexers. The lines *si* and *latch* are the inputs of the upper multiplexer controlled by *se1*. The output of the upper

multiplexer and *D* are the inputs of the bottom multiplexer controlled by *se0*.

The output of the upper multiplexer and *D* are the inputs of the bottom multiplexer controlled by *se0*. When *se0*=0, the flip flop is in normal operation mode. When *se0*=1 and *se1*=1, the flip flop is in scan operation mode. When *se0* = 1, *se1*=0, the flip flop loads the value stored in the latch connected to the latch line.

### 2) Signature Register

The signature register having following functions to meet the demand of the proposed measurement.

- Capturing the test response in arbitrary timing.
- Shifting out the signature data in arbitrary timing.

Fig. 3 shows the signature register for the proposed measurement system. The length of the signature register in this example is four bit. Therefore it has four flip flops FF0, FF1 and FF3. The signature register can be configured to a shift register. The line *sge* controls the whole configuration. When *sge*=1, it works as a signature register. When *sge*=0, it works as a shift register.

### 3) Advantages of Proposed System

They have proposed a new delay testing method that overcomes many problems in detecting small delay defects outlined. In the new delay detection in the slack interval approach, additional delays, including those on short paths, are observed by sampling outputs within the supposed clock interval. Thus, unlike the traditional delay test method, the new approach does not require the setting up of most awful-case signal propagation conditions for a fault to be detected. As long as the fault is active along the signal path, it is detected. For a combinational circuit, this is done by observing the outputs at multiple time intervals, each gradually shorter than the nominal switching delay of the logic block. For practical scan based circuits, this translates to capturing the test responses to a delay test pattern at multiple fast clocks, each higher than the nominal operational clock rate.

In these proposed system aim to enhance both the quality and the efficiency of small-delay defect testing and characterization.

### 4. Conclusion

The proposal of this paper is as follows

In this paper they have proposed different methods of SDD.

- The proposal of the delay measurement method using signature registers and variable clock generator.
- This method can applied not only SOC but also FPGA. Because the smaller delay defect is serious problem in FPGA.

A future work is the low cost application of the proposed measurement to FPGA.

### References

- [1] K. Noguchi, K. Nose, T. Ono, and M. Mizuno, "A small-delay defect detection technique for dependable

- LSIs,” in Proc. IEEE Symp. VLSICircuits, 2008, pp. 64–65.
- [2] B. I. Dervisoglu and G. E. Stong, “Design for testability: Using scanpath techniques for path-delay test and measurement,” in Proc. IEEEInt. Test Conf. (ITC), 1991, pp. 365–374.
- [3] A. Krstic and K.-T. Chen, Delay Fault Testing for VLSI Circuits. Norwell, MA: Kluwer, 1998.
- [4] H. Yan and A. D. Singh, “Evaluating the effectiveness of detecting delay defects in the slack interval: A simulation study,” in Proc. IEEEInt. Test Conf. (ITC), 2004, pp. 242–251.
- [5] M. Beck, O. Barondeau, X. Lin, and R. Press, “Logic design for on-chip test clock generation-implementation details and impact on delay test quality,” in Proc. IEEE Des., Autom. Test Eur. Conf. Exhib. (DATE), 2005, pp. 56–61.