This example having three flip flops FF0,FF1 and FF2. Each flip flop has the input line (bottom), the output line (upper), and the clock line clk. Each flip flop is connected to an extra latch. At first, we assume that each flip flop has its own extra latch. The value of each flip flop is stored in the respective latch, and the value of each latch can be loaded to the correspondent flip flops.

In the proposed measurement, the test vector is stored in these latches after scan-in operation. Once the test vector is stored in the latches, the test vector can be loaded from these latches in a clock without scan-in operation.

It minimize the time for multiple sensitization of a path. The horizontal line which connecting these flip flop is known as scan path. The symbols *si* and *so* represent the scan input and scan output respectively. The SIG represents the signature register using the linear feedback shift register as its component. The input of SIG is connected to the output of the last scan flip flop ff2. More detail structures of the scan flip fops and the signature register are shown in Figs. 2 and 3 respectively.

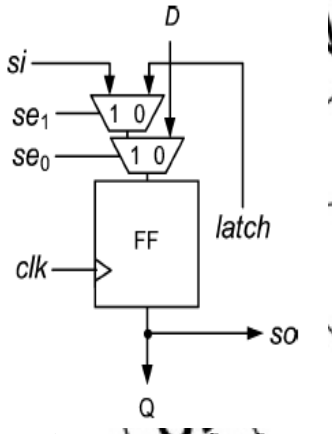

Figure 2: Scan flip-flop

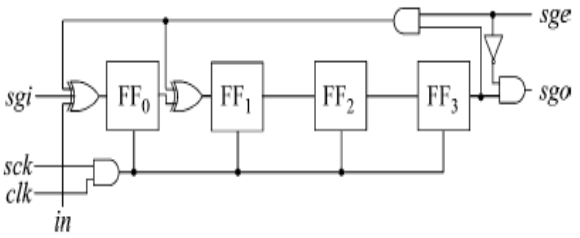

Figure 3: Four bit reconfigurable signature register

1) Scan Flip Flop for Measurement

Fig. 2 is the gate level description of the scan flip flop for the proposed measurement. The lines *sgi*, *sgo*, and *clk* are the input, output, and clock lines of signature register respectively. The line *latch* is connected to another extra latch which provides the test bit to the scan flip flop. The lines *si* and *so* are the input and output for constructing the scan path. The input *si* is connected to *so* of an adjacent scan flip flop. The output so is connected to *si* of an adjacent scan flip flop or the scan output. The scan flip flop contains two multiplexers. The lines *si* and latch are the inputs of the upper multiplexer controlled byse_1. The output of the upper multiplexer and D are the inputs of the bottom multiplexer controlled byse_0.

The output of the upper multiplexer and D are the inputs of the bottom multiplexer controlled byse_0. Whense_0=0, the flip flop is in normal operation mode. Whense_0=1andse_1 =1, the flip flop is in scan operation mode. When$se_0 = 1$,se_1=0, the flip flop loads the value stored in the latch connected to the latch line.

2) Signature Register

The signature register having following functions to meet the demand of the proposed measurement.

• Capturing the test response in arbitrary timing.
• Shifting out the signature data in arbitrary timing.

Fig. 3 shows the signature register for the proposed measurement system. The length of the signature register in this example is four bit. Therefore it has four flip flops FF0, FF1 and FF3.The signature register can be configured to a shift register. The line *sge* controls the whole configuration. When *sge*=1, it works as a signature register. When sge=*0*, it works as a shift register.

3) Advantages of Proposed System

They have proposed a new delay testing method that overcomes many problems in detecting small delay defects outlined. In the new delay detection in the slack interval approach, additional delays, including those on short paths, are observed by sampling outputs within the supposed clock interval. Thus, unlike the traditional delay test method, the new approach does not require the setting up of most awful-case signal propagation conditions for a fault to be detected. As long as the fault is active along the signal path, it is detected. For a combinational circuit, this is done by observing the outputs at multiple time intervals, each significantly shorter than the nominal switching delay of the logic block. For practical scan based circuits, this translates to capturing the test responses to a delay test pattern at multiple fast clocks, each higher than the nominal operational clock rate.

In these proposed system aim to enhance both the quality and the efficiency of small-delay defect testing and characterization.

4. Conclusion

The proposal of this paper is as follows
In this paper they have proposed different methods of SDD.

- The proposal of the delay measurement method using signature registers and variable clock generator.
- This method can applied not only SOC but also FPGA. Because the smaller delay defect is serious problem in FPGA.

A future work is the low cost application of the proposed measurement to FPGA.

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