

# A Review of Phase Lock Loop Techniques used in Communication Engineering

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**Abstract:** *In the optical communication in a backbone infra-structure, flexibility means, for example, programmable bitrates requiring a PLL with robust operation over a wide range of frequency range. A wide range PLL could be used by different protocols and applications so that we maximize the reusability and reduce time to market. In this review paper emphasis has been given to understand the basics of phase lock loop (PLL) systems and their underlying architecture. Also emphasis has been given to understand the basic design methodology for these systems.*

**Keywords:** Phase lock loop, Voltage controlled oscillator, frequency divider, charge pump, loop filter.

## 1. Introduction

High-performance digital systems use clocks to sequence operations and synchronize between functional units and between ICs. Clock frequencies and data rates have been increasing with each generation of processing technology and processor architecture. Within these digital systems, well-timed clocks are generated with phase-locked loops (PLLs) and then distributed on-chip with clock buffers. The rapid increase of the systems' clock frequency poses challenges in generating and distributing the clock with low uncertainty and low power. This research presents innovative techniques at both system and circuit levels that minimize the clock timing uncertainty with minimum power and area overhead. With the exponential growth of no of internet nodes, the volume of data transported by its backbone continues to rise rapidly. Among the available transmission media, optical fibers have highest bandwidth with lower cost, serving an attractive solution for internet backbone.

However, the electronic interface proves to be the bottleneck in designing high speed digital system. This fact, combined with the ever-shrinking time to market, indicates that designs based on flexible modules and macro cells have great advantages. In the optical

communication in a backbone infra structure, flexibility means, for example, programmable bitrates requiring a PLL with robust operation over a wide range of frequency range. A wide range PLL could be used by different protocols and applications so that we maximize the reusability and reduce time to market.

## 2. PLL Fundamentals

Phase-locked loops (PLLs) generate well-timed on-chip clocks for various applications such as clock-and-data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s. However, design and implementation of PLLs continue to be challenging as design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent. A large part of this research focuses on the design of a PLL for high-performance digital systems. The basic block diagram of a PLL is shown in Figure. A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock, CK<sub>ref</sub>, to produce a high frequency clock, CK<sub>out</sub>.

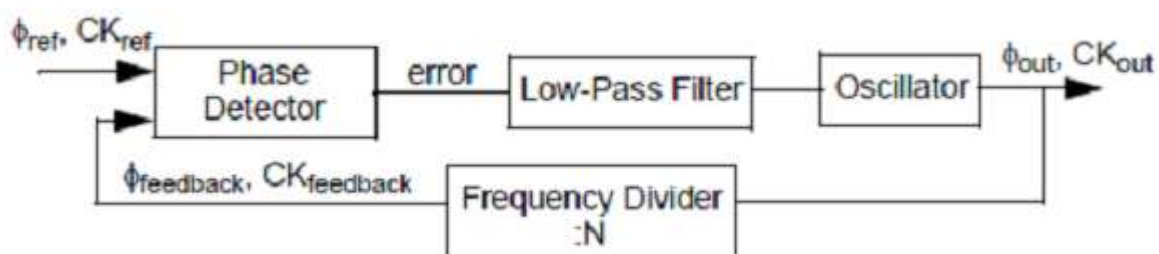


Figure 1: Basic PLL Block Diagram

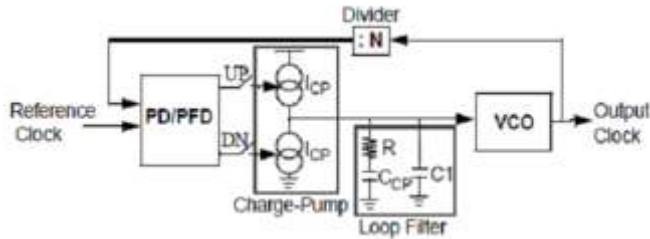
The basic operation of a PLL is as follows. The phase detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. The difference or error signal

is low-pass filtered and drives the oscillator. The filtered error signal acts as a control signal (voltage or current) of the oscillator and adjusts the frequency of oscillation to align  $\phi_{\text{feedback}}$  with  $\phi_{\text{ref}}$ . The frequency of oscillation is divided down to the feedback clock by a frequency divider. The phase is locked when the feedback clock

has a constant phase error and the same frequency as the reference clock. Because the feedback clock is a divided version of the oscillator's clock frequency, the frequency of oscillation is N times the reference clock.

### 3. PLL Component

The block diagram of a charge-pump PLL is shown in Figure. A PLL comprises of several components: (1) phase or phase-frequency detector, (2) charge-pump current, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. The functioning of each block is briefly described below.



**Figure 2:** Individual Blocks in PLL Diagram

#### 3.1 Voltage Controlled Oscillator

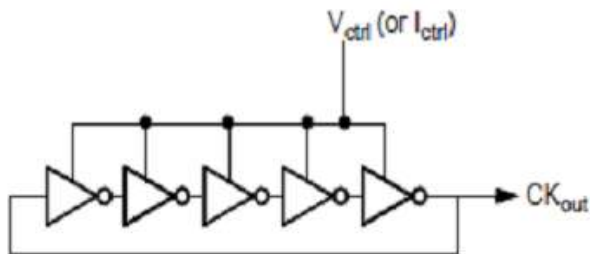
An oscillator is an autonomous system that generates a periodic output without any input. A CMOS ring oscillator shown in Figure is an example of an oscillator. So that the phase of a PLL is adjustable, the frequency of oscillation must be tunable. In the example of an inverter ring oscillator, the frequency could easily be adjusted with controlling the supply (voltage or current) of inverters. The slope of frequency versus control signal curve at the oscillation frequency is called voltage-to-frequency (current-to-frequency) conversion gain,  $KVCO$ ;

$$VCO = dfVCO/dVctrl$$

evaluated at  $fVCO$ . Since phase is the integral of frequency, the output phase of the oscillator is equal to  $\int \Phi VCO = KVCO \cdot Vctrl dt$ . In other words, the VCO in the frequency domain (s-domain), is modeled as

$$\Phi VCO / Vctrl (s) = KVCO / s;$$

Ideally, for the linear analysis to apply over a large frequency range,  $KVCO$ , needs to be relatively constant.



**Figure 3:** A five Stage Ring Oscillator

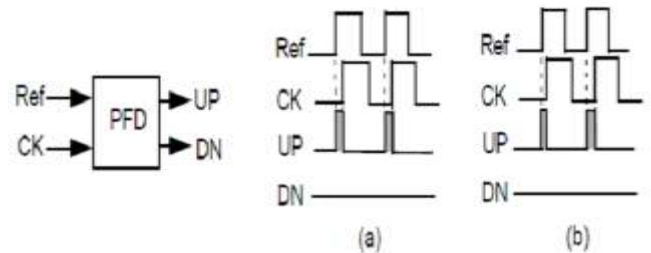
#### 3.2 Frequency Divider

The PLL reference clock is generated from a crystal. The crystals typically operate from tens to a few hundreds of MHz's. On the other hand; VCOs for clocking and parallel link applications operate at a few GHz or even ten GHz. For

proper functioning of the phase detector or phase-frequency detector, discussed in the next section, a frequency divider divides down the VCO frequency to the frequency of the reference clock.

#### 3.3 Phase Detector

The phase detector (PD) compares the phase difference between two input signals and produces an error signal that is proportional to the phase difference. In the presence of a large frequency difference, a pure phase detector does not always generate the correct direction of phase error. Phase error accumulates rapidly and can oscillate between phase error of  $>180^\circ$  and  $<180^\circ$  from cycle to cycle. The average phase detector output contains little frequency information and no valuable phase information. Since the phase detector is insensitive to frequency difference at the input, upon start-up when the oscillator's frequency divided by  $N1$  is far from the reference frequency, the PLL may fail to lock. The problem is known as an inadequate acquisition range of the PLL. To remedy the problem, a phase-frequency detector (PFD) is used that can detect both phase and frequency differences. Figure 2.4 conceptually demonstrates the operation of a PFD for two cases: (a) the two input signals have the same frequency, and (b) one input has higher frequency than another input. In both cases, the DC contents of PFD's outputs, UP and DN, provide information about phase or frequency difference



**Figure 4:** Operation of a PFD: (a)  $f_{ref} = f_{CK}$ ,  $\phi_{ref} \neq \phi_{CK}$  and (b)  $f_{ref} > f_{CK}$

#### 3.4 Charge Pump and Loop Filter

The charge-pump circuit comprises of two switches that are driven with UP and DN outputs of PFD as shown in Figure 2.2. The charge-pump injects the charge into or out of the loop filter capacitor (CCP). The combination of charge-pump and CCP is an integrator that generates the average of UP (or DN) pulses. This average voltage adjusts the frequency of the subsequent oscillator circuit. Since the VCO introduces another integrator, the loop gain of a charge-pump PLL has two poles at origin; thus, the closed loop system is unstable. To stabilize the system, a zero,  $\omega_z = 1/RCCP$ , is introduced in the loop gain by adding a resistor, R, in series with CCP. The PFD, charge pump and filter are often modeled with a linear continuous-time model. In reality, the PFD acts as a pulse modulator system and drives the charge-pump for the duration of pulse width which is equal to PFD input phase difference,  $\Delta\phi$ . The actual phase response is not linear because phase is cyclical. Furthermore, the phase information is discrete, sampled at the clock reference frequency.

### Noise and Power Considerations

The primary goal to design a PLL for high-performance digital systems is to generate an output clock with minimum timing uncertainty. The timing uncertainty arises from mismatches in devices and noise sources present in the system. Device mismatches causes a static phase shift (or skew) in the PLL output clock from its desired phase. Skew can be minimized with a careful layout and increasing the device size. Skew is generally less critical than jitter because, due to its static nature, the system can compensate for the static errors. Dynamic noise causes a random phase shift (or jitter) in the PLL output clock. The noise sources in a PLL are device electronic noise such as thermal noise or flicker noise and power-supply or substrate noise.

### 4. Conclusion

In this paper a very basic analysis of Phase lock loop and its underlying components has been considered, this work will be farther extended by designing and modeling a phase lock loop along with modifications. As seen and discussed in the research paper that the phase lock loop has several distinct advantages over traditional method of signal conditioning along with this the PLL system has far more utilities as cited in various research paper discussed below.

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