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A Comparative Study and Review of Different Clock Gating Techniques and their Application

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Abstract: ***With the increasing applications of electronics in day-2-day life and alteration in design techniques in the field of VLSI, we are required to design the ICs with maximum efficiency. By efficiency, here we mean the power consumption, the delays, operation at different frequencies and the stability of designed circuit. In this paper we have focused on the Clock Gating technique to decrease the dynamic power dissipation of CMOS based circuit, being an issue of great concern at higher clock rates. Further we analyzed a Clock Gating technique to observe difference in the power consumption in Johnson Counter. Doing some power analysis in SPICE, it is observed that proposed technique has lower power dissipation compared to the conventional design.***

Keywords: Clock Gating (CG); latch free clock gating; latch based clock gating; Flip-flop based gating; Clock gated Johnson Counter.

1. Introduction

Clock power consumes almost 50 percent of total chip power and is expected to increase further in up-coming designs at 45nm or below. This is due to the fact that dynamic power dissipated in a circuit is directly proportional to voltage and the frequency of the clock as given by following equation:

$$\text{Power} = \text{Capacitance} * (\text{Voltage})^2 * (\text{Frequency})$$

Hence, reducing clock power is very important as we are moving on circuits operating in GHz range. Clock gating is one of the booming techniques for power reduction used commonly now-a-days.
Most commonly used methods employed for minimizing dynamic power in sequential circuits are generally based on the following techniques:
1) Clock-gating (CG)
2) Re-timing technique
3) State assignment technique
Here we are discussing about Clock Gating Technique only.

The following section describes clock gating techniques and a comparison shown in Johnson Counter considering the conventional design with clock gated design. Methodologies, Application, Schematic, Results and some Conclusions will be discussed further in this review paper.

2. Clock Gating

Clock gating technique is used to reduce the power dissipation in sequential circuits by gating unnecessary clock pulses from various segments of system. It is observed that clock transitions contribute to major part of power dissipation in a system (almost 15-45%) which is a matter of great concern especially at frequency of operation in several GHz. Here unnecessary transitions are not loaded to sub-component when the clock is not active for that part. CG is illustrated in figure 1 block CG, which blocks the clock signal associated with each functional unit when the gating condition is not true.

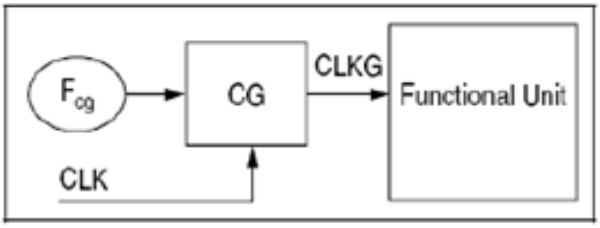


Fig 1. Clock gating principle

Figure 1: Clock Gating Principle

It is good design ideology to turn off the clock when it is not needed. Automatic clock gating is supported by modern EDA tools. They identify the circuits where clock gating can be inserted.
There are different types of clock gating techniques to optimize power in VLSI circuits which will be our main concern in this paper. They can be:
1) Latch-free based design.
2) Latch-based design.
3) Flip-flop based design.
4) Intelligent clock gating optimizing option available in synthesis tool like Xilinx, Altera, Cadence etc.

3. Latch-Free Based Clock Gating Design

The latch-free clock gating style uses a simple AND or OR gate (depending on the edge on which flip-flops are triggered). Here if enable signal goes inactive in between the clock pulse or if it is activated multiple times then gated clock output either can terminate untimely or generate multiple clock pulses. This restriction makes the usage of this technique inappropriate and can lead to improper circuit functioning. This design is shown below in figure 2:

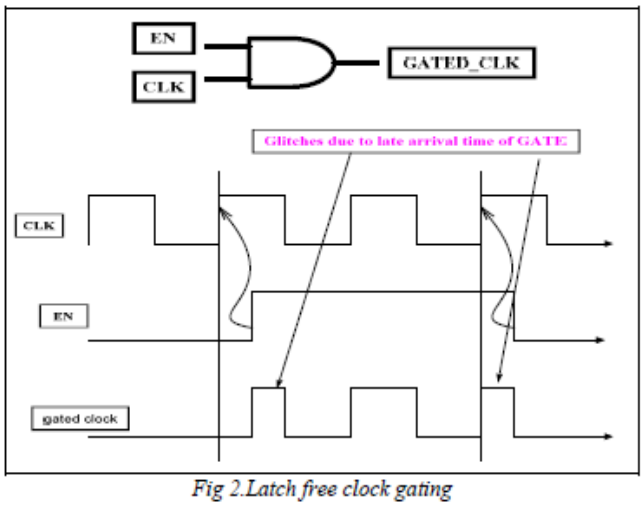
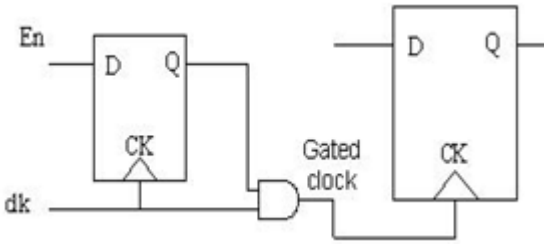


Fig 2.Latch free clock gating

4. Latch-Based Clock Gating Design

The latch-based clock gating style includes a level-triggered latch in the design to hold the enabled clock gated signal from the active edge of the clock until the inactive edge of the clock. Since the latch captures the state of the enable signal and holds it until the complete clock pulse has been generated, the enable signal need only be stable around the rising edge of the clock. The design technique is described in the figure 3 shown below:



Latch Based clock gating

This gating technique is easy to implement. A simple AND gate is utilized to generate the gated clock signal. This configuration (figure 4) is glitch-free because the control signal, generated when Phi1 is high, is stable and remains stable when Phi2 goes high.

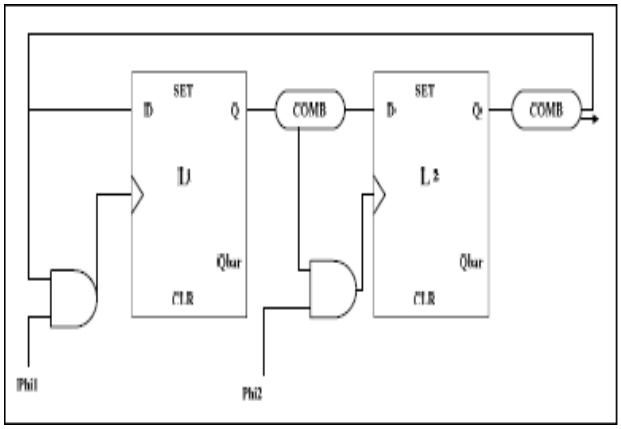


Figure 4: Clock gating of latched based design

5. Flip-Flop Based Clock Gating Design

This kind of flip-flops based design are not preferable if design area and power considerations are more important parameters in the circuit, but their advantage compared with gated-clock-based design is that testability can be easily executed and clock skewing is more easy to look after.

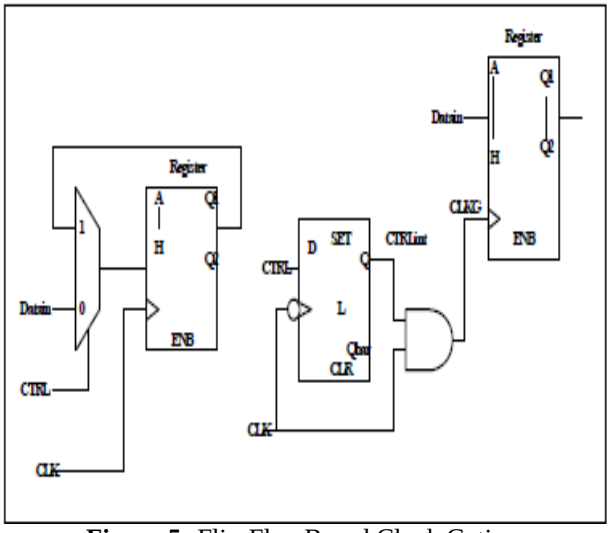


Figure 5: Flip-Flop Based Clock Gating

6. Intelligent Clock Gating Optimizing Option Available in Synthesis Tool

Recently, in many industrial tools like Altera and Xilinx, intelligent clock gating option is available in the tool itself to optimize the power consumption of the design. It may be possible that designer may not always get power reduction to estimated level. Therefore in such cases designer may have to utilize clock gating methods reviewed above at RTL level to further reduce the dynamic power consumption of the circuit and ultimately optimize it.

7. Issues in Implementation of Clock Gating Design Techniques

1)The clock gate may introduce changes in the waveform of the clock other than switching it on or off.
2)Clock gating hold time violation and set-up time violation.
3)Clock gating can potentially divide clock, so care should be taken about the phase of clock gating signal.
4)Glitches may be present in the gated clock.
5)Improper control of the gating signal can result in improper working of circuit.
6)Extra hardware requirements in circuitry.

8. Applications and Implementation of Clock Gating Technique

In this section, we have shown the reduction in dynamic power consumption in JOHNSON COUNTER circuit. Giving a brief review about Johnson counter, these are ring counters which have 2^N count states, where N is the number of bits in counter. Further they are preferable because they can self-initialize from the all-zeros state, without having

any requirement of the first count bit to be provided externally at time of their start-up.

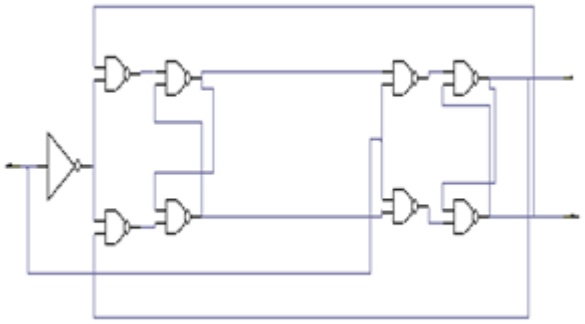


Figure 6: JK-FF used in clock gated design

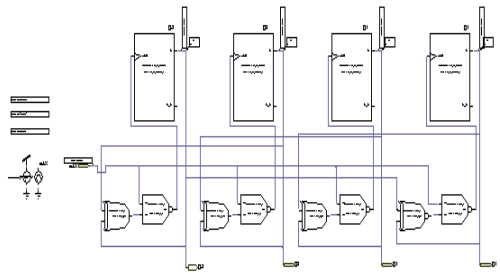


Figure 7: Clock gated Johnson counter (schematic)

9. Work Completed

Design of conventional Johnson counter using D flips flop. Design of clock gating logic circuitry to be implemented in Johnson counter.

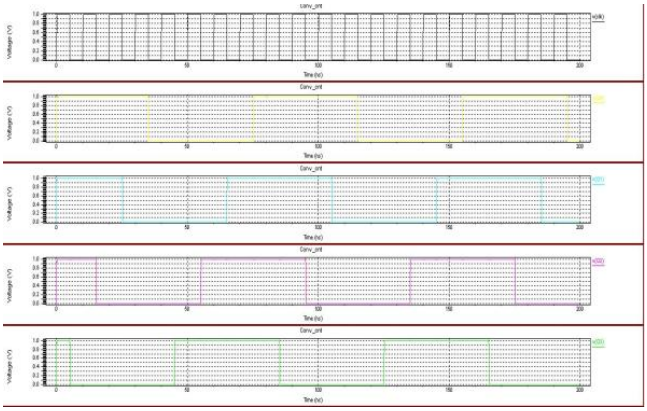


Figure 8: Clock Gated Design Waveforms

10. Simulations and Results

Table 1: Power Consumption Results

Frequency(MHz)	100	200	300	400	500
Power consumption In Conventional Design (uW)	20.02	36.67	53.93	72.96	90.46
Power consumption in Modified Design (uW)	12.53	23.31	33.98	45.16	55.92

The simulated results make this fact absolutely clear that there is considerable amount of reduction in Power Dissipated in Johnson Counter. A plot of Power Consumption Vs Frequency for the same is shown in the fig 9 described below.

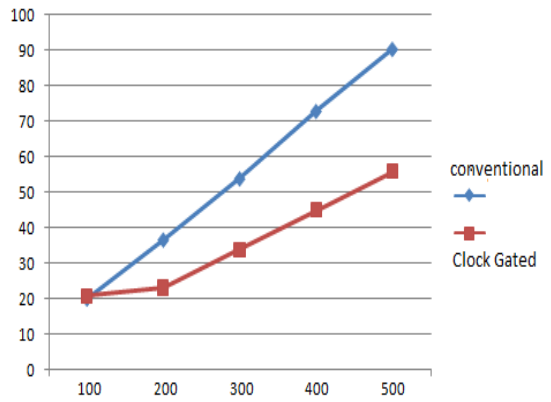


Figure 9: Power vs. Frequency plot

11. Conclusion

We have shown in SPICE simulations of each of the design the analysis of power dissipated in circuit. The main parameter of observation is Power consideration. Although theoretically power dissipation due to clock transitions is minimized by 75, but in simulations it is found that the total power dissipation is minimized by 38 % compared to the conventional system power dissipation. It indicates that the clock gating system contributes in the power dissipation but still our designed system is power friendly compared to the conventional design.

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