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A Review and Comparative Study of Different Low Power Consumption Techniques

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Abstract: ***Power consumption has became a main problem in VLSI especially the static power consumption. So to reduce this we use different low power consumption techniques such as Reverse Body Biasing, Dual Threshold CMOS, Sleepy Stack, sleepy transistor, sleepy keeper approach. We also analyze this and make our results***

Keywords: Reverse Body Biasing, Dual Threshold CMOS, Sleepy Stack, sleep transistor, sleepy keeper approach

1. Introduction

With advancement in VLSI we require devices with less power consumption and short delay. But in actual these both are contradict to each other. If we increase the one, another one must be decreases because power delay product must be constant so there must be proper tradeoff between power consumption and delay. RBB, DTCMOS, sleepy stack, Sleep transistor technique is used to reduce the power consumption. This can be done by reducing sub threshold current which further reduces the static power consumption. We know that power consumption is proportional to the sub threshold current, if we decrease the current we can decrease the power consumption and this current is decreased if we increase the threshold voltage so here we increase the threshold voltage by using RBB and DTCMOS techniques and the sub threshold current also reduced by sleepy stack techniques in which we give the same input to the 2 MOSFETs so that there is no leakage current.

This paper is organized as follows: Section 1 is methodologist in which we study different methods for low power consumption. Section 2 includes the experiment methodology. Section 3 includes the schematic results. Section 4 includes the conclusion.

2. Methodology

There are different methods to reduce the power consumption.

Sleep Transistor: In this type of technique the sleep transistors having high threshold is placed between the Vdd and the pull up network and another transistor is placed between the pull down network and ground. These transistors turn ON when circuit is ON and turn off when circuit is idle. By cutting off the power supply this can reduce the leakage power. But when it is cut off it does not hold states it destruct the states.

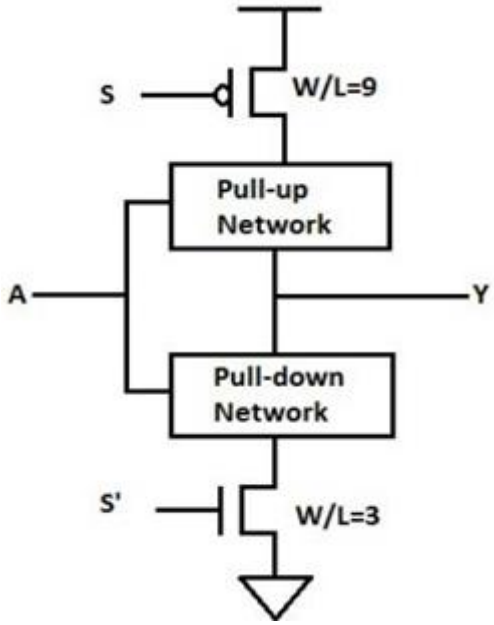

Figure 1: Sleep Transistor

Sleepy Stack approach: This technique divides the transistor into two half size transistors. In this every half transistor added in series so that there is small leakage current. It also added sleepy transistors to disconnect the power supply and ground from the network so that there is no power consumption in off mode.

Sleepy Keeper approach: This technique is used to remove the problems occurred in sleep transistors means the problem of holding stage. So it uses the two transistors PMOS in parallel to NMOS and NMOS in parallel to PMOS. Both of this is provided with feedback from the output of first circuit. By this it reduce the more power consumption.

Reverse Body Biasing technique: In this technique we provide voltage to the body terminal of MOSFET to increase the threshold voltage which further decreases the sub threshold current which helps to reduce the power consumption because power is proportional to the current.

Dual Threshold CMOS: In this technique we use different CMOS with different threshold voltage to decrease the power consumption. It mainly decreases the sub threshold leakage

current. But at the same time it also increases the number of MOSFETs which increases the delay.

There is one paper [1] which combines all this approach to reduce the power consumption. We also analyses this paper. This approach reduces the power consumption.

3. Experimental Methodology

In this paper they have designed multiplexer and JK flip flop using these techniques and dynamic power is measured when the sleepy switch is ON and static power is measured when sleepy switch is off. They conclude that if we use these techniques then dynamic power is decreased by 30% and static power is decreased by 59% in multiplexer but it will increase the delay by 55% and in JK flip flop the dynamic power is reduced by 13% and static power is reduced by 99% but delay is increased.

This is the figure 2 of 2 input NAND gate. In this NAND gate they uses DTCMOS techniques in which they uses two threshold MOS for reducing the leakage current. In this NAND gate they also use the RBB with -2.2V because at this static power consumption is minimum.

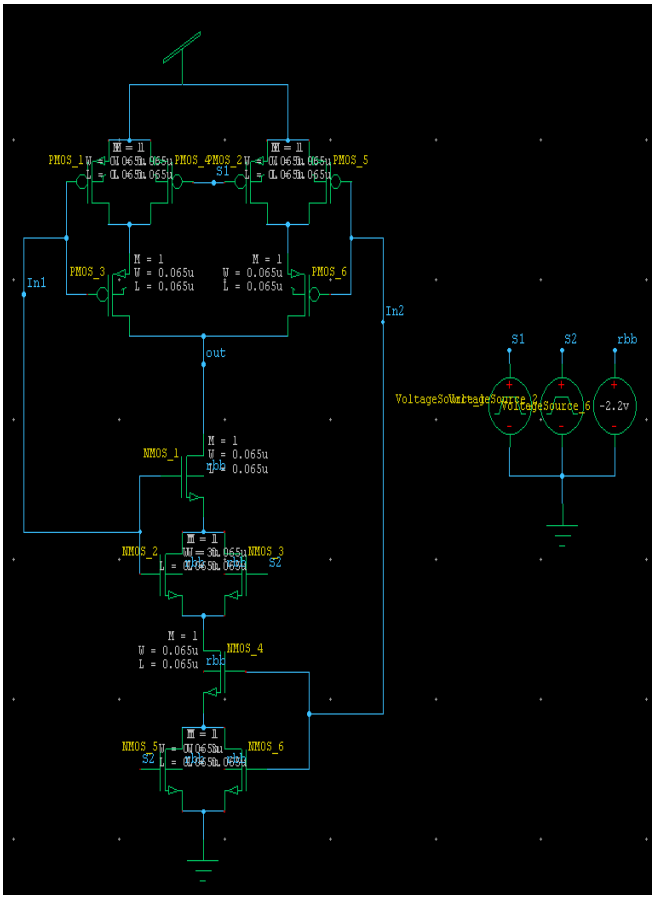

Figure 2.2: Input NAND gate

In JK master slave flip flop it works in two steps when clock is high only master will works, slaves will not work but when clock is low master will not work only slave will work. In this paper they designed this JK master slave flip flop using 2 input NAND gate sleepy stack with RBB and DTCMOS.

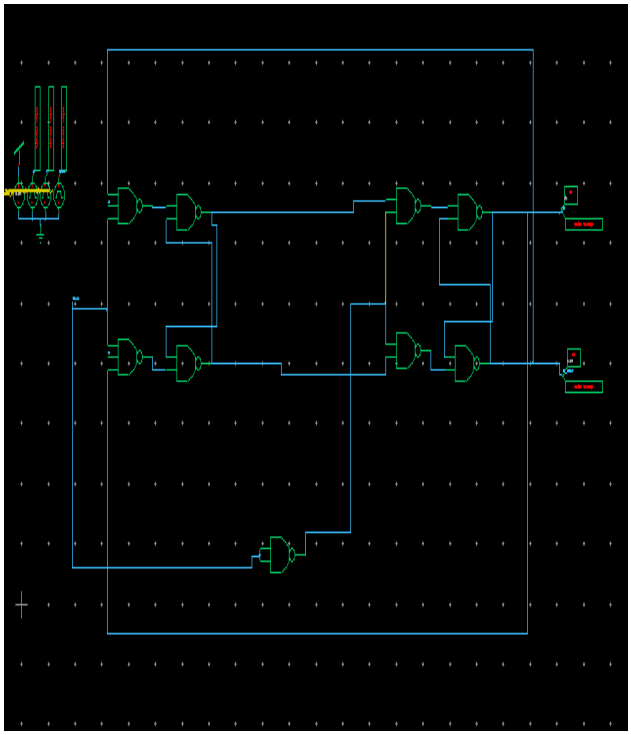

Figure 3: Schematic of JK flip flop

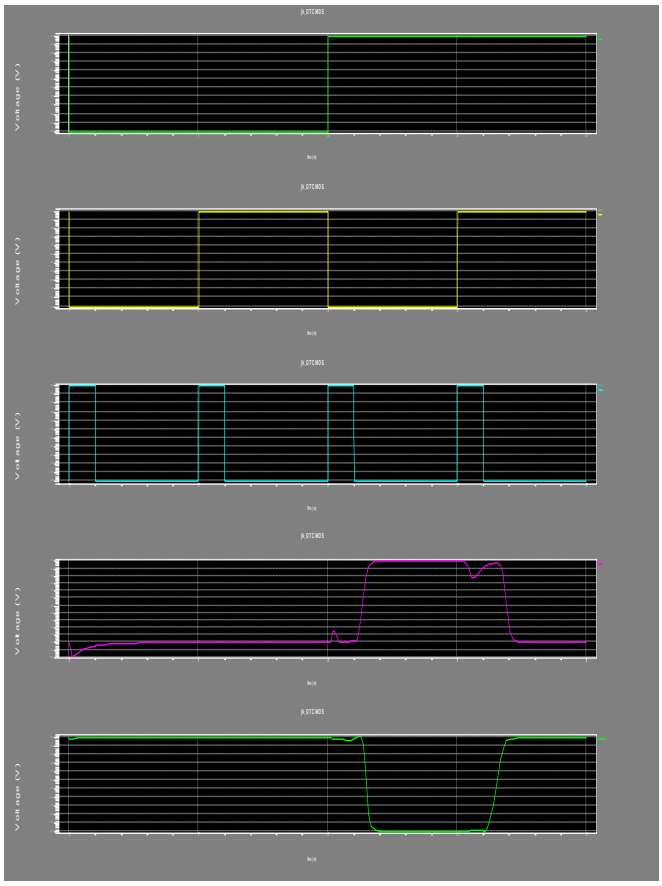

Figure 4: Output waveform of JK master-slave flip-flop

In multiplexer also they uses the 2 input and 3 input NAND gate. In this multiplexer there is 2 select lines A and B with 4 inputs I0, I1, I2, I3. With the help of these select lines we select the inputs. In this we uses the RBB, DTCMOS, Sleepy Stack technique.

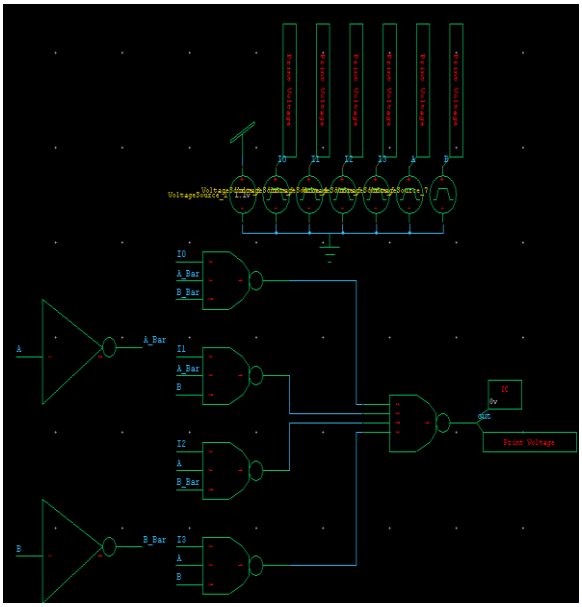

Figure 5: Schematic of multiplexer

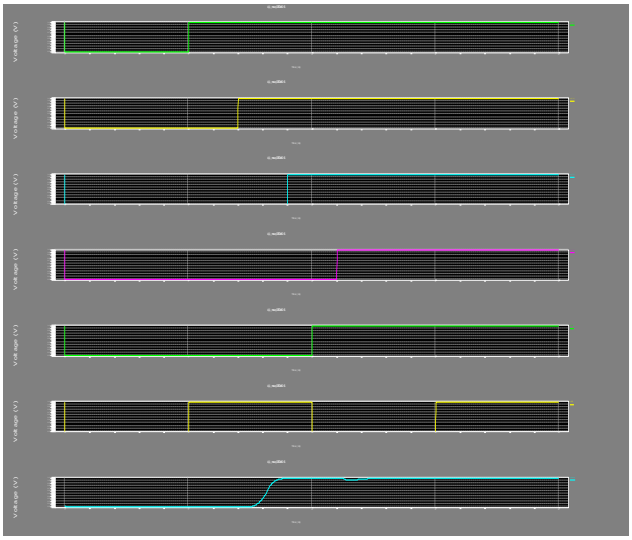

Figure 6: Output waveform of 4*1 multiplexer

4. Simulation Results

Table 1: Percentage Static power saving for 4*1 Multiplexer with RBB and without RBB

State	Static power(nW) with DTCMOS & RBB	Static power(nW) without DTCMOS & RBB	Percentage Saving (%)
00	744	1346	44
01	938	1322	29
10	1037	1366	24
11	1120	1383	19

Table 2: Percentage Delay Increment for 4*1 Multiplexer with RBB and without RBB

State	Delay(pSec) with DTCMOS & RBB	Delay(pSec) without DTCMOS & RBB	Percentage Increment (%)
00	**393**	**262**	**50**
01	**597**	**459**	**30**
10	**673**	**439.86**	**53**
11	**545**	**422**	**29**

Table 3: Dynamic power, Delay analysis of JK Master-Slave Flip-Flop with DTCMOS and RBB

65nm	Dynamic Power(nW)	Delay(pSec)
With DTCMOS & RBB	933	322
Without DTCMOS & RBB	1032	206
Percentage Saving (%)	9.59	56.31 (Increment)

Table 4: Static power, with DTCMOS and RBB

State	Static power(nW) with DTCMOS & RBB	Static power(nW) without DTCMOS & RBB	Percentage Saving (%)
00	351.2	1911.3	81.62
01	351.3	1669.7	78.96
10	533.8	1910	72.05
11	533.9	1690.5	68.42

5. Conclusion

In this paper the technique used by them is very effective. It reduces the total power consumption by many times which we require the most but at the same instance it also increases the delay. In this paper the number of MOSFETs also increases which increases the size of the circuit which is not require. In this paper it specifies to work only at high clock but if we work at high clock only then we can't get the results. Also the waveform shown for JK is not correct. In this we can reduce the switches because if we not use this then also we get the full swing, it reduces the number of MOSFETs which decrease the size of the circuit also it reduces the delay and the power consumption.

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