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Matrix Representation of Hanoi Graphs

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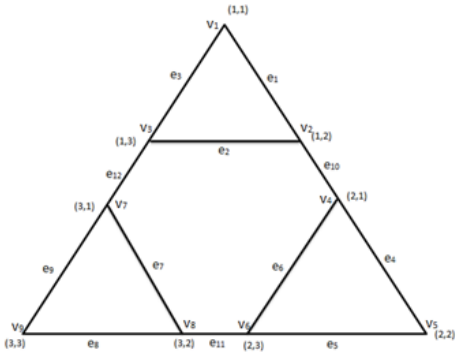
Abstract: ***In this Paper, we construct the circuit matrix and the incidence matrix of Hanoi Graph H_2. Finally, we are able to detect the number of edges and number of vertices in Hanoi graphs with the help of the identity matrix.***

Keywords: Hanoi Graphs, Circuit matrix, Incidence matrix.

AMS subject classification (2000): 05C15, 05C69

1. Introduction

The Tower of Hanoi puzzle, invented in 1883 by the French mathematician Edouard Lucas, has become a classic example in the analysis of algorithms and discrete mathematical structures. The puzzle consists of n discs, no two of the same size, stacked on three vertical pegs, in such a way that no disc lies on top of a smaller disc. A permissible move is to take the top disc from one of the pegs and move it to one of the other pegs, as long as it is not placed on top of a smaller disc. The set of configurations of the puzzle, together with the permissible moves, thus forms a graph in a natural way. The number of vertices in the n-disc Hanoi graph is 3n.



Graph 1

The Hanoi graph H_n corresponding to the allowed moves in the tower of Hanoi problem. The above figure shows the Hanoi graphs for small n. The Hanoi graph H_n can be constructed by taking the vertices to be the odd binomial coefficients of Pascal's triangle computed on the integers from 0 to $2^n - 1$ and drawing an edge whenever coefficients are adjacent diagonally or horizontally. The graph H_n has 3^n vertices and $3(3^n - 1)/2$ edges. Each Hanoi graph has a unique Hamiltonian cycle. (Equivalently, each Hanoi graph has exactly two distinct directed Hamiltonian cycles.)

H_n has 3^{n-1} small triangles, each of which can contain at most one vertex in an independent vertex set. But the triangles are arranged in the plane in such a way that choosing the apex of each gives a (maximum) independent vertex set .Hanoi graphs are perfect.

2. Circuit Matrix

In a Circuit Matrix the edges are distinct. In this Hanoi graph H_2 we have Five circuits. Among these five circuits the first three circuits are the three cliques in the graph. The fourth circuit is one which covers all the three cliques and the fifth one is the circuit which includes the cycle that consists of all the non-adjacent vertices.

In Graph 1, the circuits are
$\{e_1, e_2, e_3\}$, $\{e_4, e_5, e_6\}$, $\{e_7, e_8, e_9\}$, $\{e_{10}, e_6, e_{11}, e_7, e_{12}, e_2\}$, $\{e_1, e_{10}, e_4, e_5, e_{11}, e_8, e_9, e_{12}, e_3\}$.

Let the number of different circuits in a graph G be q and the number of edges in G be e. Then a *Circuit Matrix* A= $[a_{ij}]$ of G is a q by e, (0,1)-matrix defined as follows :
$a_{ij} = 1$, if i^{th} circuit includes j^{th} edge, and
$a_{ij} = 0$, otherwise.
The Circuit Matrix of graph 1 is

$$A = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array} \begin{array}{c} \begin{array}{cccccccccccc} e1 & e2 & e3 & e4 & e5 & e6 & e7 & e8 & e9 & e10 & e11 & e12 \end{array} \\ \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \end{array}$$

The following observations can be made from the above circuit matrix of the graph 1:

i. Each row of **A** is a circuit vector.
ii. The number of 1's in a row is equal to the number of edges in the corresponding circuit.

3. Incidence Matrix

Let G be a graph with n vertices, e edges and no self-loops. Define an n by e matrix **B** = $[b_{ij}]$, whose n rows correspond to the n vertices and the e columns correspond to the e edges, as follows :
$b_{ij} = 1$, if j^{th} edge e_j is incident on i^{th} vertex v_i, and
$b_{ij} = 0$, otherwise.
Such a matrix **B** is called *vertex-edge incidence matrix* (or) simply i*ncidence matrix.*
The incident matrix of the graph 1 is

$$B = \begin{array}{c} \\ v1 \\ v2 \\ v3 \\ v4 \\ v5 \\ v6 \\ v7 \\ v8 \\ v9 \end{array} \begin{array}{c} \begin{array}{cccccccccccc} e1 & e2 & e3 & e4 & e5 & e6 & e7 & e8 & e9 & e10 & e11 & e12 \end{array} \\ \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 \end{bmatrix} \end{array}$$

The following observations can be made from the above incident matrix of the graph1:

i. Since every edge is incident on exactly two vertices, each column of **B** has exactly two 1's.
ii. The number of 1's in each row equals the degree of the corresponding vertex.

Next, we find the Transpose matrix of both the circuit and incidence matrices. From the transpose matrix we can conclude the following theorem.

4. Theorem

Let **A** and **B** be the circuit and incidence matrix whose columns are arranged using the same order of edges. Then we can prove that
$A.B^T = B.A^T = 0$ (mod 2).

Where superscript **T** denotes the transpose matrix.
Proof :
Consider a vertex *v* and a circuit **C** in a graph **G**. Either *v* is in **C** or it is not. If *v* is not in **C** then, there is no edge in the circuit **C** that is incident on *v*. On the other hand, if *v* is in **C** then, the number of those edges in the circuit **C** that are incident on *v* is exactly two.

Consider the i^{th} row in B and the j^{th} row in A. Since the edges are arranged in the same order, the nonzero entries in the corresponding positions occur if the particular edge is incident on the i^{th} vertex and is also in the j^{th}circuit.

If the i^{th}vertex is not in the j^{th} circuit, there is no such nonzero entry and the dot product of the two rows in zero. If the i^{th} vertex is in the j^{th} circuit, there will be exactly two 1's in the sum of the products of individual entries. Since 1 + 1 = 0 (mod 2), the dot product of the two arbitrary rows one from A and other from B is zero.
Hence the proof.

Hence,

$$\mathbf{AB^T} = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{array} \begin{array}{c} \begin{array}{ccccccccc} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 \end{array} \\ \begin{bmatrix} 2 & 2 & 2 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & 2 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 2 & 2 & 2 \\ 0 & 2 & 2 & 2 & 0 & 2 & 2 & 2 & 0 \\ 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 & 2 \end{bmatrix} \end{array} = \mathbf{0 \pmod 2}$$

and

$$\mathbf{BA^T} = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \end{array} \begin{array}{c} \begin{array}{ccccc} 1 & 2 & 3 & 4 & 5 \end{array} \\ \begin{bmatrix} 2 & 0 & 0 & 0 & 2 \\ 2 & 0 & 0 & 2 & 2 \\ 2 & 0 & 0 & 2 & 2 \\ 0 & 2 & 0 & 2 & 2 \\ 0 & 2 & 0 & 0 & 2 \\ 0 & 2 & 0 & 2 & 2 \\ 0 & 0 & 2 & 2 & 2 \\ 0 & 0 & 2 & 2 & 2 \\ 0 & 0 & 2 & 0 & 2 \end{bmatrix} \end{array} = \mathbf{0 \pmod 2}$$

Therefore,

$$\mathbf{AB^T \times BA^T} = \begin{bmatrix} 12 & 0 & 0 & 8 & 12 \\ 0 & 12 & 0 & 8 & 12 \\ 0 & 0 & 12 & 8 & 12 \\ 8 & 8 & 8 & 24 & 24 \\ 12 & 12 & 12 & 24 & 36 \end{bmatrix} = 0 \pmod 2$$

Since the Hanoi graph H_2 consists of three discs, we get a 3×3 identity matrix from the above matrix

$$\begin{bmatrix} 12 & 0 & 0 \\ 0 & 12 & 0 \\ 0 & 0 & 12 \end{bmatrix}$$

$$= 12 \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

= 12 I
= 4nI .Here n = 3.
Hence this Hanoi graph H_2has

$$4nI = 12 \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

5. Conclusion

Therefore, the Hanoi graph H_2 has n^2 vertices and $\frac{n(3n-1)}{2}$ edges.

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