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Comparative Analysis of Cascaded Half Bridge Inverter Using Different Modulation Techniques

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Abstract: ***The multilevel inverters have gained very great interest in the power industry. It is easy to generate high power with medium voltage switches multilevel structure in which the voltage stresses of the devices can be controlled. Increase of the number of voltage levels in inverter without the increase in the rating of the switches increases the power rating and reduces the harmonic distortion. It enables to reach high voltages with low harmonic distortion without the use of transformers. Different modulation techniques such as phase disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD) techniques are used to generate the pulse pattern for the inverter. In this paper, a five level and twenty one level cascaded half bridge multilevel inverter are simulated in MATLAB/Simulink and the harmonic analysis has been carried out.***

Keywords: ***Multilevel Inverter; Harmonic Distortion; Modulation Techniques; Phase disposition; Phase opposition disposition; Alternate phase opposition disposition.***

1. Introduction

In recent years, the demand for energy has been increased due automation in house hold and industrial applications. This increased the demand for renewable energy sources. Renewable energy extraction needs huge amount of investment for resources; it leads to increase in cost of initial extraction. Therefore energy has to be managed carefully, so different power electronic converters have been designed for the reliable distribution of energy [1]. Multilevel converters are gaining importance because high power can be managed with medium-voltage switches. They present a new set of features that are well suited for use in reactive power compensation. The unique structure of multilevel voltage source inverters allows them to reach high voltages with low harmonics. The multilevel converters are mostly used in power generation, transmission, power quality devices like FACTS, variable speed drives, reactive power compensation and water plants [2].

The general structure of multilevel inverter is to synthesize a sinusoidal voltage from several levels of dc voltages. As the number of levels increases the synthesized output waveform has more steps which produce a staircase wave that approaches a desired waveform. Also, as more steps are added to the waveform the harmonic distortion of the output wave decreases. According to load requirement, component specification and improved output response, the multilevel inverters (MLI) are mainly classified as (i).Diode clamped multilevel inverter (DCMLI) (ii).Capacitor clamped (flying capacitor) multilevel inverter (FCMLI) and (iii).Cascaded multilevel inverter(CMLI). The diode clamped multilevel inverter has the advantages of high inverter efficiency, reduced usage of filters and simpler control method. But this topology has some drawbacks such as excessive use of clamping diodes, difficulty in controlling the real power flow in multi converter systems and diode reverse recovery of clamping diodes would become a major design challenge in high power applications. In FCMLI, a large number of capacitors are used to clamp the voltage. This topology has the major advantages of capability to provide uninterruptible power during power outages due to the use of large amounts of storage capacitors, control of both real and reactive power, lower harmonic content and switch combination redundancy. In spite of these advantages, this topology is having drawbacks of excessive number of storage capacitors, inverter control can be very complicated and switching losses are high for real power transmission. Unlike DCMLI and FCMLI, CMLI topology requires least number of components to achieve same voltage levels. It ensures optimized circuit layout and soft switching techniques can be used to reduce the switching losses and device stresses. Cascaded topology reduces common mode voltage which reduces the damage of insulation of motor and also reduces the switching frequency which reduces the switching losses [3]-[9].

This paper is organized as follows. Section II deals with the analysis of cascaded half bridge multilevel inverter topology. It is followed by review of different PWM techniques in section III. The simulation results are presented and the harmonic analysis is discussed in section IV.

2. Cascaded Half Bridge Multilevel Inverter Topology

In cascaded half bridge multilevel inverter, a series of half bridge inverter units are connected using separate dc sources which may be obtained from batteries, fuel cells or solar cells. The main function is to synthesize desired voltage from separate dc sources. The output voltage is the stack of the voltages generated from individual modules. To synthesize N level output, N-1 modules are required. The number of switching devices is equal to 2(N-1). A five level cascaded half bridge topology is shown in fig. 1.The output voltage of five level inverter swings between $+2V_{dc}$ and $-2V_{dc}$.

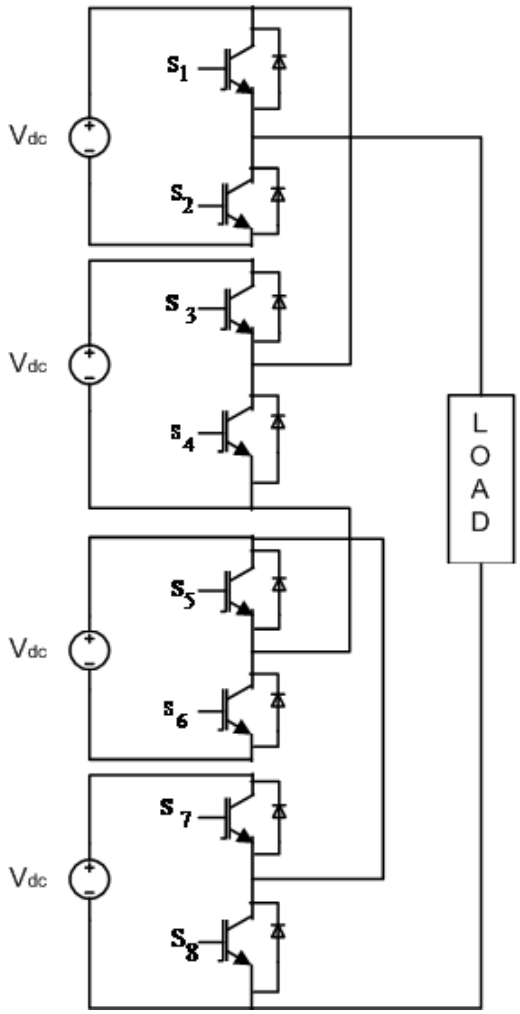

Figure 1: Configuration of five levels cascaded half bridge multilevel inverter

3. Modulation Techniques

There are several modulation strategies to control the multi level converters. The most commonly used is the multi carrier PWM technique. The advantage of multi carrier PWM strategies is that it can be easily implemented to low voltage modules.

3.1 Principles of multi carrier PWM

The carrier based Pulse width modulation is achieved by comparing the reference sinusoidal signal with high frequency triangular carrier signal. To generate pulse pattern for N level converter N-1 carrier signals are required. All the carrier signals have the peak to peak amplitude A_c and frequency f_c. The sinusoidal reference waveform has a frequency f_r and peak to peak amplitude A_r. The reference signal is positioned at the Centre of the carrier set and continuously compared with the carriers. At every instant, whenever the magnitude of reference wave is greater than a carrier wave the output goes to 1 and a positive ongoing pulse is generated. As the reference falls below each carrier the output goes to 0 and a negative ongoing pulse is generated. The multi carrier PWM techniques are further classified as: Level shifted PWM techniques and Phase shifted PWM techniques. In general the amplitude modulation index (m_a) for level shifted PWM is given as:

$$m_a = \frac{2A_r}{(N-1)A_c} \quad (1)$$

Similarly, the amplitude modulation index for phase shifted PWM is given by:

$$m_a = \frac{A_r}{(\frac{A_c}{2})} \quad (2)$$

The frequency modulation index (m_f) for level shifted and phase shifted PWM techniques are given as:

$$m_f = \frac{f_c}{f_r} \quad (3)$$

3.2 Phase Disposition PWM (PDPWM)

In this method all the carriers above and below zero reference line are in same phase as shown in fig 2. The PDPWM is the widely used strategy for Modular Multilevel converters because it provides load voltage and current with lower harmonic distortion [10].

3.3 Phase opposition disposition PWM (PODPWM)

In this method all the carriers have the same frequency and equal amplitude. All the carriers above the zero value reference are in phase among them and the carriers below zero value reference are in phase opposition with respect to above carriers (180 degrees phase shifted) as shown in fig 3 [10].

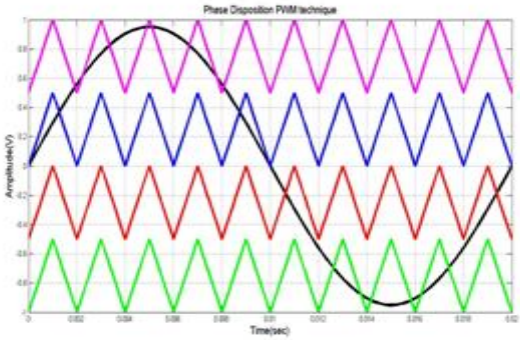

Figure 2: Phase Disposition PWM

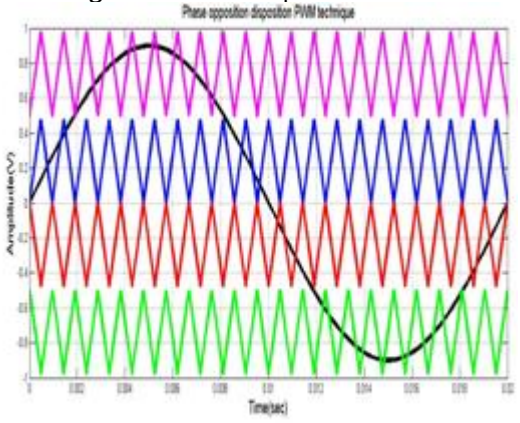

Figure 3: Phase opposition Disposition PWM

3.4 Alternate Phase opposition disposition PWM (APODPWM)

In this method all the carriers have the same frequency and amplitude. All the carriers have 180 degrees phase shift between them as shown in fig 4 [10].

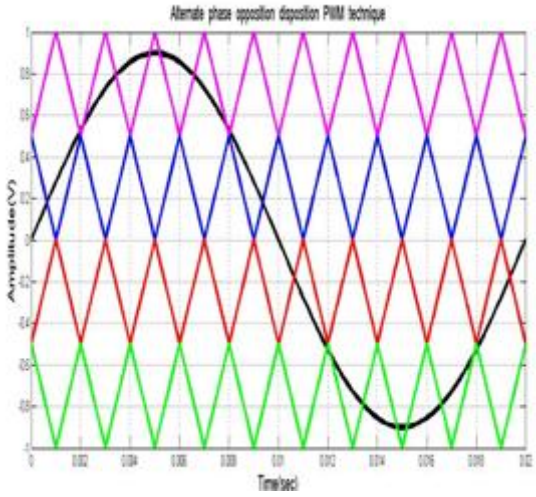

Figure 4: Alternate Phase opposition Disposition PWM

3.5 Phase shifted PWM (PSPWM)

The phase shifted multicarrier PWM technique has its performance parameters closest to PDPWM strategy. All the carriers have same amplitude and frequency but the carriers are displaced by shifting their phase as shown in Fig. 5. The carrier waves are phase shifted so that the switching instants of different sub modules are offset in time, thus reducing the harmonics in the output voltage. The phase shift can be done by choosing any delay but to achieve minimum harmonic distortion the delay is given by (4), where T_S is the switching period and N indicates number of levels. This technique ensures substantial reduction in losses as each sub module switches at only a fraction of the overall switching frequency. Even though PSPWM is easy to implement the control becomes complex as the number of modules increases. This can be overcome by lowering the switching frequency for individual sub modules but it leads to voltage fluctuations in the sub module voltages [10].

$$\Delta = \frac{T_S}{N-1} \quad (4)$$

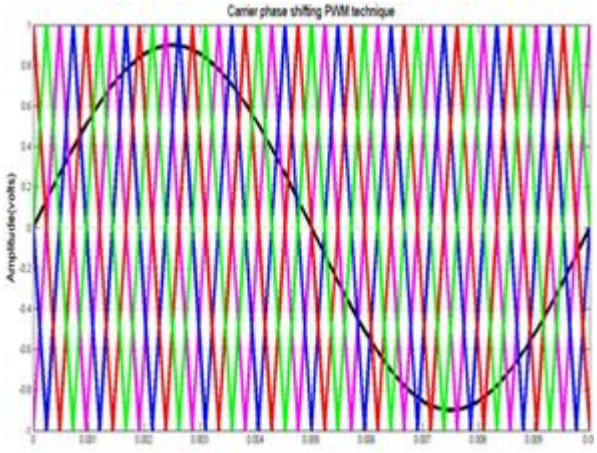

Figure 5: Phase Shifted PWM

4. Simulation Results

A 5-level and 21-level cascaded half bridge multilevel inverter are simulated in MATLAB/Simulink using different modulation techniques. The dc bus voltage is taken as 100V and the load parameters are R=20Ω, L=10mH.

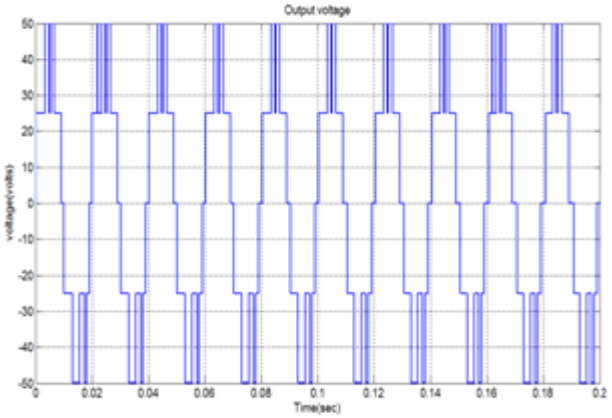

Figure 6: Simulated load voltage of 5-level CMLI using PDPWM

Fig 6 and Fig 7 represents the simulated load voltage and corresponding FFT analysis of 5-level cascaded half bridge inverter using PDPWM. The total harmonic distortion (THD) of output voltage is observed as 26.47% for modulation index m_a=0.9.

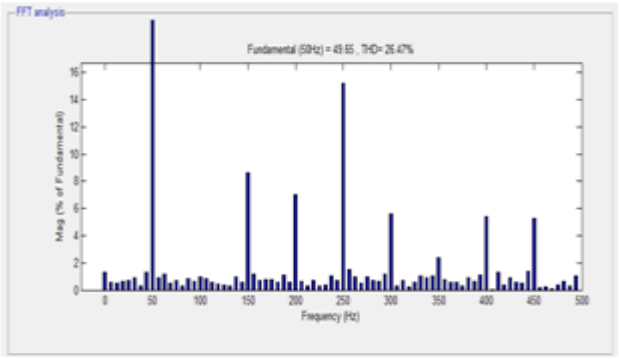

Figure 7: FFT analysis of load voltage using PDPWM

Fig 8 and Fig 9 represents the simulated load voltage and corresponding FFT analysis of 5-level cascaded half bridge inverter using PODPWM. The total harmonic distortion (THD) of output voltage is observed as 29.21%.

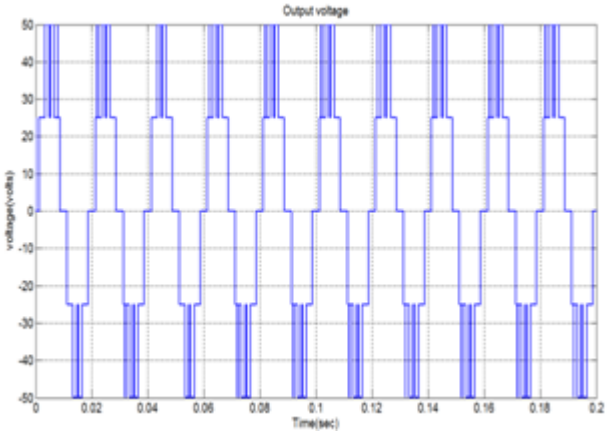

Figure 8: Simulated load voltage of 5-level CMLI using PODPWM

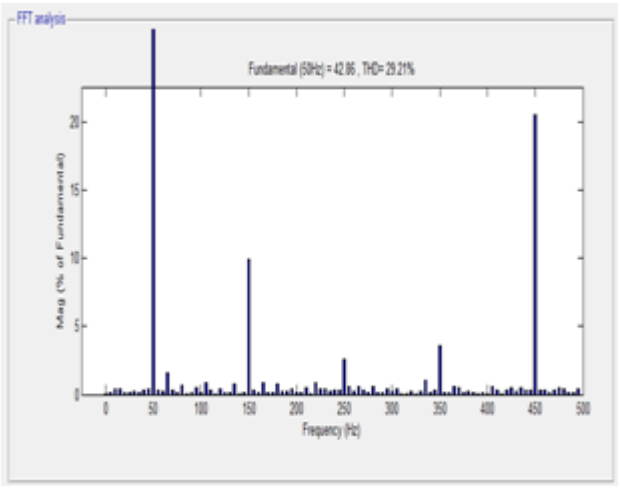

Figure 9: FFT analysis of load voltage using PODPWM

Fig 10 and Fig 11 represents the simulated load voltage and corresponding FFT analysis of 5-level cascaded half bridge inverter using APODPWM. The total harmonic distortion (THD) of output voltage is observed as 27.22%.

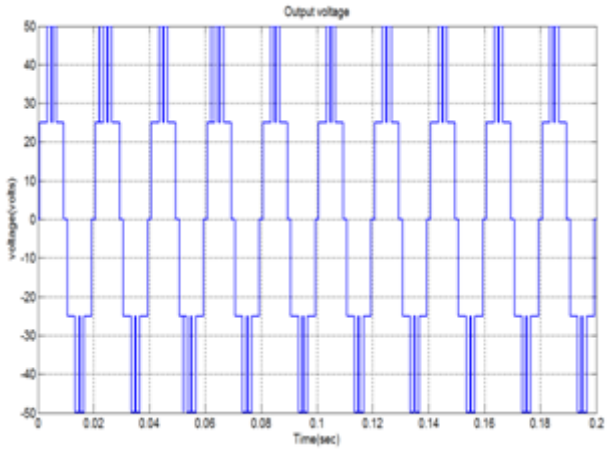

Figure 10: Simulated load voltage of 5-level CMLI using APODPWM

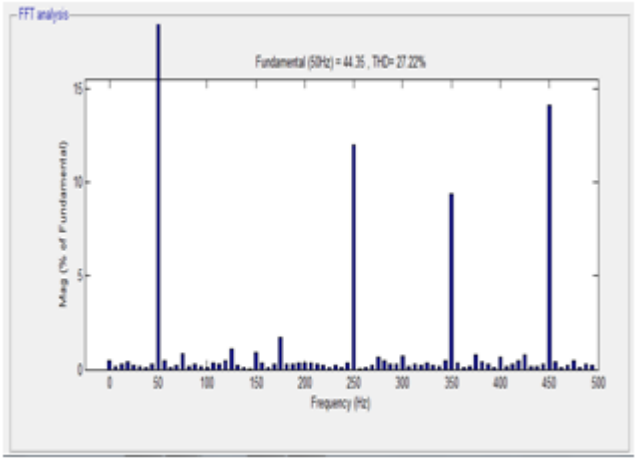

Figure 11: FFT analysis of load voltage using APODPWM

Fig 12 and Fig 13 represents the simulated load voltage and corresponding FFT analysis of 21-level cascaded half bridge inverter using PDPWM. The total harmonic distortion (THD) of output voltage is observed as 4.81%.

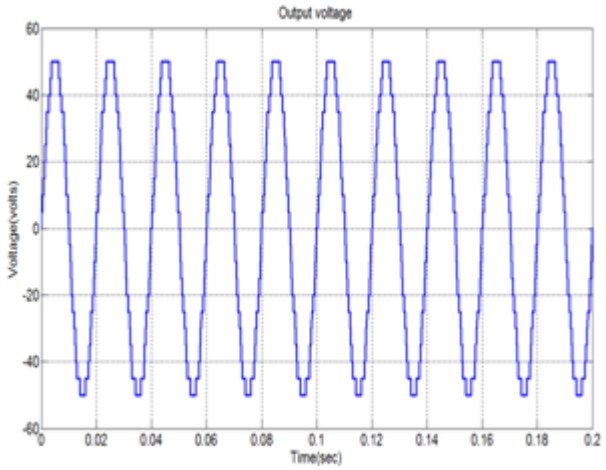

Figure 12: Simulated load voltage of 21-level CMLI using PDPWM

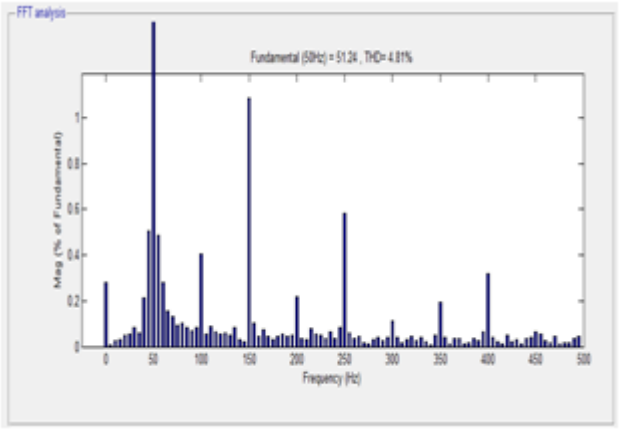

Figure 13: FFT analysis of load voltage using PDPWM

Fig 14 and Fig 15 represents the simulated load voltage and corresponding FFT analysis of 21-level cascaded half bridge inverter using PODPWM. The total harmonic distortion (THD) of output voltage is observed as 4.90%.

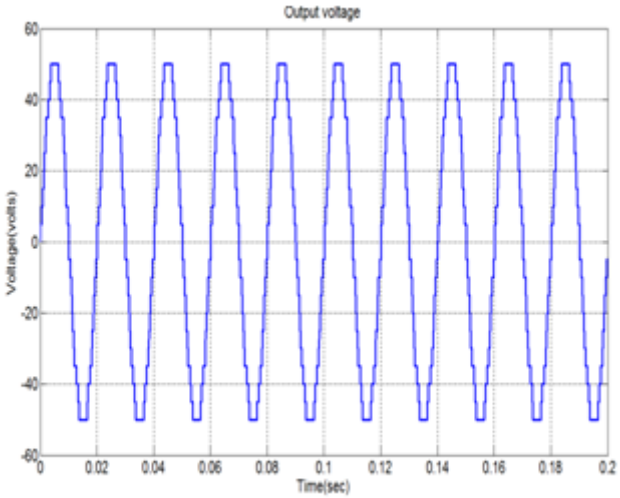

Figure 14: Simulated load voltage of 5-level CMLI using PODPWM

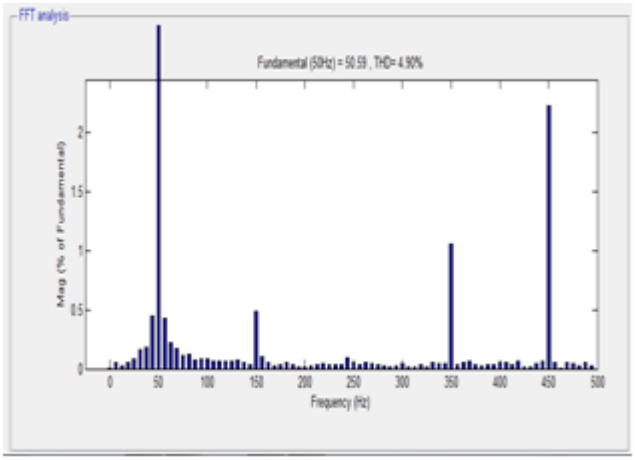

Figure 15: FFT analysis of load voltage using PODPWM

Fig 16 and Fig 17 represents the simulated load voltage and corresponding FFT analysis of 21-level cascaded half bridge inverter using APODPWM. The total harmonic distortion (THD) of output voltage is observed as 4.83%.

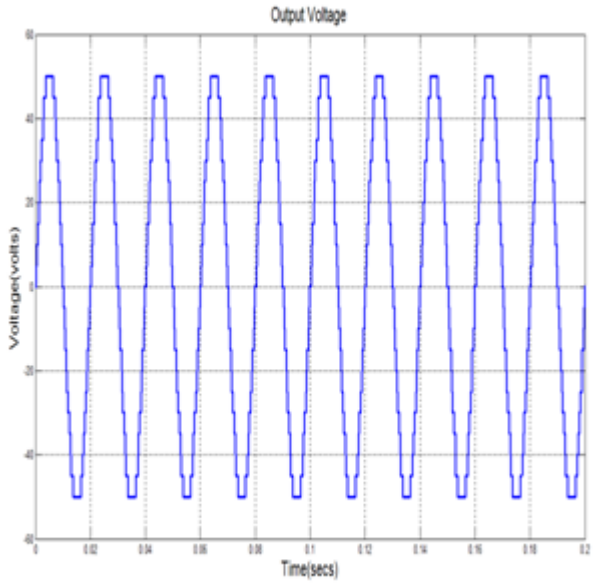

Figure 16: Simulated load voltage of 21-level CMLI using APODPWM

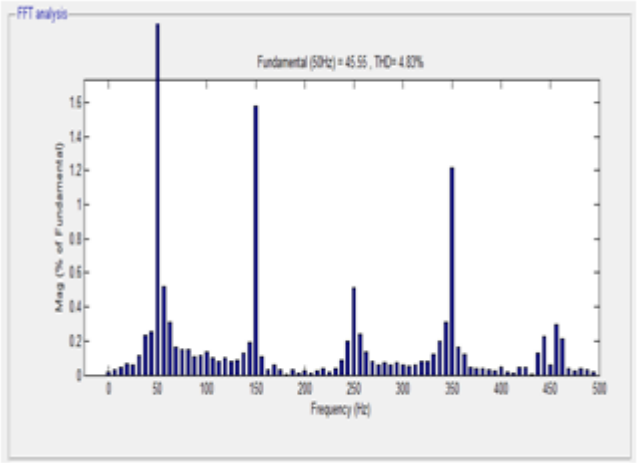

Figure 17: FFT analysis of load voltage using APODPWM

A comparison of total harmonic distortion (%THD) for 5-level and 21-level is shown in table 1. The harmonic analysis for 5-level and 21-level for different modulation indices is shown in Fig 18 and Fig 19. It can be observed that the PDPWM yields lowest harmonic distortion when compared to other methods.

Table 1: Comparison of %THD of 5-level and 21-level CMLI at m_a=0.9

Technique	*5-level*	*21-level*
PDPWM	26.47	4.81
PODPWM	29.21	4.90
APODPWM	27.22	4.83

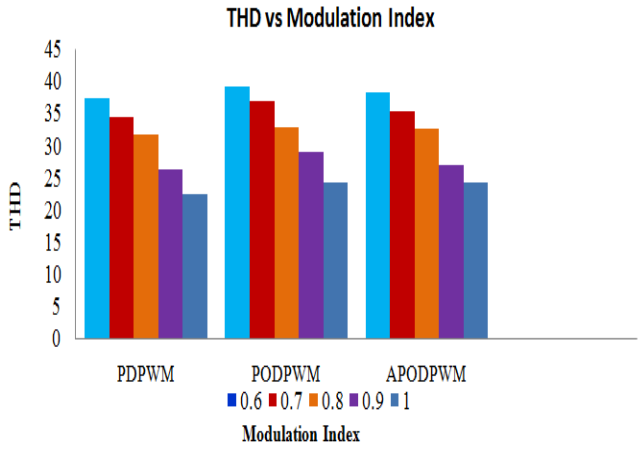

Figure 18: Harmonic spectrum of 5-level CMLI for different modulation indices

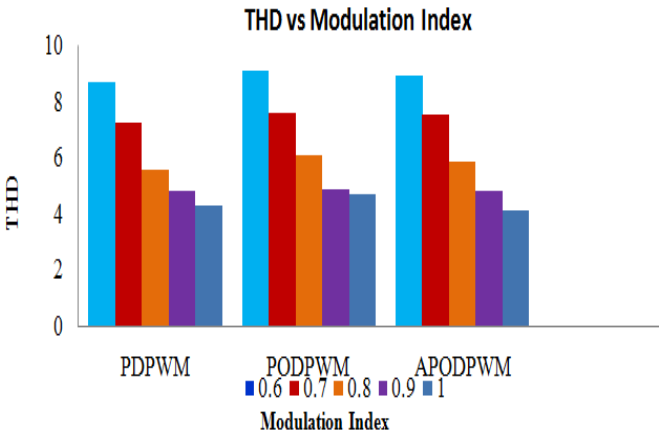

Figure 19: Harmonic spectrum of 21-level CMLI for different modulation indices

5. Conclusion

In this paper, performance of cascaded half bridge topology for different modulation techniques has been reviewed. 5-level and 21-level inverters are simulated using different PWM techniques in MATLAB/Simulink. A comparative analysis of these converters in terms total harmonic distortion has been presented. As the number of levels is increased, the total harmonic distortion is reduced considerably. Among the various PWM techniques, PDPWM proved to be the simplest strategy with lowest THD at different modulation indices.

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