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Analysis of Implicit Type Pulse Triggered Flip Flop

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Abstract: ***In this paper, analysis of the pulse triggered flip flop is done. We compare the several styles of implicit type pulse triggered flip flop. In order to reduce the power consumption, conditional enhancement technique is used which speed-up the discharge path along the critical path. This was confirmed by simulation using 90nm technology, 1.0V power supply and clock frequency of 500MHz***

Keywords: flip flop, low power, VLSI, pulse triggered.

1. Introduction

In the several past years, low power has emerged as a principal theme in today's industry. The need of low power has become more important than area and performance because low power increases the portability of any system which is the main demand in very large scale integration (VLSI) chips.

Flip flop is one of the most power consuming component is digital design used in many modules like register file, shift register and many more. Flip flop consist of the clocking system which consist of clock distribution network and storage network, which is the major part of the power consumption(consuming almost 50% of the total power consumption).

We have considered pulse triggered flip flop over the master slave flip flop because master slave flip flop works on two stage generation, first master stage second slave stage and are characterized by hard edge property whereas pulse triggered flip flop reduces two stage to single stage and is characterized by soft edge property, negative setup time and have small Data to Q delay. Pulse triggered flip flop are consist of pulse generator for generating the strobe signal and latch for storing the data.

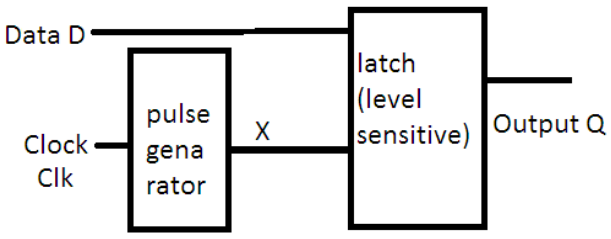

Figure 1: Pulse triggered flip flop

Pulse Triggered flip flop is characterized into two different type of flip flop as: implicit type and explicit type pulse triggered flip flop. This characterization is based on pulse generation. In implicit type, pulse generation is done inside the flip flop example IPDCO, MHLFF, SCCER. In explicit type flip flop the pulse is externally generated. In this paper the analysis of different type of implicit type pulse triggered flip flop example EP-DCO, SCDFF.

2. Conventional Implicit Type P-FF Design

A. IPDCO

It is implicit pulsed-Data close to output shown in figure 2. It consists of mainly two parts, pulse generator and semi dynamic latch design. Pulse generator works on the And logic. Inverter e use to latch the data and inverter I4 and I5 are used to hold the data and inverter I6 and I7 are used to latch the data. Clock signal takes the complementary signal with a delay to generate a transparent window equal in size to delay by inverter I1-I3. The main advantage of this flip flop is it occupies smaller area and also it uses single phase clocking. The disadvantages of this flip flop are larger switching power and there is a larger capacitance load. It results in speed and performance degradation.

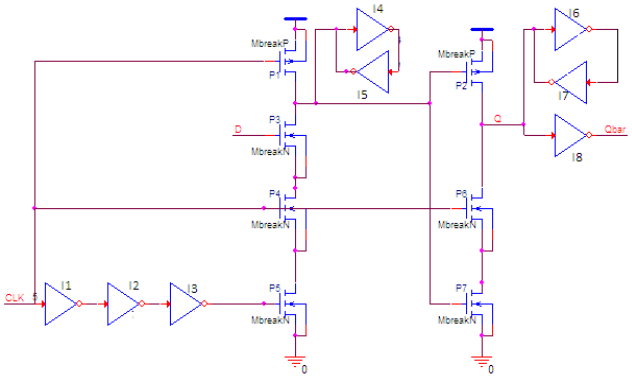

Figure 2: IPDCO

B. MHlFF

It is modified hybrid latch flip flop. This is a modified version of pulse flip flop which employ static latch structure. In this type of flip flop node X is not precharge periodically by clock signal. In this node X depends on output Q data. When Q is low, the node X is maintained high because it is controlled by PMOS transistor P1 which reduce unnecessary discharging. The disadvantage of this design is during '0' to '1' transistor there is no longer D-to-Q delay and when data D and output Q both are high there is extra power consumption because of floating node.

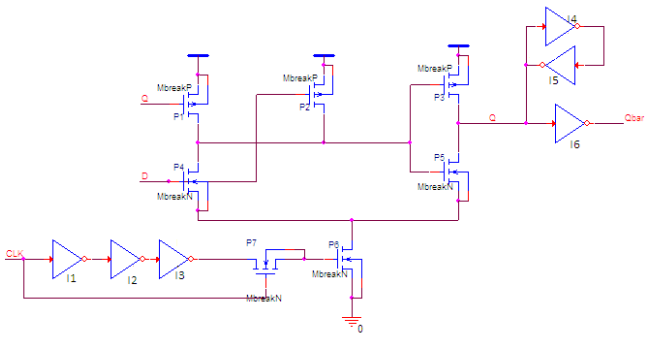

Figure 3: MHLFF

C. SCCER

It is single ended conditional capture energy recovery. This design uses conditional discharge technique in which controlling of discharge path is done by eliminating the switching activity when the input is at HIGH. It has extra NMOS transistor P4 which is control by Q-bar which eliminates the unwanted switching activity (if D=1 there is no discharge).

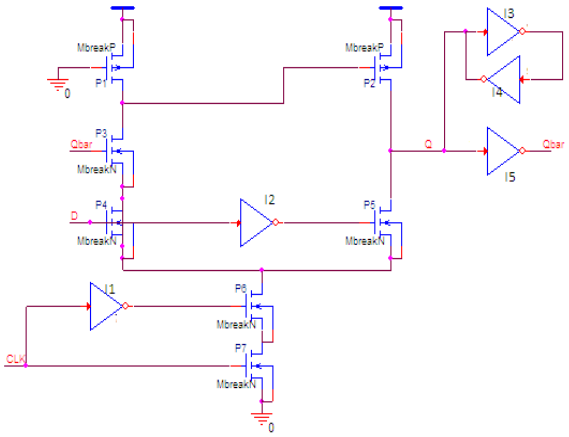

Figure 4: SCCER

D. Pulse Control Flip Flop

In this type of flip flop pulse control enhancement scheme is used. In this, two control schemes are used. First, it reduces the number of nMOS transistor present in the discharge path. Secondly, it place the extra Transistor P8 parallel to P7 forming the pass transistor logic(PTL) base And gate which enhances the pull down strength when input data is '1'. As AND logic are usually complementary making the output node Y low most of the time. Only at the rising edge of the clock both the inputs of AND logic that is both the transistor P7 and P8 turns on making output node Y to high which makes the transistor P9 on for the time span depending upon the inverter I1 and when both the transistor P7 and P8 are off makes the output node Y floating which does not affect the circuit. The longest discharge path is driven by two transistor And logic which helps in speeding up the operation of conduction through parallel transistor P7 and P8. The longest discharge path formed in this circuit is when the input andQbar output both are "1'. For this condition transistor 'P3' is added in the circuit which is usually off and turns on only at longest discharge path situation else it is off due to node X is on most of the time. This transistor gives additional boosting to node Y.

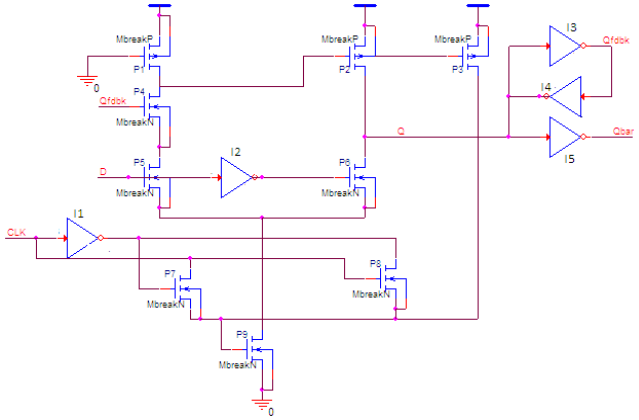

Figure 5: Pulse control Flip Flop

3. Simulations Result and e analysis of Performance Pulse Triggered Flip Flop

The simulations are carried out using orcad p-spice tool at 90nm technologies. All the implicit type pulse triggered flip flop design are simulated to obtain power dissipation and D-to-Q delay and then from the obtained results power-delay product (PDP) is calculated. Simulated are done with power supply of 1.0V and 500MHz clock frequency. All the simulations were done in such way to obtain the trade-off between power and D-toQ delay.

In the simulation setup model the input are generated through buffer and output of flip flop is loaded with a 20fF capacitor and 3ff capacitor at clock buffer. The setup model for simulation in shown in figure 2. The waveform of the simulation results of IPDCO is shown is the figure 3. The waveform shows the output waveform Q, clock pulse clk, input data D.

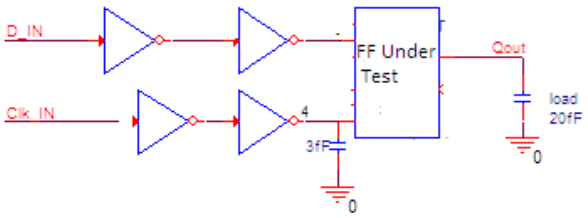

Figure 4: Simulation Setup Model

In addition, table 1 shows the simulation results of various pulse triggered flip flop explained in section 2. The power consumption is measured for different data activity factors i.e., at 100%, 50%, 25%, 0%(all 0's and all 1's). D-to-Q delay, setup time and hold time for 50% data activity are calculated at same frequency.

Because of the shorter discharge path and less number of nMOS transistor pulse control flip flop have the lowest power consumption and lowest delay. Table 1 summarizes many more important parameters related to these pulse triggered flip flop design. These include number of transistor, setup time, hold time, min D-to-q delay, optimal PDP and the clock tree power. The number of transistor of the pulse control flip flop is not the lowest one but its layout area is smaller than all.

Table 2 shows the leakage power consumption of all the implicit type pulse triggered flip flop in a stand by mode. For this we have assume the output Q as "0" when the input data is "1" to exclude the extra power consumption which is coming from the discharge of the internal node. The different clock and input data is applied and it is evaluated that minimum leakage power consumption is for pulse control FF due to shorter discharge path.

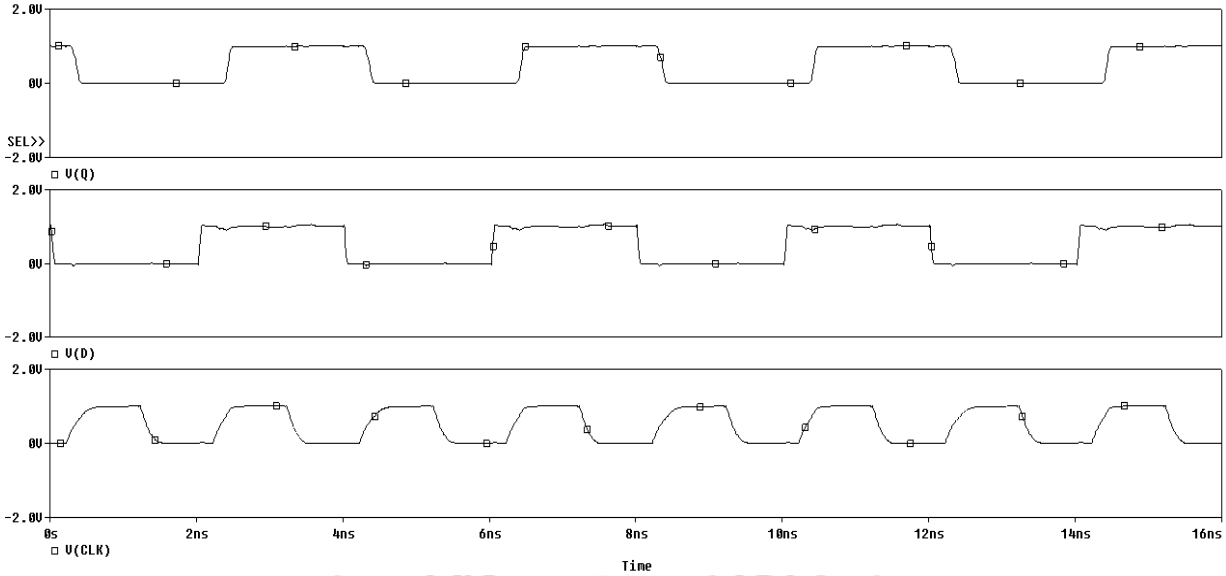

Figure 6: Waveform of IPDCO

Table 1: Comparison of various parameters of P-FF

FF-properties	*IPDCO*	*MHLLF*	*SCCER*	*Pulse control FF*
Number of transistors	23	19	17	19
Setup time	-63.40875p	-52.94585p	-87.08199p	-35.83660p
Hold time	83.46603p	94.00279p	132.82237p	99.91470p
D-to-Q delay	85.26985p	50.39905p	48.50285p	44.31183p
Clk tree power	10.41662u	11.44199u	12.42559u	8.44869u
Avg Power (100%)	33.63076u	24.26441u	48.82760u	23.69463u
Avg Power (50%)	26.54047u	17.89674u	41.04685u	16.33088u
Avg Power (25%)	22.99401u	14.84493u	36.93289u	12.61928u
Avg Power (0%) all-one	30.48862u	12.16193u	32.76998u	9.07649u
Avg Power (0%) all-zero	12.88690u	13.93788u	34.78829u	10.96937u
Optimal PDP	3.59658f	0.85360f	1.89309f	0.69216f

Table 2: Leakage power consumption

Design/(clk,data)	**(0,0)**	**(0,1)**	**(1,0)**	**(1,1)**
IPDCO	14.13759n	17.42209n	20.44268n	20.44265n
MHLLF	998.96393n	532.26180n	2.76190u	1.26048u
SCCER	14.26057n	8.50696u	14.18575n	8.50696u
Pulse CONTROL FF	17.57839n	12.52954n	17.54398n	8.18108u

4. Conclusion

In this paper, various different design of implicit type pulse triggered flip flop are simulated and compared. Pulse control scheme flip flop design consumes lowest power because number of nMOS transistor is reduced and conditional enhancement scheme is also employed to reduce the discharge path. Simulation results gives the PDP, setup time, hold time and clock tree power of various implicit type P-FF like MHLFF,IPDCO, SCCER.

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