Analysis of Implicit Type Pulse Triggered Flip Flop

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Abstract: In this paper, analysis of the pulse triggered flip flop is done. We compare the several styles of implicit type pulse triggered flip flop. In order to reduce the power consumption, conditional enhancement technique is used which speed-up the discharge path along the critical path. This was confirmed by simulation using 90nm technology, 1.0V power supply and clock frequency of 500MHz

Keywords: flip flop, low power, VLSI, pulse triggered.

1. Introduction

In the several past years, low power has emerged as a principal theme in today’s industry. The need of low power has become more important than area and performance because low power increases the portability of any system which is the main demand in very large scale integration (VLSI) chips.

Flip flop is one of the most power consuming component in digital design used in many modules like register file, shift register and many more. Flip flop consist of the clocking system which consist of clock distribution network and storage network, which is the major part of the power consumption(consuming almost 50% of the total power consumption).

We have considered pulse triggered flip flop over the master slave flip flop because master slave flip flop works on two stage generation, first master stage second slave stage and are characterized by hard edge property whereas pulse triggered flip flop reduces two stage to single stage and is characterized by soft edge property, negative setup time and have small Data to Q delay. Pulse triggered flip flop are consist of pulse generator for generating the strobe signal and latch for storing the data.

2. Conventional Implicit Type P-FF Design

A. IPDCO

It is implicit pulsed-Data close to output shown in figure 2. It consists of mainly two parts, pulse generator and semi dynamic latch design. Pulse generator works on the And logic. Inverter e use to latch the data and inverter I4 and I5 are used to hold the data and inverter I6 and I7 are used to latch the data. Clock signal takes the complementary signal with a delay to generate a transparent window equal in size to delay by inverter I1-I3. The main advantage of this flip flop is it occupies smaller area and also it uses single phase clocking. The disadvantages of this flip flop are larger switching power and there is a larger capacitance load. It results in speed and performance degradation.

B. MHIFF

It is modified hybrid latch flip flop. This is a modified version of pulse flip flop which employ static latch structure. In this type of flip flop node X is not precharge periodically by clock signal. In this node X depends on output Q data. When Q is low, the node X is maintained high because it is controlled by PMOS transistor P1 which reduce unnecessary discharging. The disadvantage of this design is during ‘0’ to ‘1’ transistor there is no longer D-to-Q delay and when data D and output Q both are high there is extra power consumption because of floating node.
C. SCCER

It is single ended conditional capture energy recovery. This design uses conditional discharge technique in which controlling of discharge path is done by eliminating the switching activity when the input is at HIGH. It has extra NMOS transistor P4 which is control by Q-bar which eliminates the unwanted switching activity (if D=1 there is no discharge).

D. Pulse Control Flip Flop

In this type of flip flop pulse control enhancement scheme is used. In this, two control schemes are used. First, it reduces the number of nMOS transistor present in the discharge path. Secondly, it place the extra Transistor P8 parallel to P7 forming the pass transistor logic(PTL) base And gate which enhances the pull down strength when input data is ‘1’. As AND logic are usually complementary making the output node Y low most of the time. Only at the rising edge of the clock both the inputs of AND logic that is both the transistor P7 and P8 turns on making output node Y to high which makes the transistor P9 on for the time span depending upon the inverter I1 and when both the transistor P7 and P8 are off makes the output node Y floating which does not affect the circuit. The longest discharge path is driven by two transistor And logic which helps in speeding up the operation of conduction through parallel transistor P7 and P8. The longest discharge path formed in this circuit is when the input and Qbar output both are ‘1’. For this condition transistor ‘P3’ is added in the circuit which is usually off and turns on only at longest discharge path situation else it is off due to node X is on most of the time. This transistor gives additional boosting to node Y.

3. Simulations Result and e analysis of Performance Pulse Triggered Flip Flop

The simulations are carried out using orcad p-spice tool at 90nm technologies. All the implicit type pulse triggered flip flop design are simulated to obtain power dissipation and D-to-Q delay and then from the obtained results power-delay product (PDP) is calculated. Simulated are done with power supply of 1.0V and 500MHz clock frequency. All the simulations were done in such way to obtain the trade-off between power and D-to-Q delay.

In the simulation setup model the input are generated through buffer and output of flip flop is loaded with a 20fF capacitor and 3fF capacitor at clock buffer. The setup model for simulation in shown in figure 2. The waveform of the simulation results of IPDCO is shown is the figure 3. The waveform shows the output waveform Q, clock pulse clk, input data D.
Table 2 shows the leakage power consumption of all the implicit type pulse triggered flip flop in a standby mode. For this we have assume the output Q as “0” when the input data is “1” to exclude the extra power consumption which is coming from the discharge of the internal node. The different clock and input data is applied and it is evaluated that minimum leakage power consumption is for pulse control FF due to shorter discharge path.

Table 2: Leakage power consumption

<table>
<thead>
<tr>
<th></th>
<th>IPDCO</th>
<th>MHLLF</th>
<th>SCCER</th>
<th>Pulse control FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design(clk,data)</td>
<td>(0,0)</td>
<td>(0,1)</td>
<td>(1,0)</td>
<td>(1,1)</td>
</tr>
<tr>
<td>IPDCO</td>
<td>14.13759n</td>
<td>17.42293n</td>
<td>20.44268n</td>
<td>20.44265n</td>
</tr>
<tr>
<td>MHLLF</td>
<td>998.96393n</td>
<td>532.26180n</td>
<td>2.76190u</td>
<td>1.26048u</td>
</tr>
<tr>
<td>SCCER</td>
<td>14.26057n</td>
<td>8.50696u</td>
<td>14.18575n</td>
<td>8.50696u</td>
</tr>
<tr>
<td>Pulse CONTROL FF</td>
<td>17.57839n</td>
<td>12.52954n</td>
<td>17.54398n</td>
<td>8.18108u</td>
</tr>
</tbody>
</table>

4. Conclusion

In this paper, various different design of implicit type pulse triggered flip flop are simulated and compared. Pulse control scheme flip flop design consumes lowest power because number of nMOS transistor is reduced and conditional enhancement scheme is also employed to reduce the discharge path. Simulation results gives the PDP, setup time, hold time and clock tree power of various implicit type P-FF like MHLFF, IPDCO, SCCER.

References


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