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Design and Optimization of LDO Regulator with MTCMOS Techniques

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Abstract: ***Advances in VLSI technology changed that to allow the creation of System-on-Chip (SoC) devices that integrated those discrete components on a single chip. The most obvious driver for low-power environments leads to increase the demand for battery operated application. Highly accurate Low Drop-Out (LDO) regulators in power supply ICs are typically under 500mA, and frequently used in a wide range of electronic products. LDOs provide a power management solution and satisfying their needs like low power, space-conscious design etc. The main characteristic of the LDO regulator design is to minimize the quiescent current and dropout voltage so as to provide high efficiency. The proposed LDO regulator uses ultra-low quiescent class-AB error amplifier (ERR AMP) and a slew-rate (SR) enhancement circuit to minimize the effect of capacitance and speed up transient response designed in the 180nm technology. The MTCMOS design technique is used to reduce the quiescent current than conventional LDO.It increased the demand for low-cost energy-constrained system applications. The proposed LDO design is simulated by using the cadence analog environment.***

Keywords: Power supply IC, Class- AB error amplifier, Low-dropout regulator, Slew rate

1. Introduction

Power-management-units (PMU) need to be more efficient than ever and integrated circuits (ICs) to power regulation and management have become one of the fastest growing segments of the electronic industry. Every electronic device needs a power-source to work. In mobile devices this source is the battery. The battery management is very important since it is the good use of the battery energy that allows the devices to become more and more autonomous. Therefore, when designing a circuit, the designer needs to target the maximum efficiency. The power management unit is responsible for a balanced distribution of energy according to the consumption of the further circuits and the state of operation (e.g. the devices need less power when they are in the standby mode. A PMU is composed by three types of systems: DC-DC converters and two types of LDOs [1]. One of the most important challenges today in designing electronic applications is to minimize the power consumption of the system.

To accomplish this, most systems utilize various low power modes which help to minimize the overall power consumption [2]. Low Dropout Linear Voltage Regulators (popularly referred to as LDOs) are common building blocks in any power system and the choice of linear regulator can have an important impact on the overall system power consumption. A series low-dropout regulator is a circuit that provides a well specified and stable dc voltage whose input to output voltage difference is low. The dropout voltage is defined as the value of the input/output differential voltage where the control loop stops regulating. To complicate this choice, it is often required that the LDO not only feature ultra−low quiescent current but should additionally provide good dynamic performance to assure stable, noise−free voltage rail, suitable for sensitive circuits [3]. LDO regulators have become the power management ICs that are widely used in portable electronics products to realize low profile, low dropout, and low supply current. Historically, the standard for supply voltages was ±15 V. In recent years the trend is towards lower supply voltages. This is partially due to the processes used to manufacture integrated circuits. One of the enabling technologies of this increase is the reduction of size of the transistors used in the process [4][5].Initially the voltage regulator function was implemented using discrete low dropout linear regulators, LDOs. Today most phones are built using more integrated power management solutions, that include a large number of regulators, LDOs and switching regulators, battery chargers, sequencing circuitry, supervisory and housekeeping circuitry [6][7]. For the majority of applications within portable devices where loads are operated from a battery source, the LDO offers a simple, small and cost-effective solution [8]. Other LDO applications include PC motherboards, graphic cards, post-regulation in switching power supplies, telecom equipment and consumer applications such as HDTVs. In addition, automotive applications continue to use LDOs for their low switching noise and low cost [9].Minimizing quiescent current and dropout voltage while maintaining good regulation and fast response is the main issue of the LDO regulator design.

The rest of the paper is organized as follows. Section I gives the introduction about power management IC and their importance of LDO. Section II discusses the LDO regulator design. Section III explains the proposed LDO regulator design and their characteristics. Section IV explains simulation results and discussion for proposed LDO regulator design. Section V deals with conclusion of proposed LDO design.

2. LDO Regulator Design

A low-drop out or LDO regulator is a linear voltage regulator which can operate with a very small input–output differential voltage. The advantages of a low dropout voltage include a lower minimum operating voltage, higher efficiency operation and lower heat dissipation. The basic function of voltage regulation provides clean, constant, accurate voltage to a circuit. Voltage regulators are a fundamental block in the power supplies of most all-electronic equipment. A voltage

regulator is designed to automatically maintain a constant voltage level. A voltage regulator may be a simple "feed-forward" design or may include negative feedback control loops. It may use an electromechanical mechanism, or electronic components. In automobile alternators and central power station generator plants, voltage regulators control the output of the plant. In an electric power distribution system, voltage regulators may be installed at a substation or along distribution lines so that all customers receive steady voltage independent of how much power is drawn from the line.

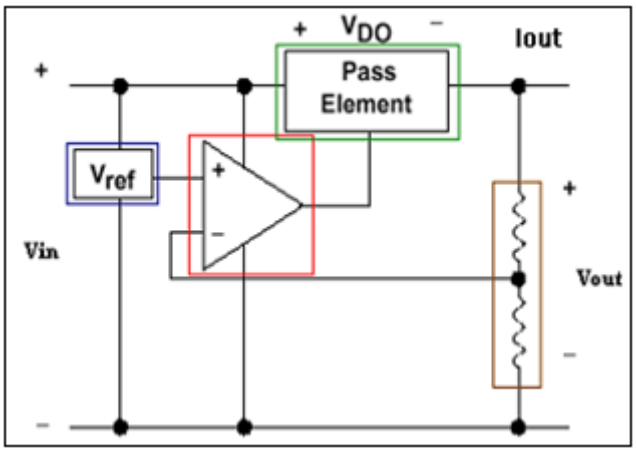

Figure 1: Basic LDO Regulator Structure

Fig.1 shows the basic LDO regulator structure. It consist of voltage reference, pass element, error amplifier and feedback resistors. The voltage reference provides a constant output voltage which will be compared with the output voltage from the feedback network. The pass element provides the output current needed to drive any load. The output current is controlled by the error amplifier output. The error amplifier produces an error signal whenever the feedback sensed output differs from the reference voltage and then the feedback network produces the output voltage (voltage divider).

A.Types of power supply ICs:

LDO regulator IC is a series type power supply IC. Power supply ICs are generally divided into 3 types, namely Series Regulators, Shunt Regulators, and Switching Regulators. Series type and Shunt type are also known as linear regulators.

1) *Series regulators:* Series regulators are connected serially between the power source and the load, to remove irregularities in the power source and thus provide a stable voltage to the load.
2) *Shunt regulators:* Shunt regulators, as the name implies, control the voltage at the load by dividing (Shunt) the current which flows to the load. The voltage of the supply is measured by the external resistors, and the output voltage is then kept constant by adjustments within the shunt regulator. The output voltage is then adjusted by changing the external resistors.
3) *Switching regulators:* Switching regulators are divided into insulating type (AC-DC convertor) and non-insulating type (DC-DC converter). As the name suggests, by switching the input ON/OFF continuously, the IC changes the voltage level and smoothens the output, and unlike the linear regulator, decreasing the voltage (step-down) and increasing the voltage (step-up) are both possible. It can handle large currents without much heat dissipation and is also highly efficient [10].

B. Electrical characteristics

[1] Output voltage: As a power supply IC, the output voltage characteristics of an LDO regulator is the most important. The specification linked with output voltage is output voltage accuracy.
[2] *Input voltage:* Input voltage is the acceptable voltage range for the LDO regulator's input.
[3] *Drop-out voltage:* Dropout voltage is the minimum difference between input voltage and output voltage for which the regulator can still supply the specified current. A low drop-out (LDO) regulator is designed to work well even with an input supply only a volt or so above the output voltage. The input-output differential at which the voltage regulator will no longer maintain regulation is the dropout voltage. Further reduction in input voltage will result in reduced output voltage. This value is dependent on load current and junction temperature.
[4] *Line Regulation:* Line regulation is a measure of the circuit's ability to maintain the specified output voltage with varying input voltage.
Line regulation $=\Delta V_o/\Delta V_i$ (1)
Where V_o & V_i – output and input voltage.
[5] *Load Regulation:* Load regulation is a measure of the circuit's ability to maintain the specified output voltage under varying load conditions.
Load regulation= $\Delta V_o/\Delta I_o$ (2)
Where V_o & I_o – output voltage & current.
[6] *Quiescent current:* Quiescent current in a regulator circuit is the current drawn internally, not available to the load, normally measured as the input current while no load is connected. Quiescent current, or ground current, is the difference between input and output currents. Minimum quiescent current is necessary for maximum current quiescent current is necessary for maximum current efficiency. Quiescent current is defined by
Quiescent current (I_q) $=I_I - I_O$ (3)
Where I_I & I_O- input & output current.
[7] *Transient response:* Transient response is the reaction of a regulator when a (sudden) change of the load current (called the *load transient*) or input voltage (called the *line transient*) occurs. Some regulators will tend to oscillate or have a slow response time which in some cases might lead to undesired results. This value is different from the regulation parameters, as that is the stable situation definition. The transient response shows the behavior of the regulator on a change. This data is usually provided in the technical documentation of a regulator and is also dependent on output capacitance.
[8] *Ripple rejection, output noise voltage:* Ripple rejection is an important characteristic for LDO regulators. Ripples appear as fluctuations superimposed on the LDO regulator's DC output. As LDO regulators are used to provide stable power supply, it is not acceptable to have ripples at the output. Even if the ripples occur at the input of the LDO regulator, a good regulator should be able to remove this disturbance.

C. LDO regulator usage considerations

1) Heat dissipation design: LDO regulator is a series type power supply IC. As such, the load current flows constantly between the input and output pins. Power is also used for the operation of the surrounding circuits. The power dissipation can be calculated as below.

Power dissipation=($V_{in} - V_{out}$) x I_{out} + (V_{in} x I_q) (4)

Where V_{in} & V_{out}- input & output voltage, I_{out}-output current, I_q-quiescent current.

*2) Choosing input capacitors :*For stable operation of the LDO regulator, input and output capacitors are necessary. By considering the stable operation of an LDO regulator, it would be advisable to increase the capacitance of input and output capacitors. However, the rise and fall time will become slower. Reducing the capacitance is not recommended but, if output current is small, input ripple is small, load current fluctuation is small, and the conditions are right stable operation can also be achieved with small capacitors.

3) Overcurrent protection circuit: Overcurrent protection circuit is a circuit which protects the regulator and the connected load from situations when a short circuit occurs at the output pin. It does not immediately shut off the current, but gradually reduces both the current and voltage when specified current is exceeded. Reducing the voltage concurrently is the objective of the LDO regulator which helps reduce heat dissipation within the regulator.

3. Proposed LDO Design

Fig.2 shows the proposed LDO regulator design structure. The proposed LDO design has consist of error amplifier, power transistor, feedback resistors and S/R enhancements circuit. Here the power transistor acts as pass element.

Fig.3 shows the proposed OTA. An operational trans-conductance amplifier (OTA) is a voltage controlled current source (VCCS).The another name of OTA as an error amplifier.

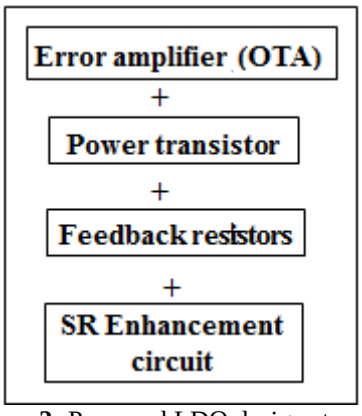

Figure 2: Proposed LDO design structure

[9] Error Amplifier (OTA)

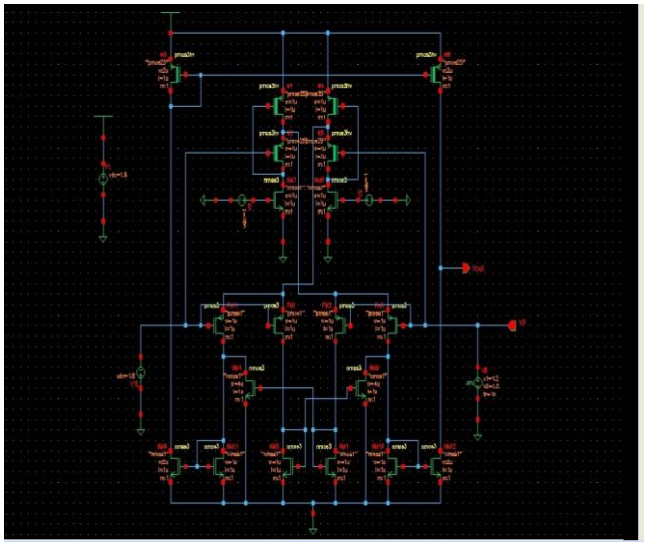

Figure 3: Proposed OTA

The Error amplifier produces an error signal whenever the fed back sensed output differs from the reference voltage. The ERR AMP is designed as a class-AB circuit so that its quiescent current is low with a high output resistance. Multi-threshold CMOS (MTCMOS) is one of the new techniques in CMOS technology. The proposed high speed MTCMOS provides low leakage current compared to other technique. It has to increase the speed of the OTA. It has to use the MTCMOS transistor. The length value of the transistor (1 µm) and width value is 1µ, 2µ, etc. Based up on the value to calculate the slew rate and settling time. Slew rate, SR, is the rate of change in the output voltage caused by a step input. Its units are V/ms. Settling time takes a finite time for a signal to propagate through the internal circuitry of an op amp. Therefore, it takes a period of time for the output to react to a step change in the input.The equation of slew rate is defined below.

Slew Rate=Δv/Δt (mV/ns) (5)

[10] Power Transistor

The area of power transistor is large compared with the other transistor. The Width and length (W/L) ratio of this transistor has large and more than N no of transistors (W/L) are equal to this transistor value. It has to carrying large amount of current and give the protection from leakage due to fabrication of circuit layout. The selected rectangular area has shown a power transistor in Fig.4.

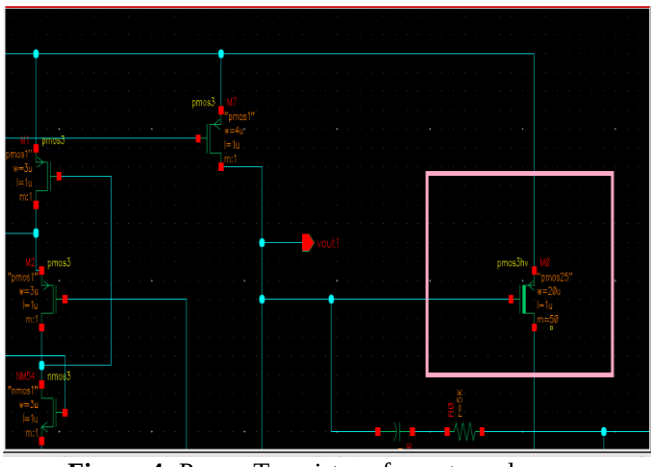

Figure 4: Power Transistor of a rectangular area

[11] Feedback resistors:

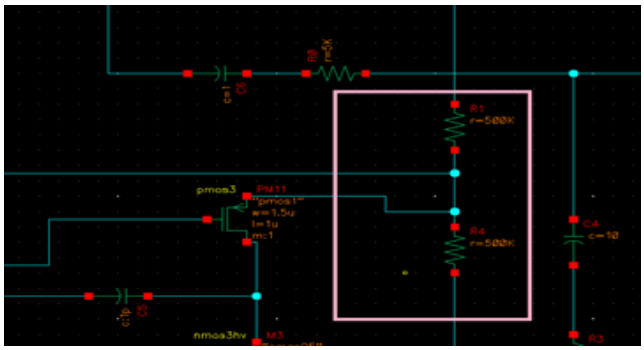

Figure 5: Feedback resistor of a rectangular area

The feedback resistors produces the output voltage and it act as a resistive divided output voltage. The selected rectangular area has shown a feedback resistor in Fig.5.

[12] SR Enhancement structure

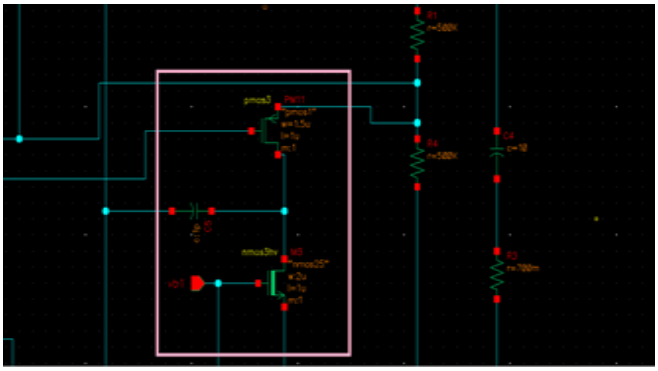

Figure 6: SR enhancement structure for selected area

It consists of a compensation capacitance and nmos3hv transistors .In this nmos3hv is an MTCMOS transistor. The external components should be minimized to reduce the printed-circuit-board layout space and speed up manufacturing process. Hence an output capactiorless LDO regulator has to be preferred.

4. Simulation Results and Discussions

The proposed LDO design structure has shown in Fig.7. MTCMOS technique has to used and simulated by using the cadence analog environment.

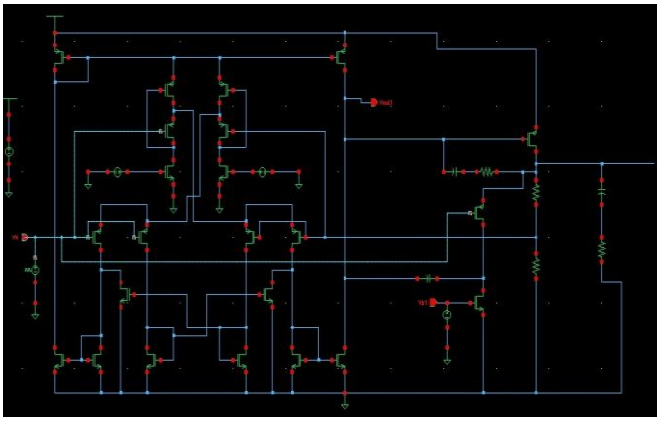

Figure 7: Proposed LDO structure

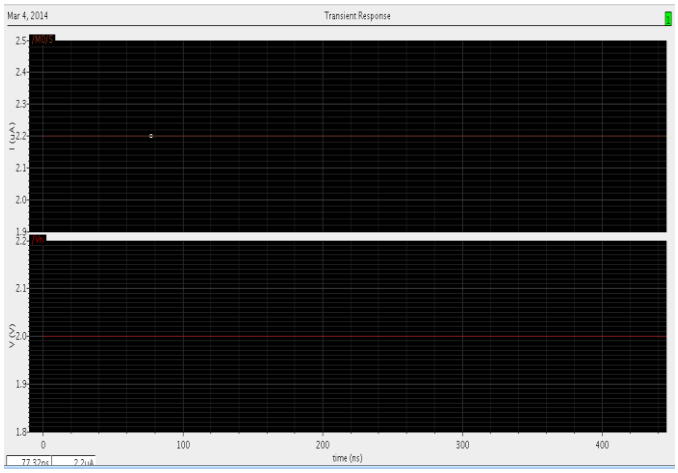

Figure 8: Output of proposed LDO structure

Quiescent current in a regulator circuit is the current drawn internally, not available to the load, normally measured as the input current while no load is connected. The quiescent current has to measured and shown in the Fig.8. Then the quiescent current value has to observe at the drain terminal of power transistor. Here the input voltage value is given as 2V. By using the MTCMOS techniques can easily get the minimum quiescent current value .Then the value is 2.2uA or 0.0220mA.

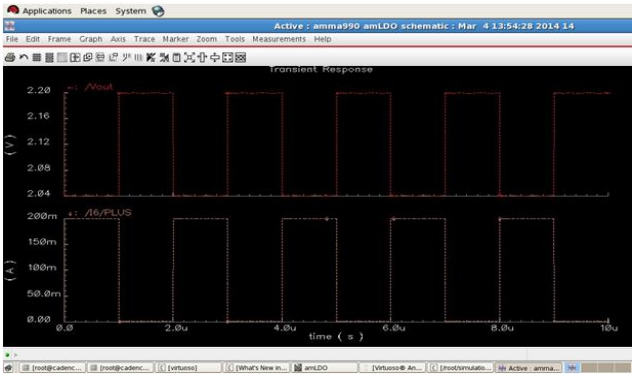

Figure 9: Output for the load current

Fig.9 shows the output for the load current in the LDO regulator design. Depend up on the load current to change the output voltage. It has to determine the ratio between output voltage and current. If the load current value is high then the output voltage is low and vice versa. LDO need minimum current to alive whenever goes to active or standby mode. MTCMOS technique is used to enhance the power efficiency as well as to reduce the quiescent current.

Table 1: Comparison of LDO Parameters

Parameters	Existing System	Proposed System
Quiescent current	0.0415 mA	0.0220 mA
Slew rate of OTA	3.75 mV/ns	12.9 mV/ns
Load regulation	0.001929 V /mA	0.0008 V/mA

Table I shows that the proposed design provides high performance. From the parameter analysis in CADANCE virtuoso environment quiescent current was calculated. From the above conclusion. A new high speed LDO design is proposed for reducing quiescent current and increase the speed of the regulator.. The proposed high speed LDO

design provides low leakage current than the previous methods. MTCMOS technique is used to increase the performance of OTA. Simulation results demonstrate the effectiveness of the proposed LDO in minimizing the quiescent current leads to increase the power efficiency time. It was designed using CADANCE virtuoso environment.

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