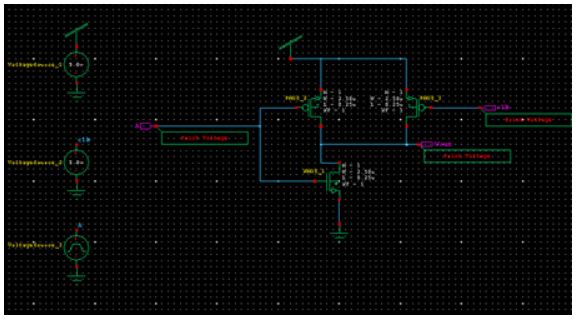

Figure 7: Schematic of Type A Static NOT

In the DML Type-B Static NOT topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode.

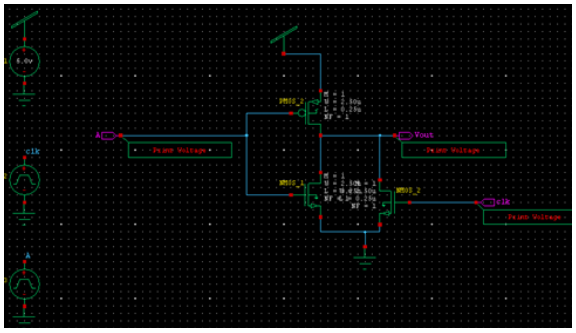

Figure 8: Schematic of Type B Dynamic NOT

The total power consumption in watts for NAND, NOR & NOT logic gates Type A and B is tabulated below.

Table 1: Comparison of NAND, NOR & NOT gates

TYPE	NAND	NOR	NOT
Conventional	6.24E-09W	5.11E-09W	3.35E-09W
Type A Static	5.32E-09W	4.91E-09W	2.37E-09W
Type A Dynamic	9.44E-09W	5.54E-09W	1.15E-09W
Type B Static	6.07E-09W	5.08E-09W	3.27E-09W
Type B Dynamic	7.02E-09W	5.15E-09W	3.26E-09W

4. DML Implementation of a Full Adder

Full Adder is the most used basic circuit in digital electronics. This work has focused on the most commonly used basic CMOS full-adder. Simulations are done for Type A and B Full Adders in Static and Dynamic modes.

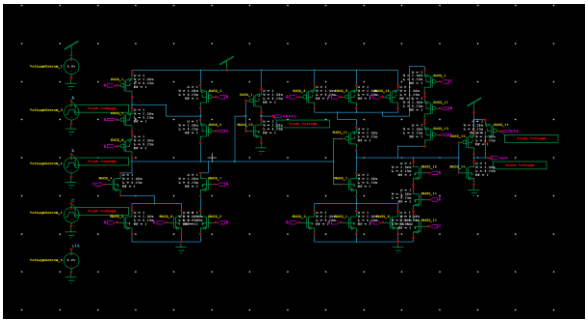

Figure 9: Schematic of Type A Static Full Adder

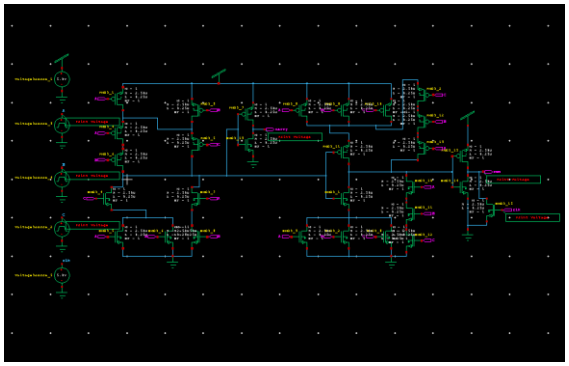

Figure 10: Schematic of Type B Dynamic Full Adder

Table 2: Comparison of Type A & B Full Adder

TYPE	FULL ADDER
CONVENTIONAL	1.978989e-004 watts
TYPE A Static	1.052234e-002 watts
TYPE B Dynamic	3.020891e-003 watts

5. Conclusion

From the results, we can observe that in Static mode there is a power reduction as compared to conventional mode. The DML sizing strategy results in reduced energy dissipation, as compared to conventional static CMOS gates. DML has immunity to process variations, temperature fluctuations, and solving some of the domino's well known drawbacks such as charge sharing, crosstalk noise, and susceptibility to glitches, which intensify with process and voltage scaling. My future extension of this work is the implementation of Power gating techniques so as to further reduce the total power consumption.

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