International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Implementation of Gesture Recognition System for Home Automation using FPGA and ARM Controller

N. Naveenkumar[1], Dr. V. Padmaja[2], Ch. Nagadeepa[3]

[1]M.Tech, ECE Department VNRVJIET, Hyderabad, India

[2]Ph.D, (ECE), Professor, VNRVJIET, Hyderabad, India

[3]M.Tech, (ECE), Asst, VNRVJIET, Hyderabad, India

Abstract: ***New natural methods of control are needed due to the increase in the number of industrial and home appliances that must be controlled. In this paper presents releasable fpga based hand gesture recognition system is proposed by using a method called artificial neural network is used this method mainly used to add learning capabilities of gesture recognition system that can be used for impaired people. The sensor based gestures control system is composed by two subsystems that communicated via radio waves. The first subsystem is a transmitter that has an accelerometer which reads predefined gesture values. The second subsystem is the receiver on which the data processing takes place. Field Programmable Gate Array (FPGA) implementation is an easy an attractive way for hardware implementation. The desired network is modeled, trained and simulated by using Xilinx. Network architecture trained with different methods could be simulated and the network that is best performing for given application is chosen for hardware implementation using vhdl language developed by Xilinx Inc. This HDL design can then be synthesized for implementation in the Xilinx family of FPGA devices.***

Keywords: Accelerometer, gesture recognition system, zigbees, artificial neural network, Field programmable gate arrays.

1. Introduction

Due to the rapid increase of number of industrial or domestic systems that must be controlled it is clear that new methods of control are needed. Gesture recognition is important for developing alternative human-computer interaction modalities that enables humans to interface with machine in a more natural way. are many types of gesture researches like body gesture, finger point movement, etc

Existing System

Previously we have used the mat lab Simulink environment for designing the system, where only software simulation was used but in the proposed system we are going to use the Xilinx system generator and implement it on FPGA

2. Proposed Systems

This paper presents an Accelerometer interface based on hand's gesture recognition. The gestures based control system is composed by two subsystems that communicated via radio waves. The first subsystem is a transmitter that captures the movement of the hand using accelerometers. The second subsystem is the receiver on which the data processing takes place. Artificial Neural Networks (ANN) are used to decide the operation. Field Programmable Gate Array (FPGA) implementation is an easy an attractive way for hardware implementation. Accelerometer consists of x y z if move accelerometer x y z co-ordinates are varying that values are send to the LPC2148 and that will be transmitted to the zigbee .zigbee also transmitted to the receiver side wirelessly. The receiver will received the data ever send transmitter that signals are send to the sparton board that wil be decide the operation that means weather fan or bulb on.

Many networks architecture trained with different methods could be tanned by a VHDL code given application is chosen for developed by Xilinx Inc. This VHDL design can then be synthesized for implementation in the Xilinx family of FPGA devices.

2.1 Block diagram

This intelligent Human-Machine interface presented in this paper is composed by two main subsystems.
1) Transmitter.
2) Receiver.

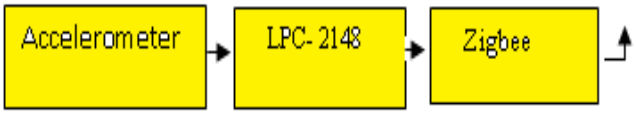


Figure 1: Transmitter

A. Accelerometers

Accelerometers are acceleration sensors. An inertial mass suspended by springs is acted upon by acceleration forces that cause the mass to be deflected from its initial position. This deflection is converted an electrical signal, which appears at the sensor output. Accelerometer x,y,z co-ordinates. those co-ordinates values are transmitted to the LPC-2148.

B. LPC2148

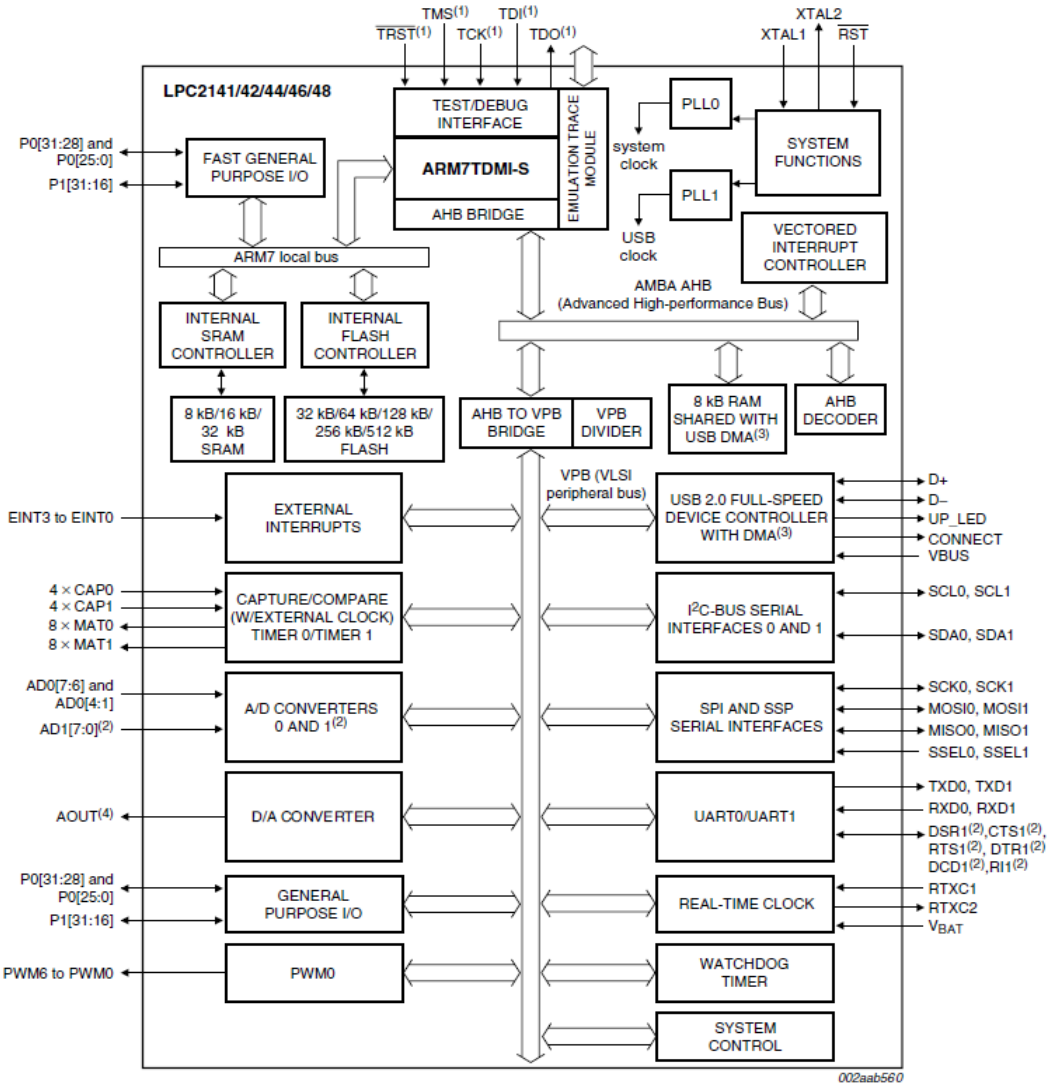
LPC stands for least pin count and these contain in built Arm-7Processor is there. ARM stands for Advanced RISC Machines. It is a 32 bit processor core, used for high end

application. It is widely used in Advanced Robotic Applications.

History and Development

ARM was developed at Acron Computers ltd of Cambridge, England between 1983 and 1985.RISC concept was introduced in 1980 at Stanford and Berkley.ARM ltd was found in 1990.ARM cores are licensed to partners so as to develop and fabricate new microcontrollers around same processor cores.

3. Architecture



(1) Pins shared with GPIO.
(2) LPC2144/46/48 only.
(3) USB DMA controller with 8 kB of RAM accessible as general purpose RAM and/or DMA is available in LPC2146/48 only.
(4) LPC2142/44/46/48 only.

Figure 2: LPC-2148 Architecture

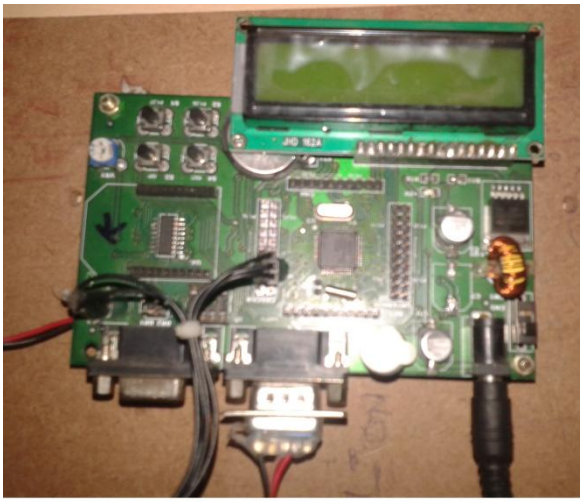


Figure 3: LPC-2148

C. Zigbee:

Zigbee is a transreceiver module which provides easy to use RF communication at 2.4 GHz. It can be used to transmit and receive data at 9600 baud rates from any standard CMOS/TTLsource. This module is a direct line in replacement for your serial communication it requires no extra hardware and no extra coding toIt works in Half Duplex mode i.e. it provides communication in both directions, but only one direction at same time.

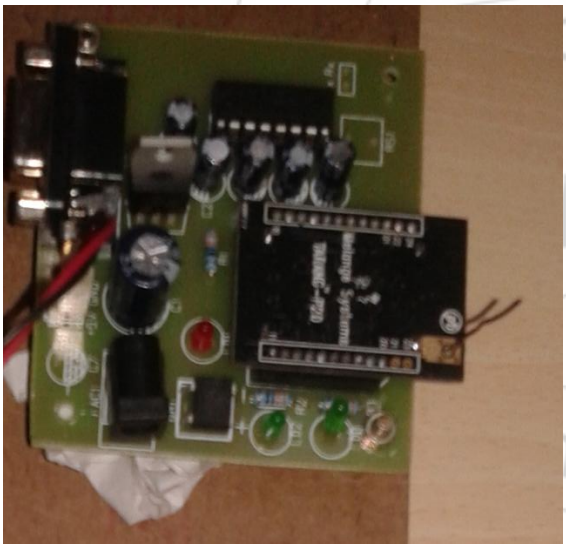


Figure 4: Zigbee

One of the intended applications of ZigBee is in-home patient monitoring. Patient's vital body parameters, for example blood pressure and heart rate can be measured by wearable devices. The patient wears a ZigBee device that interfaces with a sensor that gathers health related information such as blood pressure on a periodic basis. Then the data is wirelessly transmitted to a local server, such as a personal computer inside the patient's home, where initial analysis is performed. Finally the vital information is sent to the patient's nurse or physician via the internet for further analysis.

4. Receiver

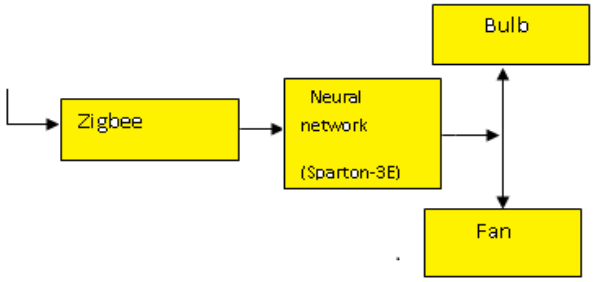


Figure 5: Receiver

Neural network

Here Kohonen's neural networks are used. Kohonen's networks are one of basic types of self-organizing neural networks. The ability to self-organize provides new possibilities - adaptation to formerly unknown input data. It seems to be the most natural way of learning, which is used in our brains, where no patterns are defined. Those patterns take shape during the learning process, which is combined with normal work. Kohonen's networks are a synonym of whole group of nets which make use of self-organizing, competitive type learning method. We set up signals on net's inputs and then choose winning neuron, the one which corresponds with input vector in the best way. Precise scheme of rivalry and later modifications of synapthic wages may have various forms. There are many sub-types based on rivalry, which differ themselves by precise self-organizing algorithm.

Architecture of self –organizing maps

Structure of neural network is a very crucial matter. Single neuron is a simple mechanism and it's not able to do much by itself. Only a compound of neurons makes complicated operations possible. Because of our little knowledge about actual rules of human's brain functioning many different architectures were created, which try to imitate the structure and behavior of human's nervous system. Most often one-way, one-layer type of network architecture is used. It is determined by the fact that all neurons must participate in the rivalry with the same rights. Because of that each of them must have as many inputs as the whole system.

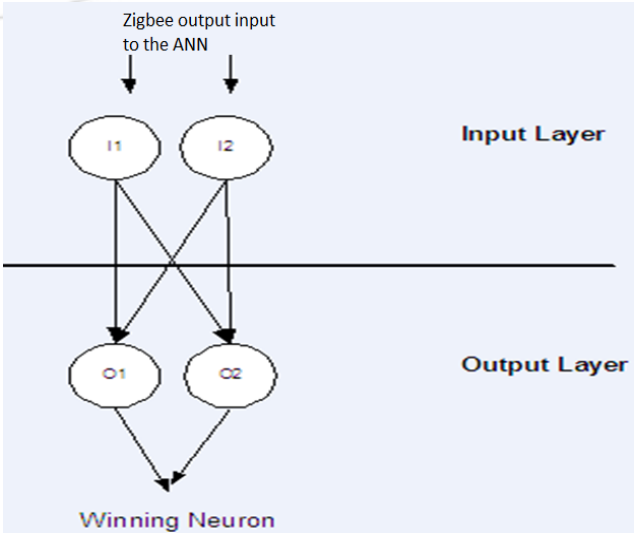


Figure 6: Neural network

Algorithm of Learning

The name of the whole class of networks came from the designation of algorithm called self-organizing Kohonen's maps. They had been described ine the publication "Self Organizing Map". Kohonen proposed two kinds of proximity: rectangular and gauss. The first is: and the second lambda" is the radius of proximity, it decreases in time.

$$G(i,x) = \begin{cases} 1 & dla \quad d(i,w) \le \lambda \\ 0 & dla \quad d(i,w) > \lambda \end{cases}$$

$$G(i,x) = \exp\left(-\frac{d^2(i,w)}{2\lambda^2}\right)$$

Use of Kohonen's method gives us better results than "Winner Takes All" method. Organization of the net is better (neurons organization represents the distribution of input data in a better way) and the convergence of the algorithm is higher. Because of that the time of single iteration is a few times longer - wages of many neurons, not only winners', have to be modified.

Here the kohonens neural network code written in VHDL and trend the neural network and that will be born to the Spartan - 3E board.

Accelerometer consists of x y z if move accelerometer x y z co-ordinates are varying that values are send to the LPC2148 and that will be transmitted to the zigbee .zigbee also transmitted to the receiver side wirelessly. The receiver wil received the data ever send transmitter that signals are send to the sparton board that will be decide the operation that means weather fan or bulb on.

5. Transmitter Flow Chart

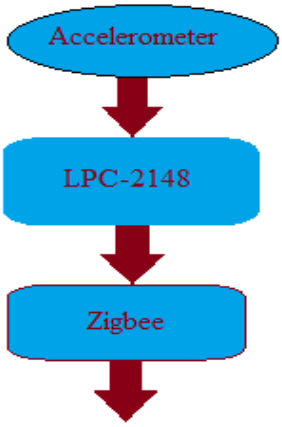


Figure7: Transmitter flow chart

6. Receiver Flow Chart

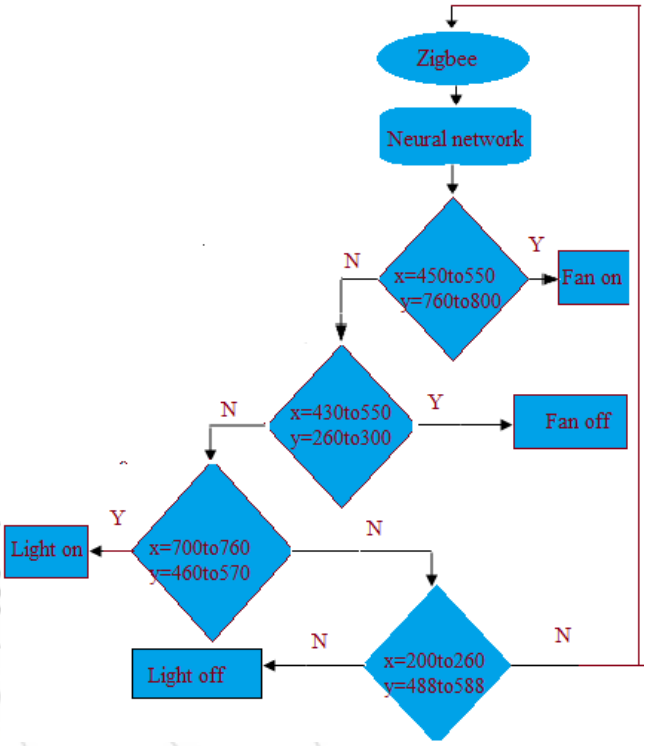


Figure 8: Receiver flow chart

7. Simulation and Synthesis Results

The hardware based implementation of carried out on single Spartan-3E family of fpga. The software development tool used for developing and verifying the design is the Xilinx ISE 10.1 version. Figure-11 to Figure-13 shows MODELSIM simulation results for light and fan ON and OFF.

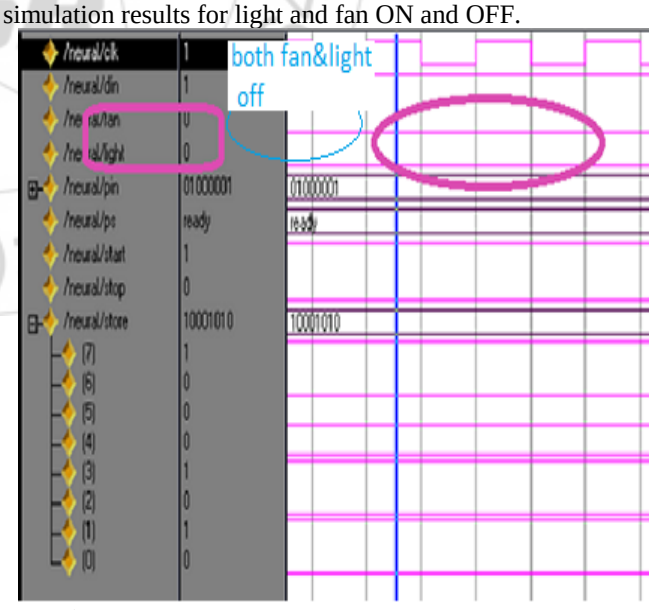


Figure 9: when din zero and out puts light and fan off

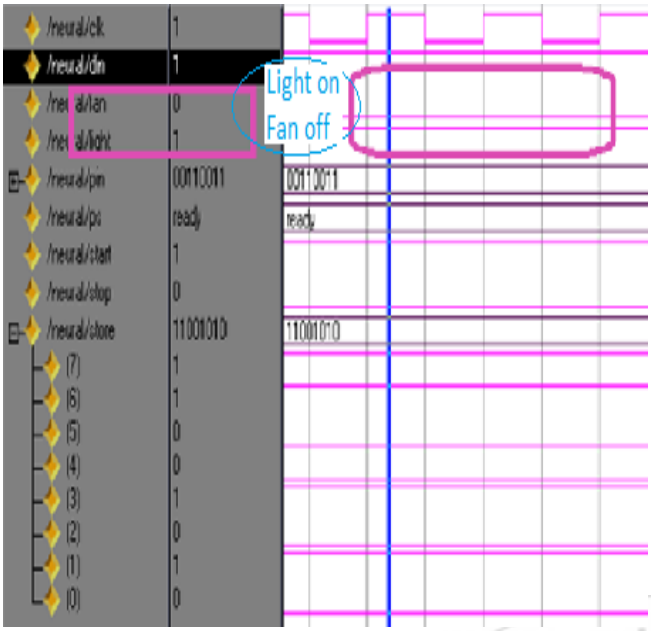


Figure 10: When din one and pin10000000. out puts light ON and fan OFF

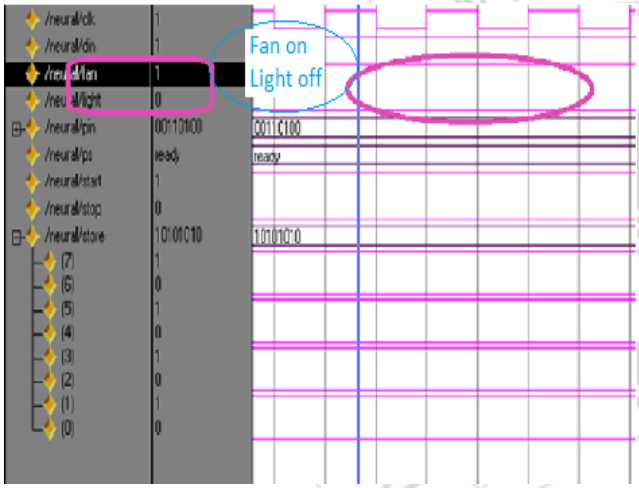


Figure 11: When din one and pin01000000. out puts light OFF and fan ON

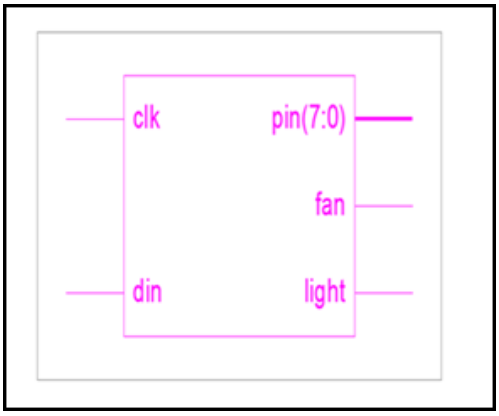


Figure 12: Technology schematic

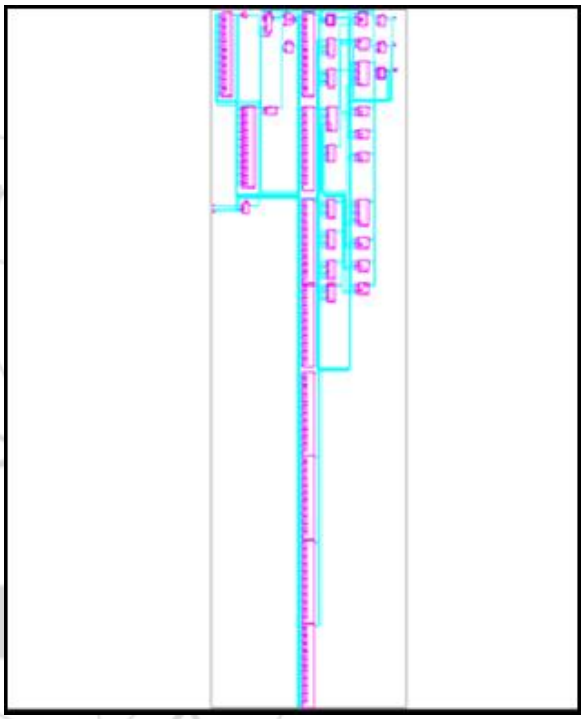


Figure 13: RTL Schematic

RTL Schematics

The Net List is RTL level of the Gesture recognition system, which is synthesizable and can be extracted on the Xilinx tool. By which we can get preface look of the system and a transition from the frontend of the VLSI designing to backend of the VLSI designing. Which means the same can run on FPGA kit and test its robustness and errors of the system can be debugged before it is taken to SOC Level and to Fab-Labs.

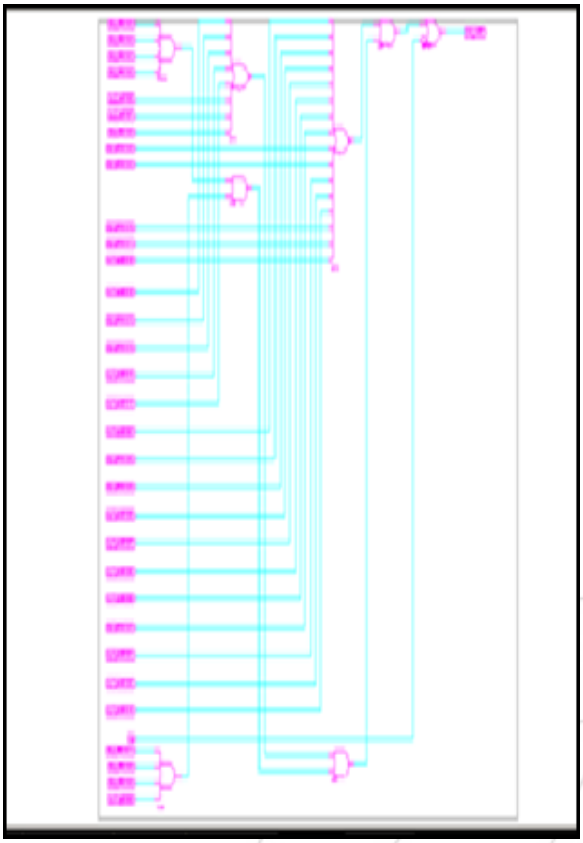


Figure 14: RTL schematic

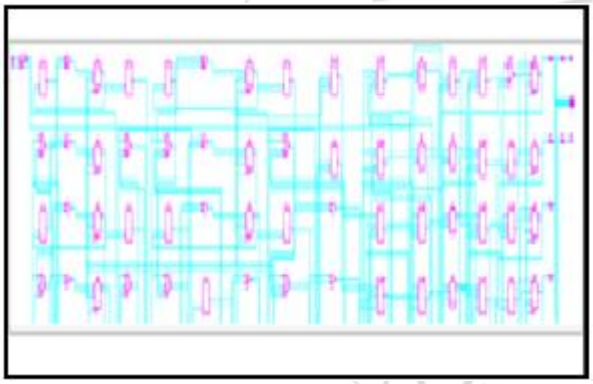


Figure 15: CLOCK distribution

Floor Planning Area

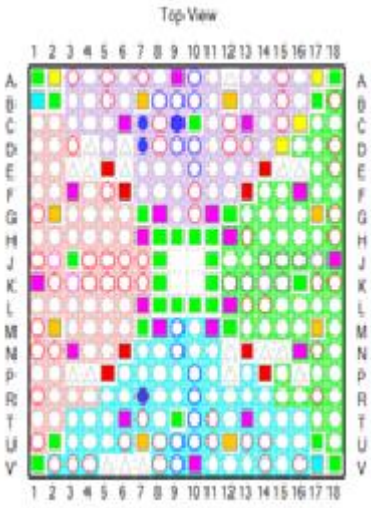


Figure 16: Xilinx floor planning area

8. Conclusions

We developed a new FPGA implementation of gesture recognition system in xilinx10.1If the system is more complex system we can also include number of of gestures. that means we can interface number of devices .here we can only interfacing light and fan.here the system implemented by a five basic gestures used . Left, right, front, back and idle.if you want more gestures the system will received more signals and also controlled by a more output devices.

References

[1] S. Oniga, A. Tisan, D. Mic, A. Buchman, A. Vida-Ratiu, Hand "Posturesrecognition system using artificial neural networks implemented inFPGA," 30th International Spring Seminar on Electronics Technology,ISSE 2007, Cluj-Napoca, ROMANIA, May 9-13, 2007, pp: 507 – 512.

[2] Stergiopoulou, N.Papamarkos "Hand gesture recognition using aneural network shape fitting technique" Elseiver Journal EngineeringApplications of Artificial Intelligence vol. 22, pp.1149 -1158, 2009.

[3] L. Marchese, "Digital neural network based smart devices", Projectproposal, FP7 European Research Program, http://www.synaptics.org,December 2006, unpublished.

[4] S. Oniga, A. Tisan, D. Mic, C. Lung, I. Orha, A. Buchman, A. Vida-Ratiu, "FPGA implementation of Feed-Forward neural networks for smart devices development", Proceedings of the ISSCS 2009International Symposium oSignals,Circuits and Systems, July 9-10,2009, Iasi, Romania, pp. 401-404.

[5] A. Tisan, S. Oniga, A. Buchman, C. Gavrincea, "Architecture and algorithms for synthesizable neural networks with on-chip learning", International Symposium on Signals, Circuits and Systems, ISSCS 2007,July 12-13, 2007, Iasi, Romania, vol.1, pp 265 – 268.

[6] J. Torresen, Sh.Tomita, „A review of implementation of back propagation neural networks", Chapter 2 in the book by N.Sundararajan and P. Saratchandran (editors): Parallel Architectures for Artificial Neural Networks, IEEE CS Press, 1998. ISBN 0-8186-8399-6.

[7] J. Zhu, P. Sutton, „FPGA implementations of neural networks – a survey of a decade of progress", 13th International Conference on Field Programmable Logic and Applications (FPL 2003), Lisbon, Sep 2003, Lecture Notes in Computer Science, 2003, Volume 2778/2003, 1062-1066, DOI: 10.1007/978-3-540-45234-8_120.

[8] S. Oniga, A. Tisan, D. Mic, A. Buchman, A. Vida-Ratiu, "Optimizing FPGA implementation of feed-forward neural networks",, Proceedings of the 11th International Conference on Optimization of Electrical and Electronic Equipment OPTIM 2008, 2008, Brasov, Romania, May 22-23, pp. 31-36.

[9] Yun Liu, Zhijie Gan and Yu Sun" Static Hand Gesture Recognition and Its Application based on Support Vector Machines" Ninth ACIS International Conference on Software Engineering, Artificial Intelligence, Networking and Parallell Distributed Computing pp 517-521, 2008.

Author Profile

N. Naveenkumar received B.Tech Degree in Electronics and communication engineering from MLR Institute of Engineering and Technology in the year 2012. He is currently M.Tech student in VLSI SYSTEM DESIGN in VNR Vignan Jyothi Institute of Engineering & Technology, Bachupally, Hyderabad and, India. And his research interested areas are in the field of Communication systems and VLSI Design.

Dr. V. Padmaja born in 1968. She received B.E Degree in Electronics and Communications Engineering, M.E Degree in Digital Systems Engineering from O.U in 1991 and 1999 respectively. She received PhD from J.N.T.U in 2009. She is a Professor in Dept. of ECE in VNRVJIET, her research of interest Includes Pattern classification, image processing and Embedded Systems. She has authored more than 17 Research papers in National and International Conferences and Journals.

Naga Deepa. CH received B. Tech Degree in Electronics & Communications and M. Tech degree in Embedded Systems from the Jawaharlal Nehru Technological University of Hyderabad, India, where she is currently pursuing the Ph.D. degree. Presently she is working as assistant professor in the Department of ECE, in VNRVJIET. Her main research interests include signal processing and pattern recognition techniques applied to electronic mobile devices. She is a life Member of ISTE and IETE.