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Fault Tolerant Linear State Machine Design Approach for Safety Critical Systems Implemented on FPGA

Sunanda[1], Fathima Rehana[2]

[1]VTU University, P.A.College of Engineering Nadupadav Manglore India

[2]Profesor, VTU University, P.A.College of Engineering Nadupadav Manglore India

Abstract: ***In this paper, a new method for the design of fault tolerant linear state machines with initial state 0 and one dimensional input and one-dimensional output is proposed. It is shown that the LFSR-implementation of the transfer function of a linear automaton can be utilized to correct transient errors in the memory elements. Since the state vector of a linear automaton is uniquely determined by the last n inputs and outputs, a transient error in a memory element can be corrected within n clock cycles by use of the corrected output symbols, where n is the number of components of the state vector.***

Keywords: TMR(tripple modular redundancy), Voter logic.

1. Introduction

New method for the design of fault tolerant linear state machines with initial state 0 and one dimensional input and one-dimensional output is proposed. It is shown that the LFSR-implementation of the transfer function of a linear automaton can be utilized to correct transient errors in the memory elements. Since the state vector of a linear automaton is uniquely determined by the last n inputs and outputs, a transient error in a memory element can be corrected within n clock cycles by use of the corrected output symbols, where n is the number of components of the state vector.

Linear state machines are of importance in different fields of application such as encoding and decoding of cyclic codes, especially BCH codes generation of pseudorandom test patterns and test response compaction by multiple input signature analyzers, the implementation of stream ciphers and others. In modern technologies the number of errors in memory elements caused by transient faults is increasing and for many applications fault-tolerant designs are now of growing interest. The standard approach for fault tolerance is triple modular redundancy (TMR).

A system is triplicated into three (functionally) identical systems and the outputs of the triplicated Systems are connected to a three-input voter which determines the output of the fault-tolerant system as the majority of the outputs of the triplicated systems.

The main advantages of TMR are that errors due to an arbitrary fault in only one of the triplicated systems are tolerated, and that no specific error model is required

2. Objectives

1. Study the state machine theory.
2. Study the fault-tolerant application in VLSI systems.
3. Develop a RTL fault-tolerant state-machine model and verify it using a RTL test bench.
4. Develop an application for fault-tolerant state machine and implement it on FPGA to observe the performance

3. Methodology

- Further literature survey has to carried out to extract more ideas
- A design plan should be created with an application
- RTL Design of the proposed design should made
- RTL verification should be done to make sure the design is working as decided
- First level FPGA implementation should be done. This will complete one full cycle.
- Next, speed, area, power and other parameters should be observed and tabulated.
- Fault tolerant logic should incorporated into the design and complete the above related steps once again.
- Comparison of the parameters should be done between regular and fault-tolerant models
- A demonstration should be setup to prove how fault tolerant system is helpful. This can be done using the application decided
- Thesis/dissertation should be written.

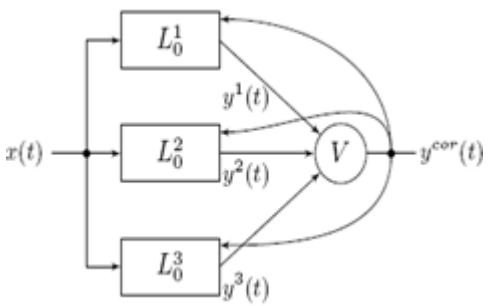

Figure 1: Triplication with State Correction through voting

4. Experimental Results

Since in all proposed designs single transient errors in the state components and in the combinational circuit parts are corrected (at least after *n* clock cycles), they are compared with known solutions, which also correct state errors and errors in the combinational parts of the circuit.Linear state machines of different dimensions (from 8 to 256 bits) were chosen and the area overhead of the proposed designs was determined.

- Triplication of the memory elements and voting of the triplicated memory elements by a single voter for all three memory elements.
- Triplication of the memory elements and voting of the triplicated memory elements by three voters for all three memory elements. Here, the corresponding combinational elements are also triplicated.
- The state of the linear state machine is encoded by a Hamming-code.

5. Conclusion

In this paper, a new method for the design of fault-tolerant linear state machines with initial state 0 and one-dimensional input and one-dimensional output was proposed.It was shown that the LFSR-implementation of the transfer function of a linear automaton can be utilized to correct transient errors in the memory elements. Since the state vector of a linear automaton is uniquely determined by the last n inputs and outputs, a transient error in a memory element can be corrected within n clock cycles by use of the corrected output symbols, where n is the number of components of the state vector. Experimental results have shown that the lowest area overhead can be obtained if the linear state machine is duplicated and a single parity bit is used to distinguish which of the duplicated machines is correct. In this case, an area overhead of 177 % for an 8-bit state vector and 160 % for a 256-bit state vector is achived.

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