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Review on Floating Point Multiplier Using Vedic Mathematics

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Abstract: ***The fundamental and the core of all the Digital Signal Processors (DSPs) are its multipliers and the speed of the DSPs is mainly determined by the speed of its multiplier. IEEE floating point format is a standard format used in all processing elements since Binary floating point numbers multiplication is one of the basic functions used in digital signal processing (DSP) application. In this work VHDL implementation of Floating Point Multiplier using ancient Vedic mathematics is presented. The idea for designing the multiplier unit is adopted from ancient Indian mathematics "Vedas". The Urdhva Tiryakbhyam sutra (method) was selected for implementation since it is applicable to all cases of multiplication. Multiplication using Urdhva Tiryakbhyam sutra is performed by vertically and crosswise, vertically means straight above multiplication and crosswise means diagonal multiplication and taking their sum. The feature of this method is any multi-bit multiplication can be reduced down to single bit multiplication and addition. On account of these formulas, the partial products and sums are generated in one step which reduces the carry propagation from LSB to MSB.***

Keywords: Urdhva-Tiryakbhyam sutra, VHDL.

1. Introduction

Multipliers are key components of many high performance systems such as microprocessors, DSP processors, various FIR filters, etc. A performance of a system is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Since multiplication dominates the execution time of most DSP application so there is need of high speed multiplier. Hence increasing the speed and optimizing area of the multiplier is a major design issue. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel Multipliers at one end of the spectrum and fully serial multipliers at the other end. These multipliers have moderate performance in both area and speed. In DSP

The formats are composed of 3 units; Sign unit, Exponent unit and Mantissa unit. Multiplication is an important fundamental arithmetic operation. A change in design implementation level by the insertion of a new technology can often make viable an existing marginal algorithm or architecture.

This work deals with the “Design of high speed multiple precision floating point multiplier using “Vedic algorithm”. In this project, Vedic Multiplication Technique is used to implement IEEE 754 Floating point multiplier with efficient use of carry save adder. The Vedic sutra is used for the multiplication of Mantissa. Performance constraints can also be addressed by applying alternative technologies as application binary floating point numbers multiplication is is one of the basic functions. The IEEE 754 standard provides for many closely related formats. The Single precision consist of 32 bits, Double precision consist of 64 bits and double extended precision of 80 bits.

Table 1: Ieee Format

Format	Sign	Exponent	Mantissa
Single Precision	1(31)	8 (23 TO 30)	23(0 TO 22)
Double Precision	1(64)	11(52 TO63)	52(0 TO 51)

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2. Floating Point Multiplication Algorithm

The double precision format helps overcome the problems of single precision floating point.The floating point numbers represented in IEEE 754 format can be divided in four different units

Mantissa Calculation Unit, Exponent Calculation Unit
Sign Calculation Unit, Normaliser Unit.

As stated in the introduction, normalized floating point numbers have the form of Z= (-1S) * 2 (E - *Bias*) * (1.M). The below fig flowchart shows how multiply of two floating point numbers is done.

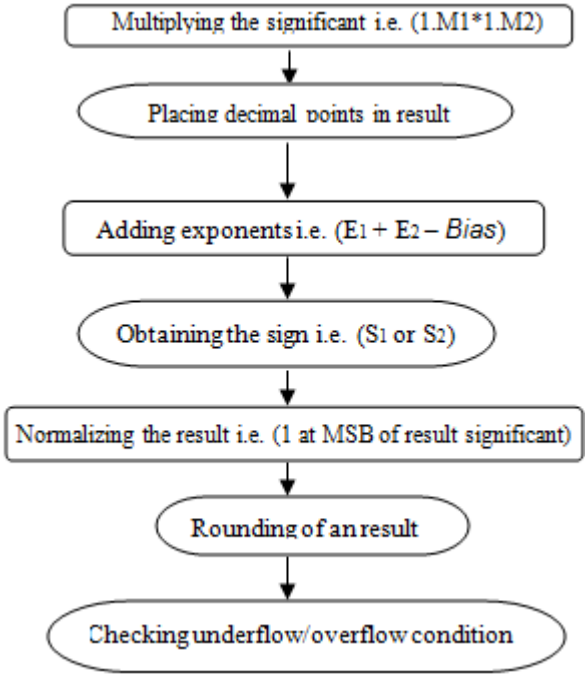

Figure 1: Steps of multiplying Floating Point numbers

3. Multiplier Design

3.1 Vedic mathematics

The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge .

3.2 Urdhva-tiryakbyham sutra

Urdhva-Tiryakbhyam Sutra is a multiplication algorithms which is applicable to all cases of multiplication.Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. In this method the partial products are generated simultaneously which itself reduces delay and makes this method fast.

1) (Anurupye) Shunyamanyat - If one is in ratio. The other is zero
2) Chalana-Kalanabyham- Differences and Similarities.
3) Ekadhikina Purvena - By one more than the previous one
4) Ekanyunena Purvena - By one less than the previous one
5) Gunakasamuchyah - The factors of the sum is equal to the sum of the factors
6) Gunitasamuchyah - The product of the sum is equal to the sum of the product
7) Nikhilam Navatashcaramam Dashatah - All from 9 and the last from 10
8) Paraavartya Yojayet - Transpose and adjust.
9) Puranapuranabyham - By the completion or noncompletion
10) Sankalana-vyavakalanabhyam - By addition and by subtraction
11) Shesanyankena Charamena - The remainders by the last digit
12) Shunyam Saamyasamuccaye - When the sum is the same that sum is zero
13) Sopaantyadvayamantyam - The ultimate and twice the penultimate
14) Urdhva-tiryakbyham - Vertically and crosswise

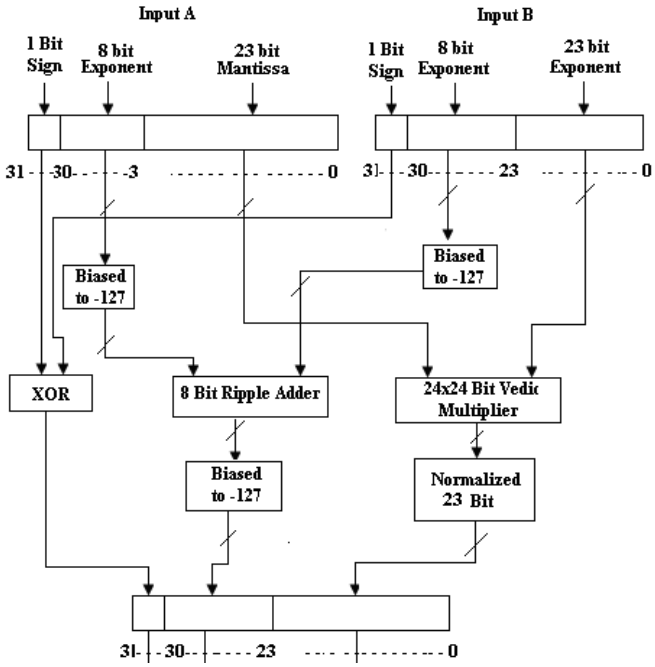

Figure 2: Block diagram of Floating Point multiplier

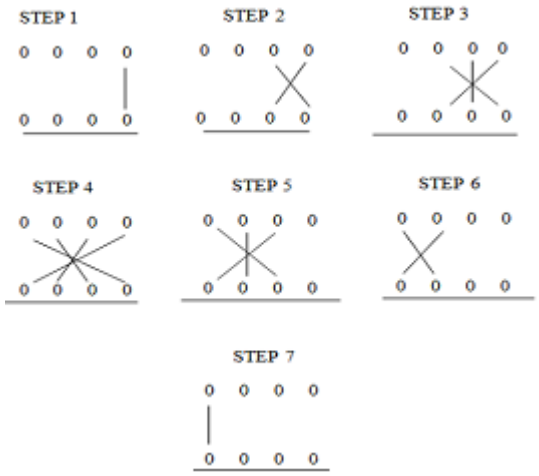

Figure 3: Line diagram of the multiplication

4. Mantissa Calculation Unit

The performance of Mantissa calculation Unit dominates overall performance of the Floating Point Multiplier. The Vedic Multiplication technique is chosen for the implementation of this unit. This technique gives result in terms of speed and power and for single precision multiplier 3*3 bit multiplier designed as a basic multiplier.

5. Literature Review

According to N. Ravi Array multiplier is used for designing of multiplier but In array multipliers partial products are calculated independently in parallel. The delay associated with the array multiplier is the time taken by the signals to propagate through the gates that form the multiplication array.Booth multiplier. According to Dr. Ravi Shankar Mishra The Arithmetic and logical unit play an important role in digital systems. Particular, Multiplication is especially

relevant instead of other arithmetic operators, such as division or exponentiation, which one is also utilized by multiplier as building blocks.Multipliers are key components of many high performance systems such as FIR filters,microprocessors, digital signal processors, etc . Asystem's performance is generally determined by the performance of the multiplier because the multiplieris generally the slowest element in the system. For faster computation, this paper compared Robertson's and Booth's algorithm in which quick and accurate performance of multiplier operation has been done.but Booth multiplication is another important multiplication algorithm. Large Booth arrays having large partial sum and partial carry registers are required for high speed multiplication and exponential operations. In this algorithm a large propagation delay associated. According to Mohamed Al-Ashrafy for designing of floating point multiplier is efficient using Carry save multiplier. This paper presents an implementation of a floating point multiplier that supports the IEEE 754-2008 binary interchange format; the multiplier doesn't implement rounding and just presents the significant multiplication result as is (48 bits); this gives better precision if the whole 48 bits are utilized in another unit; i.e. a floating point adder to form a MAC unit. The design has three pipelining stages and after implementation on a Xilinx Virtex5 FPGA.

In order to enhance the performance of the multiplier, pipelining stages are used to divide the critical path thus increasing the maximum operating frequency of the multiplier. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed by using new techniques can greatly improve system performance.
According to Honey DurgaTiwari a Vedic multiplier and square architecture is proposed based on algorithm of ancient Indian Vedic Mathematics, for low power and high speed applications. This Paper shows how the computational complexity is reduced in the case of Vedic multipliers as compared to the conventional multipliers.

The Vedic multiplication formulae, Urdhvatiryakbhyam and Nikhilam, have been investigated in detail. Due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra which reduces the multiplication of two large numbers to the multiplication of two small numbers.
The FPGA implementation result shows that the delay and the area required in proposed design is far less than the conventional booth and array multiplier designs making them efficient for the use in various DSP applications.

According to AnveshKumar discussion about the Fast Fourier Transform (FFT) and its application such as imaging, software-defined radio, wireless communication, instrumentation and machine inspection is done in this paper. In this paper reconfigurable FFT is proposed to design by Vedic mathematics.

Based on the number of multipliers and number of adders required in a normal method and a Vedic method, a comparison chart is made and it is found out that the Vedic mathematics are going to reduce the number of adder and multiplier as compared to the conventional method.

According to M.Nagaraju [3] Complex multiplication is very useful and advantageous in Digital Signal Processing (DSP) and Image Processing (IP). In order to implement the hardware of its module of Discrete Fourier Transformation (DFT), Discrete Cosine Transformation (DCT), Discrete Sine Transformation (DST) and modem broadband communications; large numbers of complex multipliers are required. Complex number multiplication can be performed by the aid of four real number multiplications and two additions or subtractions. In real number processing, carry needs to be propagated from the least significant bit (LSB) to the most significant bit (MSB) when binary partial products are added. Therefore, the addition and subtraction after binary multiplications limit the overall speed. Many alternative method had so far been proposed for complex number multiplication.

RTL View and Output Simulationof 3 Bit Multiplier

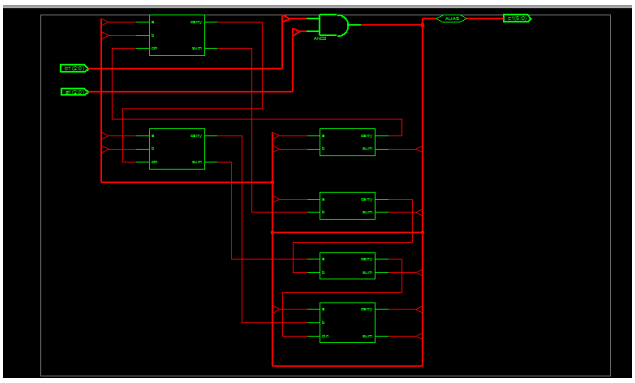

Figure 4: Rtl schematic for 3 bit multiplier

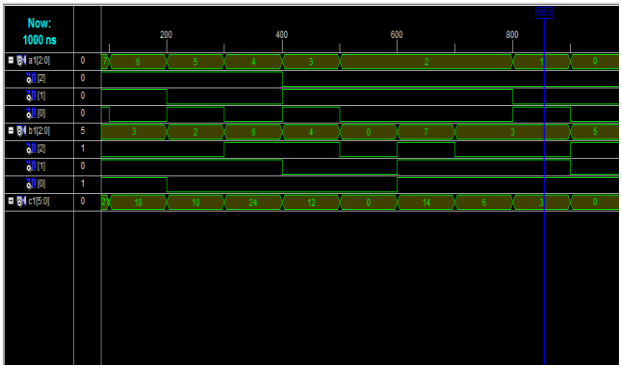

Figure 5: output simulation for 3 bit multiplier

6. Conclusion

The paper shows the efficient use of Vedic multiplication method in order to multiply two floating point numbers This paper presents an implementation of a floating point multiplier that supports the IEEE 754-2008 binary interchange format. Based on the discussion made above it is very clear that a multiplier is a very important element in any processor design and a processor spends considerable amount of time in performing multiplication and generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. An

improvement in multiplication speed by using new techniques can greatly improve system performance. So the aim of our project is Analyzing the problem, studying various ways to overcome the problems and try to improve system performance. This project can be extended for the reconfigurable architecture.

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