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# Functional Broadside Test Generation for Fault Analysis

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**Abstract**: ***When the clock frequency of the integrated circuits increases, timing related defects may occur and it is necessary to find them. The timing defects are modeled by delay faults. Transition faults are used as the delay fault model. The effect of a transition fault at a point in a circuit is that, the transition that occur at that point will not reach the flip flop or a primary output within the desired clock period of the circuit. Existing methods for testing includes Enhanced scan, Skewed load and Broadside tests. They may cause over testing. The Functional broadside test, which is a two pattern test, avoids this over testing by using only reachable states. It is a broadside test that creates in its functional clock cycles, the same state transitions that may occur during functional operation. Earlier procedures generate test sets offline for application from an external tester. Here, the circuit is used to obtain reachable states during test. Pairs of consecutive time units of the primary input sequences can be used to produce two pattern tests. They are called functional, since they use reachable states which are also possible during the functional operation.***

**Keywords:** Functional broadside tests, LFSR, Reachable states, Transition fault, Two pattern test

## 1. Introduction

With the increase in the clock frequency of the integrated circuits, defects affecting the timing behavior of the circuit may occur and detection of these defects is necessary. The purpose of delay testing is to detect these defects. A test detects a defect, when the time it takes a desired transition to propagate to an observation point exceeds the clock period allowed for that transition.

There are two fault models for delay defects [7]. They are transition fault and path delay fault. A test which delivers a rising (falling) transition to a node and sensitizes a path from that node to an observation point will detect a slow-to-rise (slow-to-fall) transition fault at that node. That same test may also detect a path delay fault associated with the particular route into and out of the node in question, though the values of the off-path inputs may invalidate the test. Transition faults are widely used as the delay fault model.

Over testing for delay faults can be viewed in two ways. Under the first view, over testing is due to the fact that redundant faults in the original circuit before scan insertion become detectable after scan insertion. Detection of these redundant faults may lead to good chips discarded as faulty. Under the second view, it is caused by non functional operation conditions during test. A synchronous sequential circuit may enter functionally unreachable states during test.

This can increase switching activity which may lead to supply voltage drops and, as a result, cause defect-free chips to fail delay testing.

Existing techniques such as Enhanced scan, Skewed load and Broadside tests may suffer from unnecessary yield loss due to over testing. Functional broadside tests are two pattern tests that avoid over testing by ensuring that the circuit traverses only reachable states during the functional clock cycles of a test. This test ensures that the initial state is a state that the circuit can enter during functional operation, or a reachable state. They operate the circuit in functional mode for two clock cycles after an initial state is given. This results in the application of a two pattern test. Since the initial state is a reachable state, the circuit goes through state transitions that are guaranteed to be possible during functional operation. Delay faults that are detected by the test can also affect functional operation. This alleviates the type of over testing seen in other methods.

## 2. Related Works

The Design-For-Testability (DFT) features of a given test methodology gives the method in which a delay test can be applied. The three popular implementations are Enhanced Scan, Skewed load and Broadside tests. Over testing due to the application of two-pattern scan-based tests was described in [6] and [7]. Over testing is related to the detection of faults that do not affect the normal operation of the circuit. There are many reasons for the non functional operation conditions. When an arbitrary state is used as the initial state, the test takes the circuit through state transitions not possible under normal operation. Hence, these nonsensical tests may cause the circuit to fail. Current demands that are higher than those possible during the functional operation may cause voltage drops. Hence, the circuit will fail. The Enhanced scan and Skewed load methods allow delay tests to be applied that are unrealizable in normal operation. The circuit operates correctly during functional operation even in the presence of these faults detected by them. These test application methodologies causes over testing.

Test generation procedures for pseudo-functional scan-based tests were described in [3] and [5]. The test sets were generated offline for application from an external tester. Pseudo-functional scan-based tests use functional constraints to avoid unreachable states that are captured by the constraints. An arbitrary state used as a scan-in state is unlikely to be a reachable state. These tests can cause over

testing. Also, they dissipate more power than possible during functional operation.

The problem of repeated synchronization is described in [4]. According to this, the sequence will force the same values on the state variables in S(c) repeatedly. The on-chip generation of Functional broadside tests is described in [2]. Here, all the primary input values are always modified together and to the same values. In addition, some primary inputs receive shifted values of the primary inputs immediately preceding them. Multiple primary input sequences are applied in order to achieve the highest possible fault coverage. To select which tests will be applied to the circuit based on every sequence, this approach uses a different gate for every sequence. Since the number of sequences is significant here, a large multiplexer and a significant number of gates are needed for this purpose. The length of the primary input sequences is varied in order to control the number of tests applied to the circuit. Thus, it has hardware overhead. The number of gates used is equal to the number of bits in cube plus the number of sequences.

## 3. Methodology

This section describes the method for generating Functional broadside tests. Section III-A describes the concept of Functional broadside tests. Section III-B describes the generation of the sequence A. Section III-C describes the selection of tests that will be applied based on A. Section III-D describes the circuit used and test generation method.

### 3.1 Functional Broadside Tests

Functional broadside tests are two-pattern tests that avoid over testing by ensuring that a circuit traverses only reachable states during the functional clock cycles of a test. A reachable state is a state that can be visited from all the circuit states or all unspecified state. The generation of Functional broadside tests requires the identification of reachable states. The discussion in this paper assumes that the circuit is initialized into a known state before functional operation starts. The initial state of the circuit is denoted by $s_r$. The discussion also assumes that functional operation consists of the application of primary input sequences starting from state $s_r$. The functional operation starts by initializing the circuit into a known state, the all-0 state. Therefore, the all-0 state is a reachable state. An unreachable state may be entered during a test, if an unreachable state is used as the initial state of the test. Thus, starting from a known reachable state, additional reachable states can be identified by considering the states that the circuit enters under the application of primary input sequences. This test applies two primary input vectors in functional mode after the initial state is given. A Functional broadside test is denoted by $< s_i a_i, s_j a_j >$, where $s_i$ is the initial state (reachable state), $a_i$ and $a_j$ are the primary input vectors, and $s_j$ is the state reached after $s_i$ and $a_i$ were applied. After $s_i$ is given, the circuit makes state transitions, from $s_i$ to $s_j$ under $a_i$ , and from $s_j$ under $a_j$. With a reachable state $s_i$, these state transitions can also occur during functional operation. As a result, the switching activity during the test can also occur during functional operation.

### 3.2 Primary input sequence generation

The primary input sequence A can be generated by using a Linear Feedback Shift Register (LFSR). But there exists a problem called repeated synchronization. In this, a random sequence takes the circuit into the same or similar reachable states repeatedly. Thus, subsets of state variables are forced to the same values. The sequence from the LFSR is modified using gates to overcome this problem.

An input cube c synchronizes a subset of state variables S(c), if applying c to the primary inputs in the all-unspecified state, results in the specification of the state variables in S(c) one time unit later. If c has a small number of specified inputs, the input vectors covered by it may appear often in the random primary input sequence. Thus, the sequence will force the same values on the subset of state variables repeatedly and may limit the fault coverage that the sequence can obtain. The input cube is selected such that the circuit can reach all its reachable states.

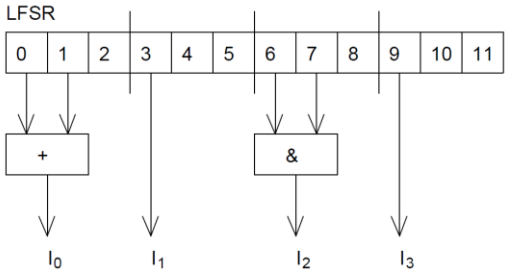


**Figure 1**: Generation of Primary input sequence

If there are n primary inputs in a circuit, a (d.n)-bit LFSR can be used. Here, the parameter d refers to the number of LFSR bits per primary input. The s27 circuit has four primary inputs (n = 4). Also, three bits of LFSR is used for each primary input to avoid repeated synchronization. Thus a 12-bit LFSR is used here. The following rules are used for modifying the sequence from LFSR. Let c(j) be the cube and mod be the number of LFSR bits for modifying a primary input.

- If c(j) = X, the value of $I_j$ is the random value produced by the LFSR.
- If c(j) = 0, the and function of mod LFSR bits gives the value of $I_j$.
- If c(j) = 1, the or function of mod LFSR bits gives the value of $I_j$.

Thus each primary input is modified using different LFSR bits thereby reducing the dependencies between them. The parameters used are d = 3, mod = 2 and c = 1X0X. The bits 0, 1 and 2 of the LFSR are used to produce $I_0$ (d = 3). Two LFSR bits are used for modifying the primary input. Since c(0) = 1, an OR gate driven by bits 0 and 1 of the LFSR is used. The bit 2 of the LFSR reduces the dependencies between the values of $I_0$ and $I_1$. For $I_1$, the third, fourth and fifth bits of LFSR are used. Here c(1) = X, $I_1$ is therefore driven directly by bit 3 of the LFSR. Bits 4 and 5 reduce the

dependencies between $I_1$ and $I_2$. For $I_2$, c(2) = 0, an AND gate driven by bits 6 and 7 of the LFSR is used. The bit 8 of the LFSR reduces the dependencies between $I_2$ and $I_3$. Similarly, $I_3$ is driven directly by bit 9 of the LFSR. This requires a 12-bit LFSR and gates as shown in Figure 1. Here the seed used is 101 011 100 100.

### 3.3 Test Selection

Functional broadside tests are two pattern tests. Every sub-sequence of length two of primary input sequence A defines a Functional broadside test, t(u) = <s(u), a(u), a(u+1)>. Here, a(u) and a(u+1) are primary input vectors that are applied in two consecutive functional clock cycles starting from A. The selection of tests that will be applied based on A is done considering the following conditions.

- The tests should be non overlapping.
- It should be possible to produce the subset of time units U efficiently.
- The test set based on U should detect as many faults as possible.
- U should be as small as possible.

The tests starting in two consecutive time units are overlapping in the following sense. Application of t(u) takes the circuit through states s(u), s(u+1) and s(u+2). Application of t(u+1)takes the circuit through states s(u+1), s(u+2) and s(u+3). The application of both t(u) and t(u+1) requires special hardware to bring the circuit back to state s(u+1) after t(u) is applied. A counter denoted by CNT can be used to select the tests. The tests that start at time units divisible by four are applied. The last two bits of the CNT are given to a NOR gate to get the function apply as shown in Figure 2. When apply=1, t(u) is applied as a two pattern test to the circuit.

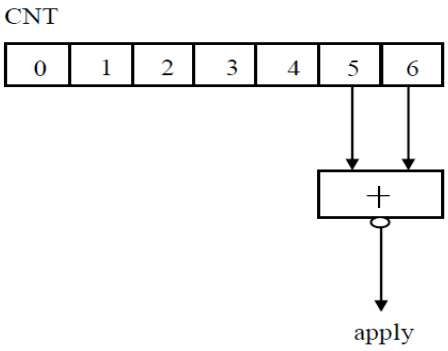


**Figure 2**: Selection of tests

### 3.4 Testing

The circuit used is ISCAS-89 benchmark s27 with initial state $s_r$ = 000. It has four inputs and three state variables as shown in Figure 3. The primary input sequence can be used as the source for primary input vector of the Functional broadside test, t(u) = <s(u), a(u), a(u+1)>. The circuit is first placed in the initial state $s_r$ and primary input sequence A is applied. Then, several of the Functional broadside tests that can be extracted from A is used in order to detect the faults. With $s_r$ as the initial state for functional operation, $s_r$ is a reachable state. In addition, the set of reachable states consists of every state $s_i$ such that there exists a primary input sequence A that takes the circuit from $s_r$ to $s_i$ . Since $s_i$ can be entered during functional operation starting from $s_r$, $s_i$ is a reachable state. Let s(u) be the state that the circuit reaches at time unit u under A. Also s(0) = $s_r$. In addition, s(u) is a reachable state. Hence every state s(u) can be used as the initial state for a Functional broadside test, t(u) = <s(u), a(u), a(u+1)>.

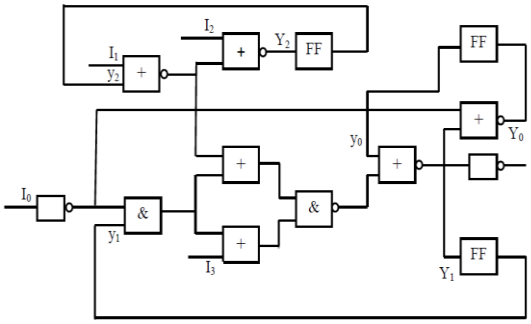


**Figure 3**: s27 circuit

At time unit u, the circuit is in state s(u). Applying a(u) and a(u+1) in functional mode will result in the application of t(u). A fault is detected by comparing the faulty state and the expected fault-free state.

## 4. Results and Discussion

The design entry is modeled using VHDL in Xilinx ISE Design Suite 12.1. The simulation of the design is performed using ISim from Xilinx ISE to verify the functionality of the design. The RTL schematic view is shown in Figure 4.

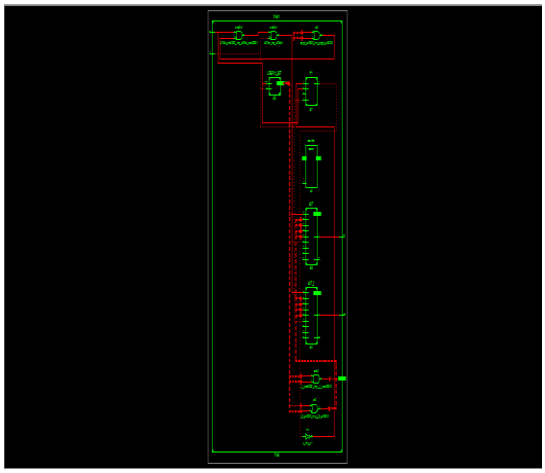

**Figure 4**: RTL Schematic

Table 1 shows the output of primary input sequence generation. Table 2 shows the state of the circuit and the primary input vector.

**Table 1**: Primary Input Sequence

| u | lfsr(u) | i(u) |
|---|---|---|
| 0 | 101011100100 | 1001 |
| 1 | 010101110010 | 1110 |
| 2 | 001010111001 | 0010 |
| 3 | 100011001100 | 1001 |
| 4 | 010001100110 | 1001 |
| 5 | 001000110011 | 0010 |
| 6 | 100010001001 | 1000 |
| 7 | 110111010100 | 1101 |
| 8 | 011011101010 | 1000 |
| 9 | 001101110101 | 0111 |

**Table 2**: Primary input sequence for s27

| u | s(u) | i(u) |
|---|---|---|
| 0 | 000 | 1001 |
| 1 | 010 | 1110 |
| 2 | 100 | 0010 |
| 3 | 000 | 1001 |
| 4 | 010 | 1001 |
| 5 | 010 | 0010 |
| 6 | 010 | 1000 |
| 7 | 100 | 1101 |
| 8 | 101 | 1000 |
| 9 | 101 | 0111 |

The Functional broadside test generation consists of primary input sequence generation, test selection and test generation. Initially, the coding of the individual sections were completed and then they were combined using the structural modeling. The simulation result of the Functional broadside test generation is shown in Figure 5.

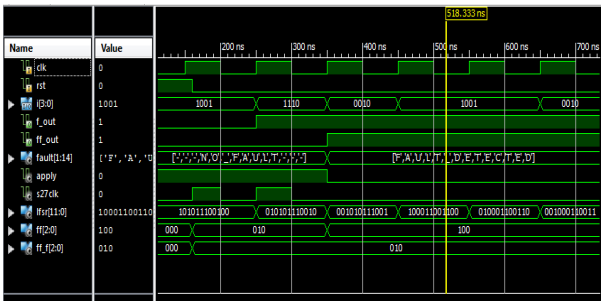


**Figure 5**: Test generation

## 5. Conclusion

The paper described the generation of Functional broadside tests using a simple and fixed hardware structure. This includes a primary input sequence generation, testing circuit and test generation. Random primary input sequences were modified to avoid repeated synchronization and thus yield varied sets of reachable states. A 12-bit LFSR with seed 101 011 100 100 and a small number of gates for modifying the sequence were used for primary input sequence generation. The functional broadside test, which is a two pattern test, was applied to the circuit in two functional clock cycles. A counter along with a NOR gate was used to select the time units at which test is to be applied. The ISCAS-89 benchmark s27 circuit was used. Over testing was avoided with the use of functional broadside tests. The work also focuses on reducing the power consumption by replacing the pattern generation technique.

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