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FPGA Based Architecture for Radar Information Analysis

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Abstract: ***Radar is an object-detection system that uses radio waves to determine the range, altitude, direction, or speed of objects. The radar transmitter transmits pulses of radio waves or microwaves that bounce off any object in their path and the object returns a tiny part of the wave's energy to the receiver. In the receiver it is processed to determine the presence of the target and location. Two main radar types are Continuous wave Doppler radar and Ultra wide band pulse Doppler radar. At the receiver part of Continuous Wave Doppler radar the incoming signal is initially converted to an intermediate frequency (IF) to filter out the unwanted low-frequency components, the filtered IF signal is then shifted to baseband using digital down converter (DDC)module. This paper emphasis on digital down conversion module at the receiver part. Digital down converter (DDC) consist of Direct Digital Synthesizer (DDS), parallel multipliers and a decimation filter. The Direct digital synthesizer produce sine and cosine waves whose magnitude is multiplied with a digital value from ADC in the parallel multiplier and the output from the multiplier is decimated to obtain the final Digital down converter output. The coding of digital down conversion module is done in VHDL and further it can be synthesized into FPGA. FPGA gives great flexibility, as compared to the conventional dedicated hardware components solution.***

Keywords: Continuous wave (CW), CIC filter, Digital Down Converter(DDC),Direct Digital Synthesizer(DDS),Field-Programmable Gate Array (FPGA)

1. Introduction

Radar is an object detection system that uses radio waves to determine the range, altitude, direction, or speed of objects. It can be used to detect aircraft, ships, spacecraft, motor vehicles and natural environment. It operates by radiating energy into space and detecting the echo signal reflected from objects, or target. The reflected energy that returns to the radar not only indicates the presence of a target, but by comparing the received echo signal with the signal that was transmitted, its location can also be determined along with other target related information.

The basic principle of radar [11] is that the transmitter generates pulse of radio waves that is radiated into space by an antenna. A portion of transmitted energy is intercepted by the target and re-radiated in many directions. The re-radiated energy that is directed back towards the radar is collected by the radar antenna, which is delivered to a receiver [10]. There it is processed to determine the presence of the target and its location.

Radar is mainly classified into two, Continuous wave Doppler radar[1] and UWB Pulse Doppler radar. Continuous wave radar is a type of radar system where known stable frequency continuous wave radio energy is transmitted and then received from any reflecting objects. CW radar generally has a simple structure and is well known for its wide range of applications such as speed-limit enforcement, human gait analysis [4] [5], vital sign monitoring [2] [3].UWB Pulse Doppler radar is a radar system that determines the range to a target using pulse timing techniques, and uses the Doppler shift of the returned signal to determine the target objects velocity. The CW Doppler radar sends out a signal from a local oscillator (LO) and then collects the reflected signal using a super heterodyne receiver. The incoming signal is initially converted to an intermediate frequency (IF) to filter out the unwanted low-frequency components and the filtered IF signal is shifted to baseband using a digital down converter (DDC) module. FPGA Based Digital down converter ensures greater flexibility, compared to the conventional dedicated hardware components solution.

2. Related works

Radio receiver is an electronic device that receives radio waves and converts the information carried by them to a usable form with the help of an antenna. The antenna intercepts radio waves (electromagnetic waves) and converts them to tiny alternating currents which are applied to the receiver, and the receiver extracts the desired information. The receiver uses electronic filters to separate the desired radio frequency signal from all the other signals picked up by the antenna, an electronic amplifier to increase the power of the signal for further processing, and finally recovers the desired information through down conversion. Radio Receiver is classified into Homodyne Receiver and Heterodyne Receiver.

Homodyne receiver directly converts received radio frequency signal to base band signal without using an intermediate frequency (IF) stage. The homodyne method uses a local oscillator that is tuned to the carrier frequency of the desired station and mixed with the incoming signal to boost the power of that frequency before being filtered. Homodyne receiver suffers from several problems such as DC offset and low frequency noise from the power supply. Heterodyne receiver overcomes these limitations.

The operation of the heterodyne receiver depends on the use of frequency mixing. Basic block diagram is shown in Figure 1. In receiver reflected signal from the object is received by an antenna. Local oscillator in the receiver produces a sine wave which is mixed with that signal, shifting it to a specific intermediate frequency (IF) usually a lower frequency. Then it is shifted to base band signal with the help of low pass filter, ADC and mixers. In conventional heterodyne radar receivers the I/Q down conversion is performed in the analog domain.

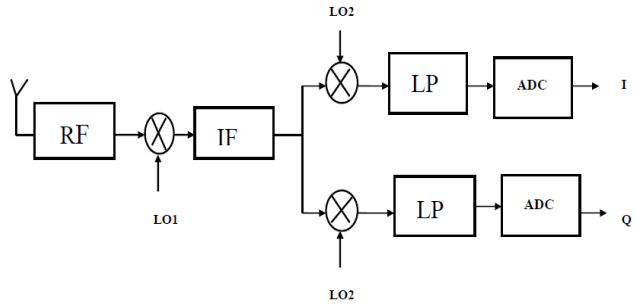

Figure 1: Conventional heterodyne receiver

Another drawback with the conventional heterodyne receiver is that two ADCs are required in each of the channel. Mismatch between these ADCs will reduce the receiver performance. Down conversion in digital domain can be used to avoid these limitations [9].

Digital I/Q down conversion based receiver structure contains a RF part with only one mixer stage which down converts the signal to an intermediate frequency signal. The signal is then band pass sampled by the ADC at IF and the I/Q down conversion is performed in the digital domain. Such receiver structure is shown in Figure 2. The RF and IF blocks in the figure consists of amplifiers and filters.

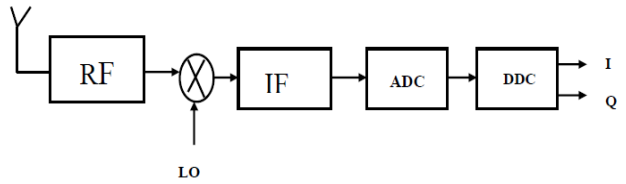

Figure 2: Heterodyne receiver structure with digital down conversion

3. Methodology

In radar receiver, reflected signal from the object is initially converted to an intermediate frequency (IF) to filter out the unwanted low-frequency components, the filtered IF signal is shifted to base band signal using a digital down converter (DDC) module.

3.1. System Overview

The basic block diagram of Digital down converter is as shown in the Figure 3. Initially the intermediate frequency is applied to the band pass filter to remove unwanted noise. The output of the band pass filter is applied to the ADC to convert analog input into digital form. This output is then fed to the parallel multiplier. Parallel multiplier multiplies the amplitudes of sine and cosine wave from the direct digital synthesizer with the ADC output. The output of the parallel multiplier is fed to the decimation filter. Decimation filter is used to reduce the sampling rate of the signal. Finally the base band signal is produced. The Main components of the Digital down converter are Direct digital synthesizer, Parallel multiplier and Decimation filter.

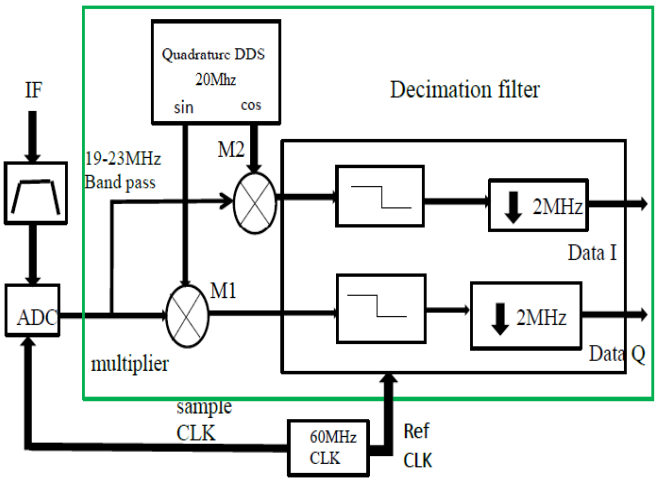

Figure 3: Block diagram of Digital down converter

3.2. Direct digital synthesizer

Direct digital synthesizer produces quadrature outputs from a reference clock. The basic block diagram is shown in Figure 4.

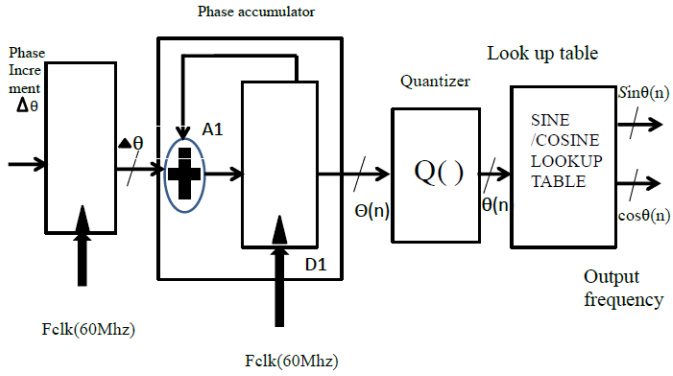

Figure 4: Block diagram of direct digital synthesizer

The main components of direct digital synthesizer [8] are phase accumulator, lookup table and quantizer. Phase accumulator is a combination of an overflow adder and a feedback register. The input frequency control word (fcw) is applied to the phase accumulator to produce a phase angle for the lookup table. The lookup table can be viewed as a mapper between an input phase angle θ and its corresponding sinθ and cosθ values. Quantizer act as a slicer between phase accumulator and look up table. Quantizer convert high precision angle to low precision angle. To reduce the look up table implementation complexity, the phase accumulator output typically is truncated [6] before being fed to the lookup table.

3.3. Parallel Multipliers

Parallel multiplier, accepts two signed input having a width of 16 bits and produce the product of these two values as the

output with a width of 32 bits. Parallel multiplier multiplies the ADC output and Direct digital synthesizer output. 16 bit parallel multipliers are based on the Baugh Wooley algorithm. This algorithm efficiently handles signed multiplication

3.4. Decimation Filter

The decimation filter is an important module that is present in the digital IF receiver part. The elimination of unwanted noise components is essential in maintaining the efficiency of receiver modules. With the use of decimation filter that operates at lower sampling rates the workload is almost reduced [7]. Decimation filter is a combination of cascaded integrator comb filter and a decimator. In the case of a decimating CIC, the input signal is fed through one or more cascaded integrators followed by a down-sampler and one or more comb sections. CIC filter consists of M integrator stage at high sampling rate and N comb stage at low sampling rate. Basic block diagram is shown in Figure 5.

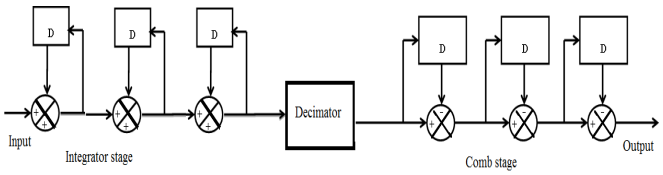

Figure 5: Block diagram of Decimation filter

The basic block diagram contains 3 integrator stages, 3 comb stages and a decimator. In each integrator stage sum of the input and output of the delay element is propagated to the next stage. Output of 3 stage integrator is fed to the decimator for reducing sampling rate and decimator output is fed to the Comb stage. In each comb stage difference between input and the output of delay element is propagated to the next stage. Final output is the baseband signal.

4. Results and Discussion

The FPGA based Digital down converter basically consists of three main blocks Direct digital synthesizer, 16 bit parallel multiplier and decimation filter. Initially the coding for the individual block was completed and then all the modules were combined by using the structural modelling. Simulation is carried out using Xilinx ISim simulator and Modelsim SE 6.2c and then synthesis is done using Xilinx ISE 14.2. The RTL schematic view of the Digital down converter is shown in Figure 6.

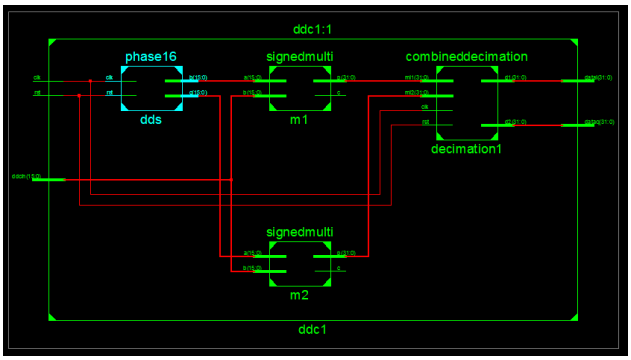

Figure 6: RTL-Schematic of Digital Down converter

Initially output from ADC is fed to the multipliers M1 and M2 present in the Digital down converter. Multiplier M1 multiplies amplitude of the sine wave from DDS and Digital output from the ADC. Multiplier M2 multiplies amplitude of the cosine wave from DDS and Digital output from the ADC. Then the outputs from the multiplier are fed to the decimation filter to obtain decimated output. The simulation result of Digital down converter is shown in Figure 7.

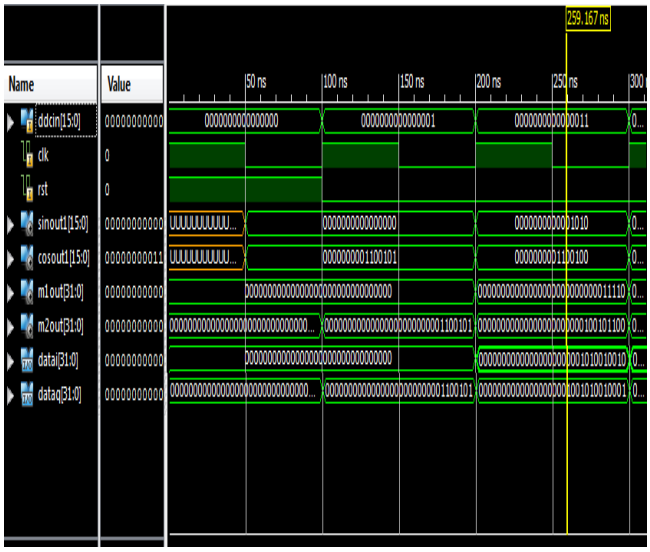

Figure 7: Digital Down Converter output

5. Conclusion

In radar receiver, reflected signal from the object is initially converted to an intermediate frequency (IF) to filter out the unwanted low-frequency components, the filtered IF signal is shifted to base band signal using a down conversion module. In conventional radar receiver the I/Q down conversion is performed in the analog domain. It suffers from several problems such as DC offset and low frequency noise from the power supply. Down conversion in digital domain can be used to avoid these limitations. The paper intends to develop a digital down converter which is a part of CW Doppler radar receiver. Digital down converter is mainly used to obtain the base band signal. Direct digital synthesizer, parallel multiplier and decimation filter are the main components of DDC.These modules are modelled in VHDL and simulation of the same is done using both Isim simulator and Modelsim SE 6.3f Simulator. The work also focuses on converting time domain output to frequency domain for better analysis.

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