International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

FPGA Based SPWM Generation Technique for Single Phase DC/AC Converters

Nithya S Kurup[1], Karthika Manilal[2]

[1]P G Scholar, VLSI and Embedded Systems, Department of ECE, T K M Institute of Technology, Kollam, India

[2]Assistant Professor, Department of ECE, T K M Institute of Technology, Kollam, India

Abstract*: Power electronics is the technology associated with efficient conversion, control and conditioning of electric power from its available input in to the desired electrical output form. It has found on important place in modern technology being a core of power and energy control. The SPWM or sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the on and off of the power switches. The SPWM principle is widely used in dc/ac converters in energy conversion and motor drive applications. In this thesis, an FPGA-based SWPM generator is presented, which is capable to operate at switching frequencies up to 1 MHz (requiring FPGA operation at 100-160MHz), thus it is capable to support the high switching frequency requirements of modern power electronic DC/AC converters. The proposed design exhibits architectural flexibility features, enabling the change of the SPWM switching frequency and modulation index either internally, or externally. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the DC/AC converter control unit complexity, cost and development time. Thus, the main contribution of this work is a system which is more faster in switching frequency than previously proposed ones and it has a more flexible architecture. Additionally, compared to the past-proposed designs, the proposed SPWM generation system exhibits less deviation of the generated SPWM output voltage from its theoretical value and consumes less power during operation. The VHDL language is used for coding and simulation is done using Xilinx ISE Design Suite 13.2.*

Keywords: PWM, SPWM, DC/AC converter, switching frequency.

1. Introduction

Power electronics is a subject that concerns the application of electronic-principles into situations that are rated at power level rather than signal level. The term power electronic converter system in general, is used to denote a static device that converts ac to dc, dc to ac, dc to dc or ac to ac. The DC/AC converters called inverters produce output AC voltage of controllable magnitude and frequency from input DC voltage. A power inverter or inverter, is an electronic device or circuitry that changes direct current (DC) to alternating current (AC). The inverter does not produce any power; the power is provided by the DC source. Inverters find wide use in induction-motor and synchronous-motor drives, induction heating, UPS, HVDC transmission etc. The pulse width modulation technique is widely used for the operation of an inverter. Output voltage from an inverter can be adjusted by exercising a control within the inverter itself. The most efficient method of doing this is by pulse width modulation. In this method, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. The PWM is a very advance and useful technique in which width of the gate pulses are controlled by various mechanisms. There are different types of pulse width modulators; they are single pulse width modulation, multiple pulse width modulation, and sinusoidal pulse width modulation. The sinusoidal pulse with modulation (SPWM) technique is widely employed in order to adjust the DC/AC inverter output voltage amplitude and frequency to the desired value. So the SPWM is widely used in power electronics to digitize the power so that a sequence of Voltage pulses can be generated by ON and OFF of the power converter switches. In a conventional inverter the output voltage changes according to the changes in the load, the PWM inverter correct the output voltage by changing the width of the pulses and the output AC depends on the switching frequency.

2. Theory

Modulation is the process of frequency transition in which any one of the parameters (amplitude, frequency or phase) of high frequency carrier signal is varied in accordance with instantaneous value of low frequency modulating signal[2]. Modulation is either analog or digital. Many signals in modern communication systems are digital due to reduced distortion and improvements in signal to noise ratios. The process of transmitting the analog signals in the form of pulses is called pulse modulation.

Pulse modulation includes:
1) Pulse amplitude modulation (PAM)
2) Pulse width modulation (PWM)
3) Pulse position modulation (PPM)
4) Pulse code modulation (PCM)
5) Delta modulation

In Pulse Amplitude Modulation (PAM), the amplitude is varied in accordance with the instantaneous value of the modulating signal. In PWM, the amplitude is maintained constant but the width of each pulse is varied in accordance with instantaneous value of the analog signal. In PWM, the sampled waveform has fixed amplitude and width where as the position of each pulse is varied as per instantaneous value of the analog signal. Pulse code modulation is a digital representation of an analog signal where the magnitude of the signal is sampled regularly at uniform intervals, then quantized to a series of symbols in a digital code. Delta modulation is a technique which provides a staircase approximation to an over sampled version of the message signal.

In pulse width modulation control, a fixed dc input voltage is given to the inverter and a controlled ac output voltage is obtained by adjusting the on and off periods of the inverter components. This is the most popular method of controlling the output voltage and this method is termed as pulse width modulation (PWM) control.

The advantages of the PWM control are:
1) PWM control is very simple and require very less hardware, So they are also cost effective.
2) They can easily implement using DSP or FPGA.

PWM waves are actually pulses of constant amplitude and varying pulse widths. This width can be varied by different modulation schemes. The most famous of these modulation schemes are analog technique and digital technique.

2.1 Analog Techniques

In analog technique there is one carrier wave which is basically high frequency triangular pulse train and modulating signal which can be sinusoidal, dc signal etc depending upon which type of modulation is used [4]. Then these two signals are compared using comparator to give desired PWM output. There are three basic modulation methods:
(a) Single pulse width modulation
(b) Multiple pulse width modulation
(c) Sinusoidal pulse width modulation.

a. Single Pulse Width Modulation
In the single pulse width modulation technique, square waveform is compared with triangular waveform and gets the resultant PWM signal [9]. This modulation gives quasi square wave output. There is single pulse of output voltage during each half cycle. RMS value of output voltage can be controlled by varying the pulse width. The ratio of triangular wave signal amplitude (Pc) and square wave signal (Pr) is called modulation index and it is calculated by M=Pr*Pc. The width of the pulse can be changed by varying the modulation index. When M=1, the square wave output is obtained

b. Multiple Pulse Width Modulation
This method of modulation is an extension of single pulse modulation. In multiple pulse width modulation technique, a dc signal is compared with triangular waveform and gets the resultant PWM signal. This modulation gives multiple pulses to reduce harmonic content. RMS value of output voltage can be controlled by varying the pulse width. The ratio of triangular wave signal frequency (Fc) and the output frequency (Fo) is called frequency modulation ratio. The width of the pulse can be changed by varying the amplitude of DC reference. Number of pulses per half cycle i.e. p = mf2. Where mf is the frequency modulation ratio.

c. Sinusoidal Pulse Width Modulation
Instead of maintaining the width of all pulses the same as in the case of uniform pulse width modulation, the width of each pulse is vary in proportion to the amplitude of a Sine wave evaluated at the center of the same pulse. The distortion factor and lower order harmonics are reduced scientifically. In the sinusoidal pulse width modulation, a sinusoidal signal is compared with triangular waveform and will get resultant PWM signal. The width of each pulse is weighted by the amplitude of sine wave at that instant. RMS value of output voltage can be controlled by varying the pulse width. The sinusoidal pulse width modulation is widely used in power electronics to digitize the power so that a sequence of voltage pulses can be generated by the ON and OFF of the power switches.

Advantages: low power loss, high accuracy of output waveform, easy to implement and control.

3. Methodology

The basic block diagram of a dc/ac converter is shown below.

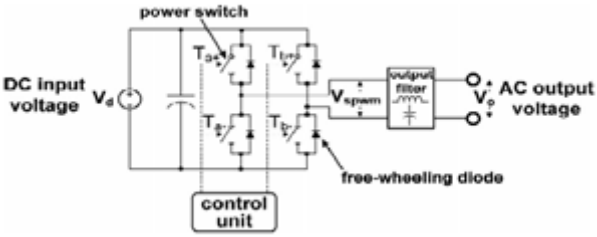

Figure 1: block diagram of a single phase dc/ac converter.

The power switches of the converter are set to the on or off state according to the Result of the spwm generator. The spwm technique is widely used to adjust the dc/ac Inverter output voltage, amplitude and frequency to the desired value. In this technique the generated pulses are either positive or negative during each half period of the spwm signal, Vspwm.

3.1 SPWM architecture

The architecture of the proposed SPWM is shown in the figure below.

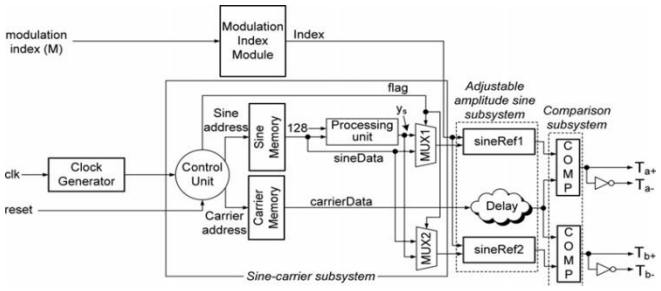

Figure 2: Architecture of SPWM.

It consists of five subsystems that implement the SPWM algorithm. The input of the system is the modulation index in single precision floating point arithmetic, while the system architecture is based on 8-bit fixed point arithmetic. The first subsystem, the clock generator, takes as input the FPGA's clock and produces a new one that allows the whole system to operate in the desired switching frequency. This clock generator consists of a Digital Clock Manager (DCM).The DCM plays the role of exactly adapting the external clock to the desired switching frequency by either increasing or

decreasing the corresponding FPGA clock frequency. The next subsystem is the modulation index subsystem, takes as input the modulation index, which ranges from 0 to 1. This value to be converted to fixed point arithmetic. Assuming there is an n-bit wide architecture, the equation to convert a floating point value to a given fixed-point architecture is the following:

$$Y_{M= M.(2^{n-1})+2^{n-1}} \quad (1)$$

Where M is the modulation index and n is the digital word length. The third subsystem consists of the control unit, two BRAMs, which contain the sinusoidal and the triangular values, respectively and two multiplexers which produce the two reference sine-waves either on a positive, or a negative cycle. In order to minimize the FPGA resource utilization, the memories were organized as follows; both the sinusoidal and the triangular pulses were sampled and quantized using MATLAB tool with the same sampling frequency, in order to produce the discrete values used for the BRAMs initialization over the corresponding sampling period. The sinusoidal memory contains the values of the first quarter of the sine-wave period [0,/2]. The values of the sine-wave in the other three quarters are calculated by mirroring and inverting the values of the first quarter.

The carrier memory contains the values of one period of the triangular wave. In this way, both the sine-wave and the carrier BRAMs operate as lookup tables (LUTs).The control unit also produces a flag signal, which is responsible for the retrieval of the sine wave values on a negative cycle. The sinusoidal-wave memory is scanned up and down four times, since this memory contains only the first quarter of a sinusoidal period. Memory up/down counting determines the value of the flag signal. When the flag is set to 0, the multiplexer outputs the data read from the sinusoidal memory (SineData). Otherwise, the multiplexer outputs the sinusoidal values on the negative cycle that correspond to the values read from the memory after processing [Negative Value (y)]. The conversion of the positive values stored in the sinusoidal memory to the corresponding negative values is performed according to the following equation:

$$Y_{x= x-[(x-2^{n-1}).2]} \quad (2)$$

Where x is the positive value stored and n is the digital word length (n=8 in the proposed architecture). The second multiplexer is used for the production of the second reference Sine-wave operating exactly on the opposite mode from the one analyzed above. Consequently, this subsystem outputs the two reference sinusoidal and triangular values (SineRef1, SineRef2 and CarrierData), respectively, synchronized in every clock cycle over a sinusoidal sampling period. The adjustable amplitude sine subsystem, takes as input the reference sinusoidal values [”SineRef (y)”] produced by the subsystems described above and generates a sinusoidal digital signal [”sineAdjustable (x)”], with amplitude adjustable according to the modulation index value, which is also input of this subsystem. The adjustable amplitude, sine-wave digital signal, which is 8-bit wide and takes values in the range 0-255, follows the equation:

$$y_{a=}((y-2^{n-1}).(index-2^{n-1}))/(2^{n-1})+2^{n-1} \quad (3)$$

Where y is the reference sine-wave value and index is the output of the Modulation Index Subsystem. The comparison subsystems implement the comparison between the high frequency, constant-amplitude triangular wave (carrier) with the two low-frequency reference sine-waves of adjustable amplitude, using a simple comparator. The control signals Ta+ and Tb+ of the DC/AC inverter power switches, comprising the SPWM pattern, are generated from the outputs of the corresponding comparators. The output of each comparator is equal to one when the output of the corresponding adjustable amplitude sine subsystem is equal to or greater than the digital value of the carrier signal. Moreover, the inverted SPWM pulses are generated in order control the DC/AC inverter power switches Ta- and Tb-.

4. Results and Discussion

The modules are modelled using VHDL in Xilinx ISE Design Suite 8.1i and the simulation of the design is performed using Modelsim SE 6.3f and Simulink to verify the functionality of the design.

4.1 Simulink Modeling

The SPWM architecture is first simulated in matlab and simulink. The pulse widths are produced by comparing the two reference sine waves and the triangular carrier wave. So two reference sine waves are generated by using signal generator and carrier triangular waves are generated by using triangular wave generator. Then the comparison between these three signals are done by using an AND operator i.e., simple multiplication of signals are used for comparison.

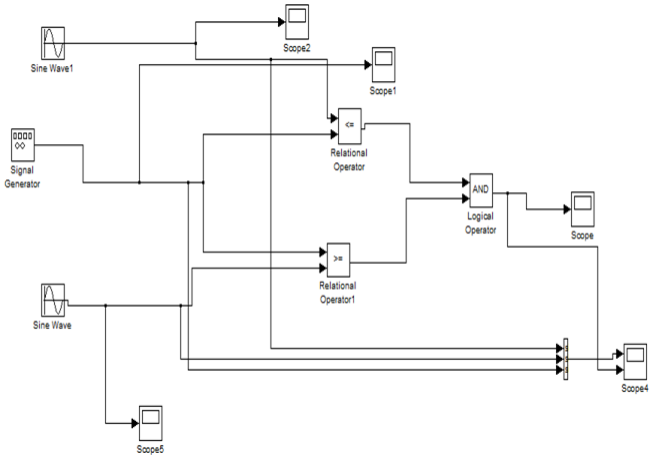

Figure 3: Simulink modeling of SPWM

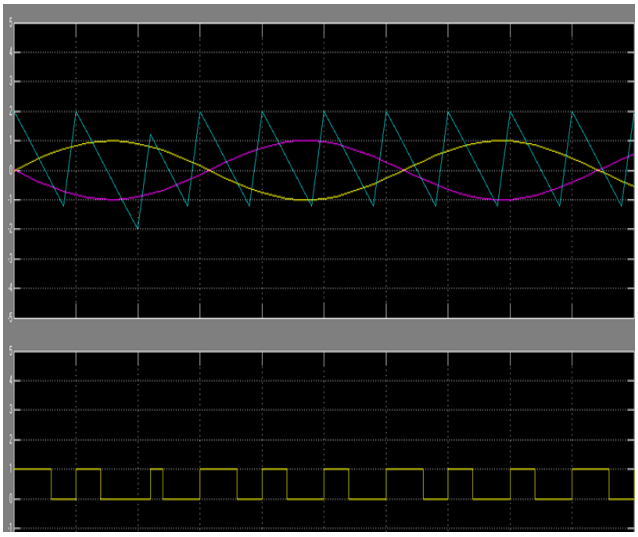

Figure 4: Output Waveform of SPWM (simulink)

4.2 SPWM Generator

The architecture presented in the previous Section has been synthesized using the VHDL language and its correct operation has been verified using the ModelSim 6.3f simulator. The SPWM output is generated at the intersection of the sinusoidal and triangular waveforms at certain sampling instants. When the value of each sine-wave is higher than the triangular wave value, the output pulse is set to logical 1, else it is set to logical 0. The sinusoidal and triangular wave values are generated by using matlab and stored these values in the form of an array and stored in LUT. The Comparison subsystem implements the comparison between the high-frequency constant-amplitude triangular wave (carrier) with the two low-frequency reference sine waves, using two comparators. The control signals g1, g2, g3, and g4 of the single phase dc/ac inverter power switches are generated from the outputs of the corresponding comparators of this subsystem, thus forming the SPWM wave at the dc/ac inverter output terminals. The DC/AC inverter control signals g2 and g4 are produced by inverting g1 and g3, respectively.

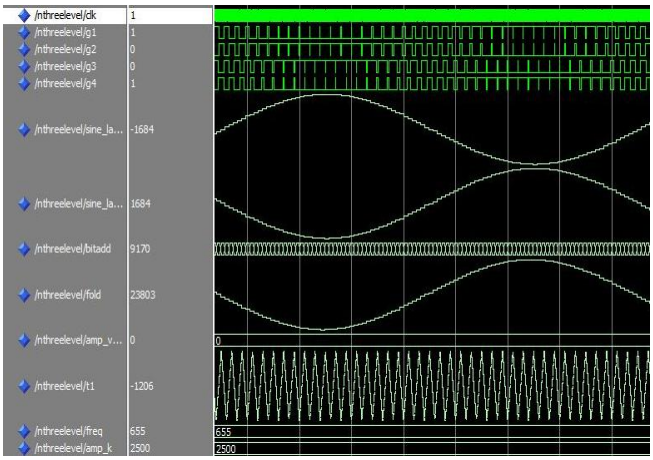

Figure 5: Output Waveform of SPWM(modelsim)

4.3 Digital Clock Manager

The input of the SPWM generator is the FPGA input clock and produces a new clock signal used by the digital circuits of the proposed SPWM generator, such that the desired SPWM switching frequency fc specified by the designer/user is generated. A Digital Clock Manager module adapts the frequency to the desired value. The simulation of clock generator was done by using modelsim and result is shown below:

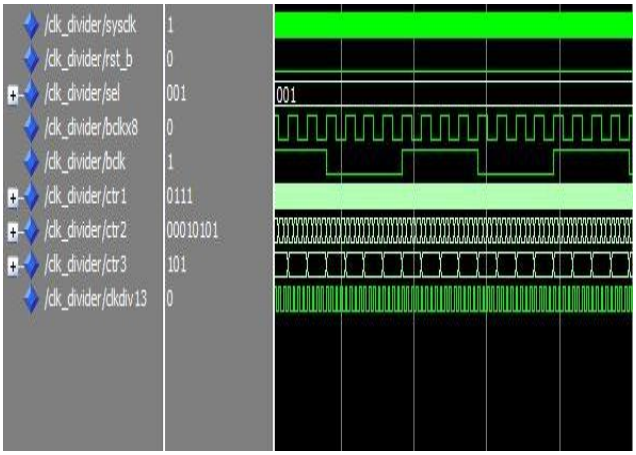

Figure 9: Simulation of DCM (Digital Clock Manager

References

[1] N. Mohan, T. Undeland, W. Robbins, Power Electronics: Converters, Applications and Design, second ed., Wiley, 1995.
[2] Timothy L. Skvarenina, Power Electronics Handbook, second ed., 2002.
[3] S. R. Bowes and D. Holliday, ”Optimal regular-sampled PWM inverter control techniques,” IEEE Trans. Ind. Electron., vol. 54, no. 3, pp. 1547 1559, Jun. 2007.
[4] N. D. Patel and U. K. Madawala, ”A bit-stream-based PWM technique for sinewave generation,” IEEE Trans. Ind. Electron., vol. 56, no. 7, pp. 25302539, Jul.2009.
[5] H. Hussin, A. Saparon, M. Muhamad, and M. D. Risin, ”Sinusoidal pulse width modulation (SPWM) design and implementation by focusing on reducing harmonic content,” in Proc. 4th Asia Int. Conf. Math./Anal. Modell. Comput. Simul., 2010, pp. 620623.
[6] R. K. Pongiannan, S. Paramasivam, and N. Yadaiah, ”Dynamically reconfigurable PWM controller for three-phase voltage-source inverters,” IEEE Trans. Power Electron.,vol. 26, no. 6, pp. 17901799, Jun. 2011.
[7] A. M. Hava and N. O. C etin, ”A generalized scalar PWM approach with easy implementation features for three-phase, three-wire voltage-source inverters,” IEEE Trans. Power Electron., vol. 26, no. 5, pp. 13851395, May 2011.
[8] D. Navarro, O. Luci c, L. A. Barrag an, J. I. Artigas, I. Urriza, and O. Jime nnez, ”Synchronous FPGA-based high-resolution implementations of digital pulse-width modulators,” IEEE Trans. Power Electron., vol. 27, no. 5, pp. 25152525, May 2012.
[9] Koutroulis E., Dollas A. and Kalaitzakis K., ”High-frequency pulse width modulation implementation using FPGA and CPLD ICs”, Journal of Systems Architecture, Vol.52 (2006): pp. 332344.