International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

DWT & IDWT Design Implementation using FPGA

Tasneem Kausar[1], Pooja Thakre[2]

RTMNU University, NUVA College of Engineering & Technology, Katol Road, Nagpur, Maharashtra, India

NUVA College of Engineering & Technology, RTMNU University, Katol Road, Nagpur, Maharashtra, India

Abstract*: In this paper three filter bank structure are evaluated by Field Programming Gate Array implementations. The traditional non polyphase structures, traditional polyphase structure and lifting structures are three filter banks. The compression performance are examined by three filter structure. For the filter coefficients, optimal quantized values are found for each structure. Discrete Wavelet Transform codec generates the best possible Peak signal to noise ratio performance for a given structure using these coefficients, in Discrete Wavelet Transform we use filter bank instead of using a single filter. By evaluating the performance optimal choices can be made for a biorthogonal 9/7 Discrete Wavelet Transform implementation based on the given application. After quantization here filter bank properties are preserved and not the properties of single filter. In this traditional Discrete Wavelet Transform can be implemented in multiple ways and then it introduces figure of merit examined hardware implementation. Two quantization techniques are used to better the performance of quantized filter bank to get higher throughput filter bank in polyphase form is used than non polyphase structure. In lifting structure, six different optimal quantized lifting implementations are designed and evaluated. To accept the proposed scheme, for the 2-dimentional Discrete Wavelet Transform computation this circuit is designed, simulated, and implemented in Field Programming Gate Array.*

Keywords: Field programming Gate Array (FPGA); Discrete Wavelet Transform(DWT);VHDL.

1. Introduction

This paper concentrates on a Field Programmable Gate Array (FPGA) implementation of a DWT code for the Biorthogonal 9/7 wavelet. Perfect Reconstruction (PR) filter bank is usually used for the computation of Discrete wavelet transform. The behavior of an FPGA implementation of the filter bank vary depending on Filter bank structure and filter coefficient quantization and the hardware architecture used to implement the filter bank structure.

The image compression ability of the filter bank implementation critically depends on the two perfect reconstruction (PR) conditions: the no-distortion condition and the no-aliasing condition. If irrational coefficient of biorthogonal 9/7 wavelet transform filter used in a floating point format then above stated two perfect reconstruction conditions are satisfied and perfect reconstruction is achieved under lossless compression by filter bank. If we present filter coefficient on a Sum- and – difference of powers of two(SPT) in a multiplier manner, fast hardware implementation on a FPGA can be achieved. Now multiplication is achieved by shifting and adding. So filter coefficient are approximated by fixed point SPT representation that is the coefficient of filter should be quantized. Hardware cost associated with implementing the coefficient is denoted by T which is number of non zero term in the SPT representation of a coincident.

FPGA implementations of three filter bank structures is checked in this paper The three structures are traditional lifting structure, polyphase structure and traditional non-polyphase structure. The above stated three structures are examined in terms of compression performance using peak signal to noise ratio (PSNR) and various hardware metrics. The Quantized Optimal value for each structure are found for filter coefficient. These coefficients are needed for the fast implementation, multiplier less Discrete Wavelet Transform (DWT) codec that produces the best PSNR behavior of the structure. This comprehensive behavior analysis makes it possible to make best choices for a biorthogonal 9/7 DWT implementation based on the requirement of the given application.

Hardware metric such as throughput and latency are found out by using filter bank structure and filter coefficient has its effect on the signal processing properties of the filter bank and determines its image compression view. Latency is power consumption properties are found using hardware architecture of filter bank.

2. Design and Implementation

2.1 Filter Structure and Quantization

Before implementation we need to quantize filter coefficient in fast hardware. Because of this frequency response of the filter is changed. If quantized filter is used in filter bank it affects perfect reconstruction properties of filter bank and also image compression performance is compromised. If we quantize filter coefficient in such a manner so that filter bank properties are conserved than minimum degradation will be caused to image compression properties. The coefficient quantization filter structure plays an important role in the performance of filter bank. Some filter structure are not affected by coefficient quantization than others and these filter structure can be utilized to minimize performance degradation of the filter bank. This paper examines two filter structure and two compensating coefficient quantization method to obtain better performance from multiplier quantized filter banks. Instead of using optimization technique the new method make use of perfect reconstruction requirement of filter bank. The design process can be widely used with any biorthogonal perfect reconstruction filter bank having finite length filters. If each filter remains symmetric after coefficient quantization then linear phase and no-aliasing condition can be saved. The magnitude response of

the low pass branches of the filter bank find out that no distortion condition is satisfied or not.

2.2 Polyphase Implementation

In this section of data throughput, regardless of whether the filters are implemented in the direct form or as a cascade of sections. During analysis stage down sampling and filtering is performed. In this method half samples are discarded which are computed by filters and due to this output rate in analysis stage is half of input rate. During synthesis stage the up sampling operation is done before filtering operation at double input rate. Since up sampling inserts zeros in the input data half of the multiplier in the synthesis filter are multiplied by zero so half mathematical operation is wasted.

2.3 Direct form implementation

Sixteen coefficients must be quantized for direct form implementation of two low pass filter. The number of non zero terms in the SPT representation of coefficient should be kept to minimum value so that test hardware performance is achieved. The important part here is that how to distribute available T across the coefficient so that best compression performance is achieved. In the first method uniform distribution of the T across sixteen coefficient are done. This allocation is referred as uniform allocation. Here improve performance of the filter bank is achieved by taking advantage of the relationship between the quantized filter and the no distortion perfect reconstruction condition.

2.4 Direct polyphase structure

In a polyphase, direct implementation of biorthogonal 9/7 filter bank filter is divided into even and odd phase. Still each phase remains symmetric. A direct form polyphase implementation needs the sum total no. of SPT terms on the direct form without polyphase. But direct form polyphase implementation is advantageous because we get double throughput without substantial change in hardware cost. Both structures gives same data output and their effect on image compression quality is same. Both structures when implied encounter some problem.

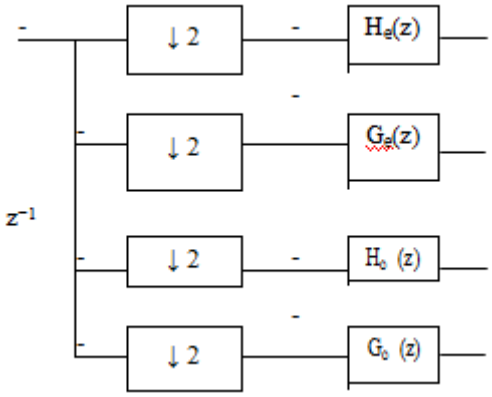

Figure 1: Direct Polyphase Structure for the Filter Banks

2.5 Cascade Structure

In polyphase cascade structure the filter is designed such that down sampling operation is moved to filter input using noble identity. The equation in polyphase representation of both cascaded structure are used such that delays are first grouped and factored out and then noble identity is employed. In cascade filter structure zeros at z=-1 are placed in a separate filter section to ensure that they are not disturbed even after coefficient quantization in the below figure shows.

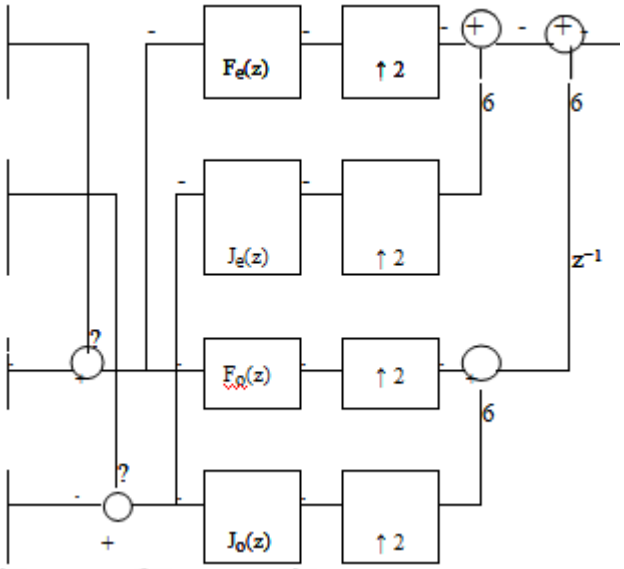

Figure 2: Cascade structure

2.6 Lifting Implementation

The polyphase and non polyphase implementation of biorthogonal 9/7 DWT use mallat's pyramid algorithm based on perfect reconstruction filter bank. Here we analyze the "lifting" approach for computing the DWT. Lifting gives us very effective substitute than the traditional convolution filter bank implementation. It has various advantages over the traditional convolution filter bank method. It requires less no. of computation than conventional method. Lifting provides thus same output rates in the analysis stage on the input rate. Here we are changing low pass and high pass filtering functions by lift and update filter and then using scaling step in the end. The synthesis part of the filter bank inverts the scaling. It inverses the sequence of lifting and update step. If scaling factors ζ and $1/\zeta$ are not getting into account and no compression is done than analysis is exactly complemented, no matter what quantized values we used for α, β, γ, δ. So lifting structure provides substantial advantage over convolution.

Here also we employ more SPT term to represent lifting coefficient. If quantized lifting coefficient are closer to unquantized coefficient then we get PSNR values achieved by fixed point hardware closer to the PSNR values obtained with unquantized coefficient. The low pass and high pass filters has four zeros at z= -1 and 1 in the unquantized 9/7 analysis. These zeros helps to find out the flatness of the analysis and synthesis scaling function and it also prevents DC leakage in analysis high pass filter. The rational lifting coefficient produces PSNR values almost exactly equal to irrational coefficients PSNR values.

2.7 Lifting Coefficient Quantization

2.7.1 Quantization objectives

Lifting structure for hardware implementation needs quantization of six lifting coefficients α, β, γ, δ ,ζ and 1/ζ. The analysis filters for magnitude response of substitute by quantization of six lifting coefficients. In this paper , the magnitude response of quantized analysis filters which is equal to the magnitude response of the unquantized 9/7 filters[H(z) & G(z)] is made by good compression performance. The shape of magnitude responses are find out by quantized lifting coefficients α, β, γ ,δ and DC gain and Nyquist are find out by ζ and 1/ζ quantized value.

2.7.2 Quantization of irrational coefficients

The problem of allocating a fixed number T of SPT terms to the six coefficients are faced by lifting coefficient quantization even though hold the adequate quality of reconstructed image. It occur in the absence of checker boarding artifact.

2.7.3 Quantization of rational coefficients

α, β and δ can be used in small SPT terms where as γ, ζ and 1/ζ can be used infinitely long SPT representations. Approximations require fixed point γ, ζ and 1/ζ quantization.

3. Conclusion

In this paper image compression applications with filter coefficient quantization and filter bank structure for fast multiplier less implementation of biorthogonal 9/7 DWT are introduced. Impact perfect reconstruction properties and degrade image compression performance of the filter bank are called as quantization of filter bank coefficients even though hardware metrics, latency & power consumption for implementation are found out by filter bank structure. This work finds which filter bank structure is best for a FPGA implementation and reach at an optimal set of quantized coefficients for this structure.

Polyphase structures make better efficiency of traditional filter bank by avoiding wasted computations. The polyphase structure combined with superior compression. Performance of cascade form and Z_1 compensation coefficients were getting by the cascade polyphase structure resulting in fast low power implementation.

References

[1] ITU-T Recommendation T.800. JPEG2000 image coding system - Part 1, ITU Std., July 2002. [Online]. Available: http://www.itu.int/ITU-T/

[2] Skodras, C. Christopoulis, and T. Ebrahimi, “The JPEG2000 still image compression standard,” IEEE Signal Processing Mag., vol. 18, no. 5, pp. 36–58, September 2001.

[3] S. Traferro, F. Capparelli, F. Piazza, and A. Uncini, “Efficient allocation of power of two terms in FIR digital filter design using tabu search,” in Proc. IEEE Int’l. Symposium on Circuits and Systems, vol. 3, 1999, pp. 411–414.

[4] Y. Lim, R. Yang, D. Li, and J. Song, “Signed power-of-two term allocation scheme for the design of digital filters,” IEEE Trans. Circuits Syst. II, vol. 46, no. 5, pp. 577–584, May 1999.

[5] Y. Lim and S. Parker, “FIR filter design over a discrete power-of-two coefficient space,” IEEE Trans. Acoust., Speech, Signal Processing, vol. ASSP-31, pp. 583–591, June 1983.

[6] N. Cho and S. Lee, “Optimal design of finite precision FIR filters using linear pro-gamming with reduced constraints,” IEEE Trans. Signal Processing, vol. 46, no. 1, pp. 195–199, January 1998.

[7] J. Mao, S. Chan, W. Liu, and K. Ho, “Design and multiplier-less implementation of a class of two- channel PR FIR filter banks and wavelets with low system delay,” IEEE Trans. Signal Processing, vol. 48, no. 12, pp. 3379–3394, December 2000.

[8] A. Akansu, “Multiplier less PR quadrature mirror filters for sub band image coding,” IEEE Trans. Image Processing, vol. 5, no. 9, pp. 1359–1363, September 1996.

[9] Y. Chen, S. Oraintara, T. D. Tran, K. Amaratunga, and T. Q. Nguyen, “Multiplier less approximation of transforms using lifting scheme and coordinate descent with adder constraint,” in IEEE Proc. Int’l Conf. Acoust., Speech, Sig. Proc. (ICASSP), vol. 3,