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Analog VLSI Implementation of Neural Network Architecture

Abhishek K. Shrinath

Department of Electronics & Communication Engineering, Shri Sant Gadgebaba College of Engineering, Bhusawal, Maharashtra, India

Abstract: ***Artificial intelligence is realized using artificial neurons. In the proposed design, we are using Artificial neural network to demonstrate the way in which the biological system processes in analog domain. The analog components like Gilbert Cell Multiplier (GCM), Adders, Neuron activation Function (NAF) are used in the implementation. This neural architecture is trained using Back propagation (BP) algorithm in analog domain with new techniques of weight storage. We are using 45nm CMOS technology for layout designing and verification of proposed neural network. The proposed design of neural network will be verified for analog operations like signal amplification and frequency multiplication.***

Keywords: Gilbert cell, neuron activation function, neural network, Analog Signals, VLSI.

1. Introduction

Intelligence is the computational part of the ability to achieve goals in the world. Artificial Intelligence is implemented by using neuron and these artificial neurons comprised of several analog components .An ANN is configured for a specific application pattern recognition ,function approximation ,learning in biological system involves adjustment to synaptic connection that exists between the neuron. The most promising approach for implementing neural network is to fabricate special purpose very large scale integrated chip.The neuron selected a analog component like multiplier and adder along with the tan-sigmoid function.

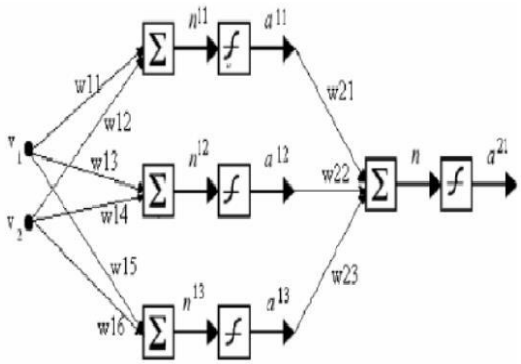

Figure 1: Layered neural network

The neural network is shown in the above figure. In this network, inputs are applied with the weight matrix, and then this weighted inputs of the adder are summed up. The output generated by adder blocks is given to the Neuron Activation function. The output of activation function is multiplied by weights again and given to the input blocks of output layer. This layered structure of neural network is implemented in VLSI using analog components. Gilbert cell multiplier, adder and differential amplifier are used for different blocks.

2. Literature Review

[1] Neeraj Chasta 1, Sarita Chouhan2 and Yogesh Kumar3 review of related work and published literature he design the implementation of Neural Network Architecture (NNA) with on a chip learning in analog VLSI for generic signal processing applications . He also say that Neural network with their remarkable ability to derive meaning from complicated or imprecise data can be used to extract patterns and to detect trends that are too complex to be noticed by either humans or other computer techniques. Due to its adaptive learning, self-organization ,real time operations and fault tolerance via redundant information coding properties it can be used in Modelling and Diagnosing the Cardiovascular System and in Electronic noses which has several potential applications in telemedicine. Another application developed was "Instant Physician" which represents the "best" diagnosis and treatment. This work can be further extended to implement neuro fuzzy system with high speed low power.

[2] Vincent F. Koosh, Rodney Goodman review of related work and published literature, it is observed that a VLSI implementation of a neural network has been demonstrated. Digital weights are used to provide stable weight storage. he also say that analog multipliers are used because full digital multipliers would occupy considerable space for large networks. Although the functions learned were digital, the network is able to accept analog inputs and provide analog outputs for learning other functions. A parallel perturbation technique was used to train the network successfully on the 2-input AND and XOR functions.

[3] From the continuous survey it is observed by B. M. Wilamowski, J. Binfet, and M. O. Kaynak Fuzzy controllers do have several advantages such as simple rule based design, but they usually produce relatively raw control surfaces, which are not acceptable for precision control. These fuzzy control surfaces also exhibit larger errors, 908.4 and 296.5. With the neural network approach presented in this paper, the resulting control surfaces are very smooth. Although the presented examples were for a two input case, the general nature of neural systems is such that they can easily handle multidimensional problems. This is not true for the fuzzy systems where the number of inputs is severely limited because with an increased number of inputs, the size of the rule table grows exponentially.

[4] Jabri,M. SydneyUniv.,NSW,Australia Pickard,S. ; Leong,P. ; Rigby,G. ; Jiang,J. Flower, B. ; Henderson, P. Mapping a functional neural network model to analog subthreshold MOS technology is a challenging task, and requires careful architectural, system level and circuit level consideration, with respect to the constraints inherent in this technology. The authors present their experience in this mapping process. The artificial neural network systems addressed are programmable ones facilitating learning either on or off chip. The authors consider multilayer feedforward networks, although the techniques can be easily adapted to recurrent networks. A multi-layer learning algorithm suitable for analog sub-threshold implementation is presented. The authors discuss system level issues, describe circuits of neurons and synapses that have been designed, and present fabrication results

[5] Wai-Chi Fang review of related work and published literature, a frequency-sensitive self-organization network has been described and shown to be effective for adaptive vector quantization. The efficiency of this FSO network is measured by its compression ability, the resulting distortion, error tolerance, and the suitability for VLSI implementation. Based upon this frequency-sensitive self organization method, a neural-based adaptive vector quantizer has been developed. By using a mixed analog digital design approach in the massively paralleled computation blocks, the advantages of small silicon area, low power consumption, and reduced I/O requirement can be achieved. A VLSl chip for 25-dimensional vector quantizer of 64 code vectors has been fabricated and tested. Its throughput rate is 2 million vectors per second and its equivalent computation power is 3.2 billion connections per second. It achieved an intrinsic compression ratio of 33.

[6] Yammenavar et al. this paper makes use of Artificial Neural Network to demonstrate the way in which the biological system processes in analog domain.Using180nm CMOS VLSI technology for implementing analog and digital circuits which performs arithmetic operations and for implementing Neural Network required large input The technology we are using to convert the given network in analog VLSI chip design is 45nm CMOS technology. The analog components used are comprised of multipliers and adders along with the tan-sigmoid function circuit. This neural network uses unsupervised learning algorithm. Using 45nm VLSI technology for implementation of feed forward neural network. The most important message here is that the logic complexity per chip has been (and still is) increasing exponentially. The monolithic voltage range & large area required for chip designing in 180 nm technology may occurred problem for signal amplification for speed, power and circuit design area. we are implementing this neural network by using different block like multiplier, adder and neuron activation function by using 45 nm CMOS technology with the required parameters .

3. 45 nm cmos Technology

Integration of a large number of functions on a single chip usually provides:

1) Less area/volume and therefore, compactness.
2) Less power consumption.
3) Less testing requirements at system level.
4) Higher reliability, mainly due to improved on-chip interconnects.
5) Higher speed, due to significantly reduced interconnection length.
6) Significant cost savings.

4. Simulation Result and Discussion

The inputs to the neuron v1 and v2 as shown in figure 1.1 are multiplied by the weight matrix; the resultant output is summed up and is passed through an NAF. The output of the activation function is then passes to the next layer for further processing. Blocks to be used are Multiplier block, Adders, NAF block with derivative.

4.1 Neural Network for Signal Compression

Using the main blocks of Gilberts cell multiplier & Neuron activation function (NAF) in 45 nm technology for signal compression in neural network. Figure 4.1 shows the schematic of neural network for signal compression. Here two analog signals are given as inputs single & output obtained which is compressed analog signal.

Figure 4.1 Schematic of neural network for signal compression

4.2 Layout of Neural Network for Signal Compression

Figure 4.2 shows the layout of neural network for signal compression which is designed using microwind 3.1 software in 45 nm cmos technology

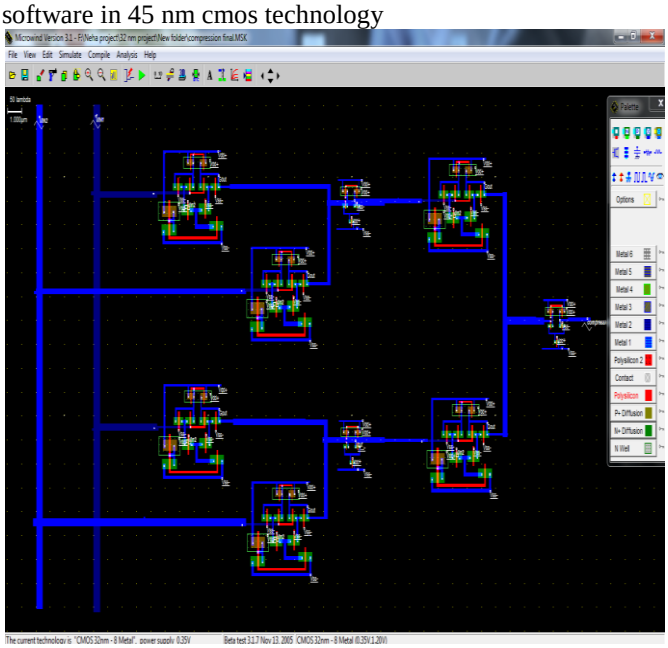

Figure 4.2 Layout of neural network for signal compression

4.3 Simulation of Neural Network for Signal Compression

Figure 4.3 shows the voltage versus time response of neural network for signal compression

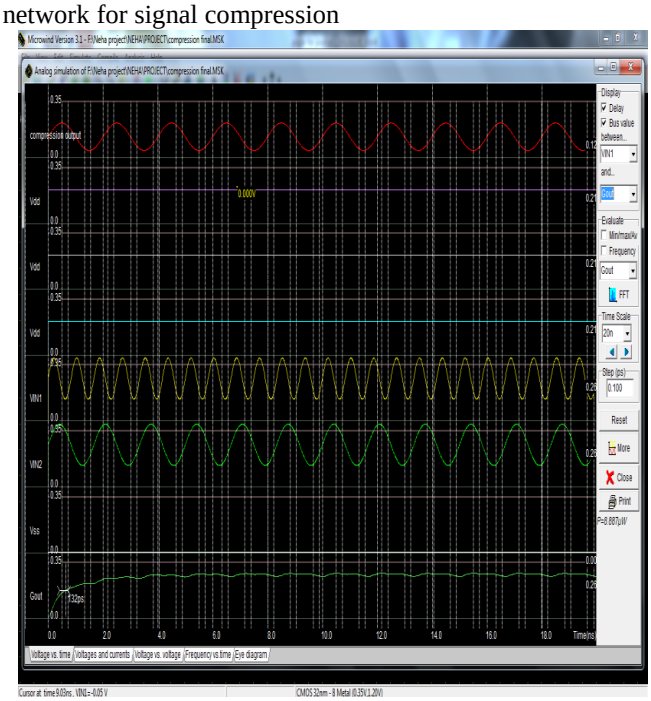

Figure 4.3 Voltage versus time response of neural network for signal compression

4.4 Neural network for Signal Decompression

Using the main blocks of Gilberts cell multiplier & Neuron activation function (NAF) in 45 nm technology for signal decompression in neural network. Figure 4.4 shows the schematic of neural network for signal decompression. Here the input of the decompression of neural network is Compressed analog signals & output obtained two analog signals which are given as a input of compression of neural network.

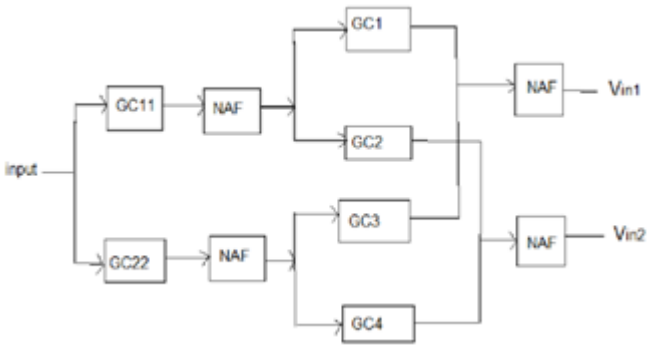

Figure 4.4 (a) Schematic of neural network for signal decompression

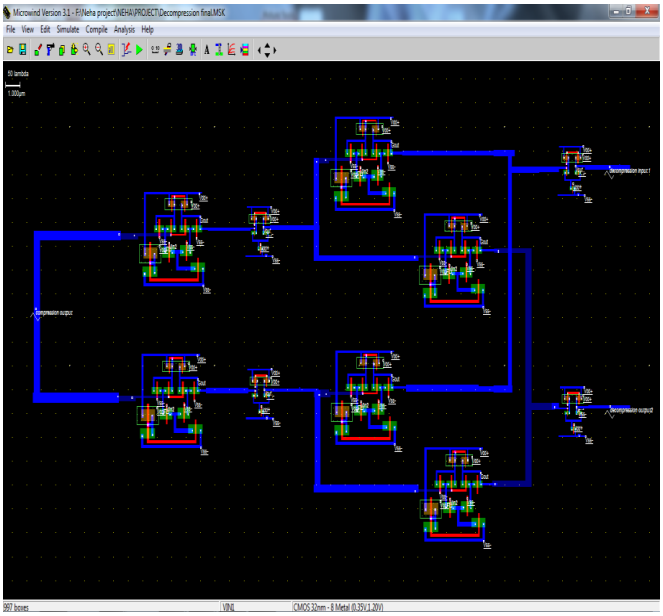

Figure 4.4 (b): Layout of neural network for signal decompression

4.5 Simulation of neural network for signal decompression

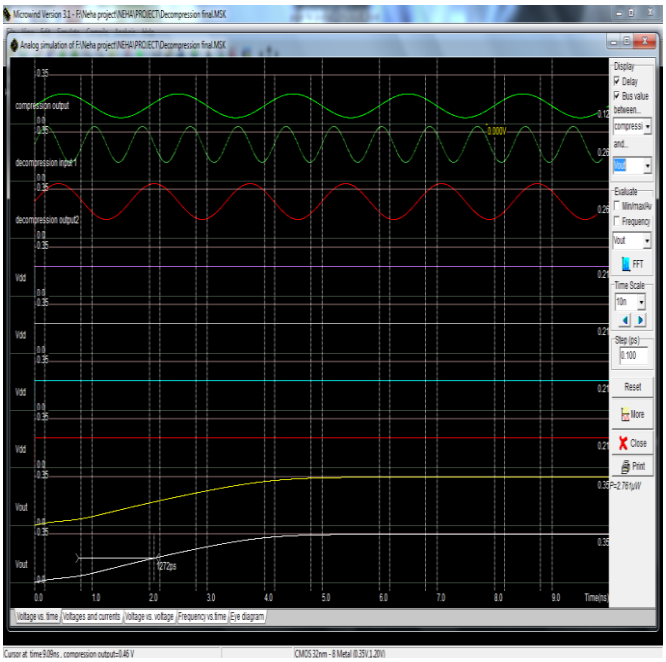

Figure 4.5: Voltage versus time response of neural network for signal decompression

5. Conclusion

VLSI technology is the fastest growing field today. Considering the advancement of future technology and the advantage of 45 nm technology over 65 and 90 nm technology, the selection of 45nm technology for the proposed project was the proper choice of technology. The VLSI implementation of a feed forward neural network for analog signal processing has been demonstrated in this project. To give an application oriented approach two analog signals are compressed and decompressed using the designed feed forward neural network and the simulation results are obtained in 45nm CMOS VLSI technology.

References

[1] Cyril Prasanna Raj P & S.L. Pinnae "DESIGN AND ANALOG VLSI IMPLEMENTATION OF NEURAL NETWORK ARCHITECTURE FOR SIGNAL PROCESSING". European Journal of Scientific Research ISSN 1450-216X Vol.27No.2 (2009), pp.199-216.
[2] Neeraj Chasta, Sarita Chaouhan & Yogeshkumar "Analog VLSI Implementation of Neural Network for Signal Processing". International Journal of VLSI design & Communication System (VLSICS),Vol.3, No.2,April 2012.
[3] Roy LudvigSigvartsen, An Analog Neural Network with On-Chip Learning Thesis Department of information, University of Oslo, 1994.
[4] Prem Kumar & G.R.C. Kaladhara Sarma "Developing a VLSI Architecture Simulation for Neural Networks Based Image Compression Neural Network". Journal of information, knowledge and research in and communication.
[5] Bapuray.D.Yammenavar1, Vadiraj.R.Gurunaik2, Rakesh.N.Bevinagidad3 and Vinayak. U. Gandage "DESIGN AND ANALOG VLSI IMPLEMENTATION OF ARTIFICIAL NEURAL NETWORK". International Journal of Artificial Intelligence & Applications (IJAIA), Vol.2, No.3, July 2011.
[6] E. Vittoz, et al., "The design of high performance analog circuits on digital CMOS chips," IEEE J. Solid State Circuit 20, 1985, pp.657-665.
[7] S. R. Kshirsagar & A.O.Vyas "Signal Processing in Neural Network using VLSI Implementation". Journal of Engineering and Computer Science, Issue June 2013.
[8] E. Vittoz, et al.," The design of high performance analog circuits on digital CMOS chips," IEEE J.SolidState Circuit 20, 1985, pp.657-665

Author Profile

Abhishek k Shrinath is a PG student, SSGB Bhusawal ,North Maharashtra University jalgoan. BE , from PRMIT&R Badnera ,SSGB Amravati university, Amravati Maharashtra, India.