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Design and Implementation of 8 BIT Vedic Multipliers USING HNG Gates

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Abstract: ***Now a days, reversible logics are emerging field in VLSI design in which Energy dissipation is an important consideration. Reversible logic is first related to energy. Researcher like Landauer states that information loss due to function irreversibility leads to energy dissipation. Thus reversibility will become an essential feature in future electronics circuit design. Reversible circuits are of high interest in applications like DSPs, low power CMOS design, nanotechnology, optical computing and quantum computing etc. The main aim and purpose of this paper is to improve the speed and power dissipation of the processor by using efficient Vedic multiplier. Vedic multiplier known as "Urdhva Tiryakbhayam" which means vertical and crosswise in English. This multiplier is designed and implemented using reversible logic Feynman Gate, Peres Gate and HNG gate. Feynman and Peres gates are used to implement the basic two bit multipliers and HNG gate is used as full adder for summation of the partial product generated by two bit multipliers in four bit multiplier. 8*8 bit multiplier is designed using four bit multipliers and three eight bit ripple carry adders. The proposed system is designed using VHDL and implemented through Xilinx ISE 13.2 Navigator.***

Keywords: Vedic multiplier, Urdhva Tiryakbhayam , Reversible logic gates, Garbage outputs, Constant outputs, *Xilinx Sparta 3E FPGA kit*

1. Introduction

In modern VLSI circuit design, reduction of power dissipation is very important goal. Multiplication is very important function in arithmetic operations. It is one of the most silicon intensive functions, especially when implemented in Programmable Logic. Multiplier is the important key components of many high performance systems such as DSPs, Microprocessors and FIRs etc. The performance of systems is dependent on the performance of the multipliers because the multiplier is generally the slowest element in the system. Generally it is most area consuming. Hence optimization of speed and area of multiplier is a major design issue during the designing of the circuit. Vedic mathematics is the set of rules which deals with some mathematical formulae .Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krisna Tirth [1]after his research on Vedas .He has invented 16 sutras. Urdhva Tiryakbhayam is one among them which is more efficient. Urdhava Tiryakbhyam is a Sanskrit word which means vertical and crosswise in English

This paper is the extension of the previous work which tries to optimize the circuit proposed in the paper. It is organized as follows: Section two says about Literature survey, section third gives the basic knowledge of Reversible Logics. Section four explains the Urdhva Triyakbhayam algorithm. Section five describes the modification of the previous design in order to evolve the optimized design. Section sixth brings the result obtained from reversible multipliers. Section seventh draws a conclusion which claims the versatility of this Reversible Urthva Triyakbhayam Vedic multiplier.

2. Literature Survey

In 1960 Landauer said that circuit designed using irreversible logic results in energy or heat dissipation due to the loss of information [1].He proved that the loss of each one bit of information loss dissipates at least KTln2 joules of energy where K is the Boltzmann"s constant and T is the absolute temperature at which operation is performed [1].Theoretically reversible logic circuits have zero internal power dissipation because they do not lose information. In 1973 Bennett showed, to avoid KTln2 joules of energy dissipation in any circuit they must be used reversible logic gates [2]. In [5] the multiplier is designed using two units: one is the partial product generation unit by using Fred kin gate and Feynman gates and other part is summing unit constructed by using 4*4 TSG gates. A set of reversible gates are needed to design a reversible circuit. Some of the reversible gates are discussed [6]. [10] Presented a fault tolerant reversible 4x4 multiplier circuit. For construction of this circuit parity preserving FRG and MIG gates were used. Multiplier circuit was designed in two parts. In second part of circuit MIG gates were used instead of half adders and full adders.

3. Significance of Reversible Logic

3.1 Reversible Logic

A reversible logic gate is an n-input n-output logic device with one-to-one corresponding mapping. With the help of this logic gates the outputs are determine from the inputs and also the inputs can be uniquely recovered from the outputs. The fundamentals of reversible computing are based on the relationship between entropy and heat transfer between molecules in the system, the probability of a quantum particle occupying a particular state at any given time, and the

quantum electrodynamics between electrons when they are in close proximity

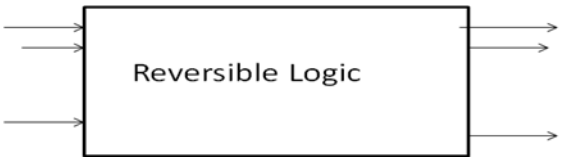


Figure 1: Reversible circuit

A reversible circuit should be designed using minimum number of reversible logic gates. There are many parameters which are used for determining the complexity and performance of the circuits for designing a reversible circuit are:

a) ***Number of Reversible gates (N):*** The total number of reversible gates used in the circuit
b) ***Constant inputs (CI):*** It is defined as the number of inputs that are to be maintained constant at either 1 or 0 in order to synthesize the given logical function.
c) ***Garbage outputs (GO***): It refers to the number of unused [4] outputs present in a reversible logic circuit. These are very essential to achieve reversibility so, it cannot be avoided.
d) **Quantum cost (QC):** It refers to the cost of the circuit in terms of the cost of a primitive gate.
e) ***Gate levels (GL)*:** This refers to the number of levels in the circuit which are required to realize the given logic functions

3.2 Basic Reversible Gate required

3.2.1. Feynman Gate

It is a 2×2 reversible gate .This gate is also known as Controlled Not (CNOT) gate. The Quantum cost of a Feynman gate is 1.This gate is generally used for Fan Out purposes.

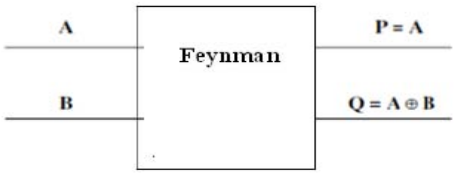


Figure 2: Feynman Gate

Table 1: Truth Table of Feynman gate

INPUT		OUTPUT	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

3.2.2. Peres Gate

It is a 3x3 gate and its logic circuit is as shown in the figure 3. The quantum cost of this gate is four. It is used to realize various Boolean functions such as AND, XOR

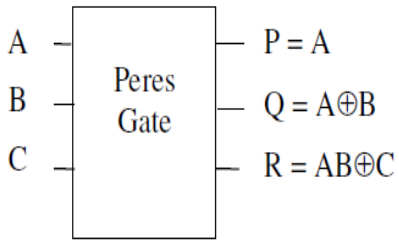


Figure 3: Peres Gate

Table 2: Truth Table for Peres Gate

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

3.2.3. Fred kin Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost of five. It can be used to implement a Multiplexer.

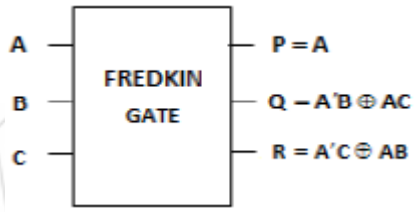


Figure 4: Fred kin Gate

3.2.4. HNG Gate

It is a 4x4 gate and its logic circuit is as shown in the below figure. The quantum cost of this gate is six. This gate is used to design a ripple carry adder. HNG [7] can produce both sum and carry in a single gate thus minimizes the garbage output and gate counts.

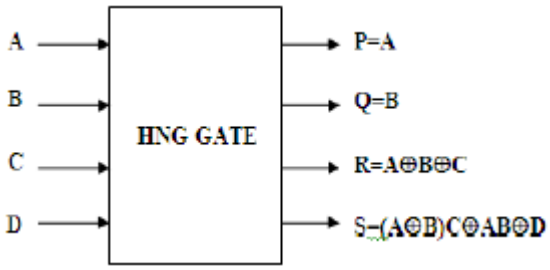


Figure 5: HNG Gate

Table 3: Truth Table of HNG gate

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	0

4. Multiplication Algo of Urdhva Triyakbhyam

Urdhva – Triyakbhyam is one of the 16 sutras which is applicable to all cases of multiplication such as Binary, Decimals and Hexadecimals. It means vertically and crosswise. It works on basis on the novel concept of all the partial products generated and then additions of these partial products are performed concurrently. The partial products generated in parallel and their summation is obtained using this formula. In other multipliers with increase in the number of bits of multiplicand or /and multiplier the time delay in computation of the product increases proportionally but this multiplier does not increases proportionately. Due to this fact time of computation is independent of clock frequencies of processors. Hence the clock frequency can be limited to a lower value. Since processor which uses lower clock frequency dissipate lower energy and it is economical in terms of power factor to use low frequency processors employing the fast algorithms. So by using Urdhva Tiryagbhyam Sutra in binary multiplication, the number of steps required to calculate the final product is reduced so computational time is reduced and increases the speed of the multiplier.

Algorithm: Fig. 6 represents the general multiplication procedure of the 4x4 multiplication.

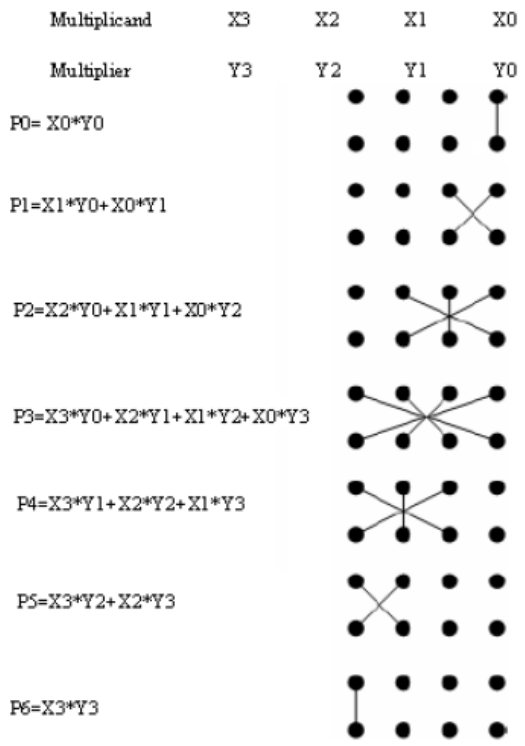


Figure 6: Multiplication procedure for 4X4 bit using "Urdhva-tiryakbyham " sutra

5. Optimization and Hardware Implementation of Urdhva Multiplier

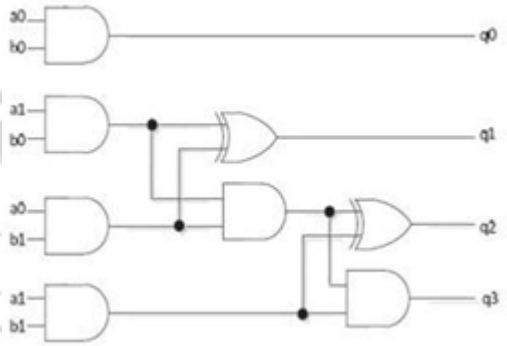


Figure 7: 2X2 UT Multiplier Using Reversible Logic Gate.

The 2 X 2 Urdhva Tiryakbhayam multiplier using conventional logic have four outputs. The logical expressions are given below

q0= a0 b0
ql= (a1.b0) xor (a0.bl)
q2= (a0.al.b0.bl) xor (al.bl)
and
q3= a0.al.b0.bl

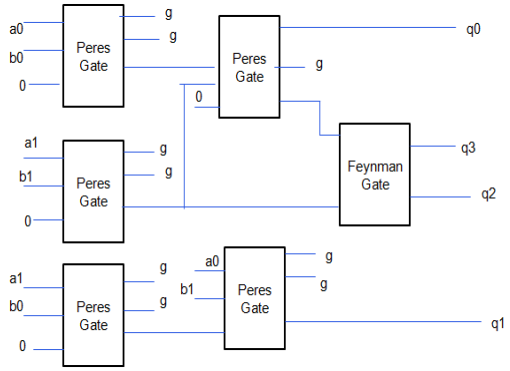


Figure 8: Implementation of 2*2 multiplier using Reversible gates

The reversible logic implementation of the above expressions require four Peres gates and one Feynman (CNOT) gate.

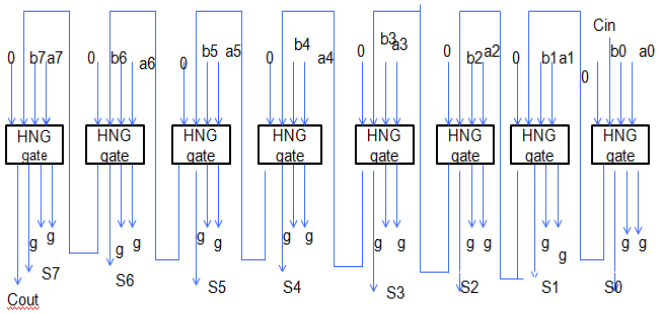


Figure 9: Eight Bit Ripple Carry Adder Using HNG Gate

The quantum cost of four bit adder unit using HNG gate is 24. The total number of garbage output is 8 and number of Constant Input is equal to 4.

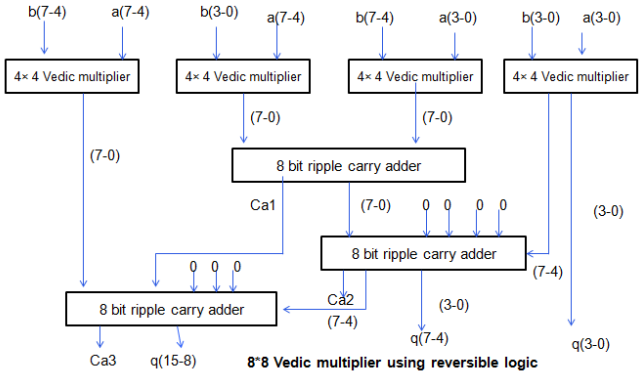


Figure 10: Shows 8 X 8 Urdhva Tiryakbhayam multiplier

The architecture of 8 X 8 Urdhva Tiryakbhayam multiplier circuits shown in the fig 11. It consist of four 4 X 4 UT multiplier unit and three 8 bit binary adders.

For Ex:

Consider two binary numbers A and B of 8 bits as shown below respectively

A = **A7A6A5A4** **A3A2A1A0**
(X1) (X0)

B = **B7B6B5B4** **B3B2B1B0**
(Y1) (Y0)

It can be showed as two four bit numbers each, i.e. A can be written as X1 X0 and B can be written as Y1 Y0 respectively, which is shown above, thus the multiplication can be showed as

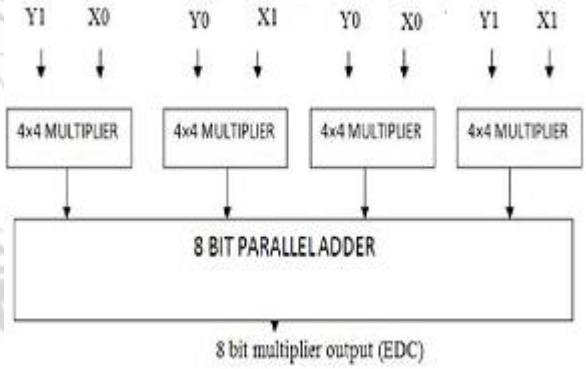
X1 X0
* Y1 Y0

EDC

Where, CP= C = X0Y0
CP= A = X1Y0
CP = B = X0Y1
CP= D = A+B
CP= E = X1Y1

Here CP= Cross Product

Thus, A*B= EDC, is achieved using Urdhava Triyakbhyam (Vertically and crosswise) sutra.



6. Results

The following figures 6.1 to 6.8 show the graphical representation of Top View, RTL schematic and wave form representation respectively. Maximum path delay in 4x4 and 8 x8 multipliers are 16.844ns and 27.31ns respectively. Estimated Power is calculated 0.052 watts for eight bit multipliers. This proposed design of the reversible 8x8 multiplier is logically verified using XILINX 13.2 and modelsim. The design is also implemented using Spartan 3E environment.

6.1 Top View

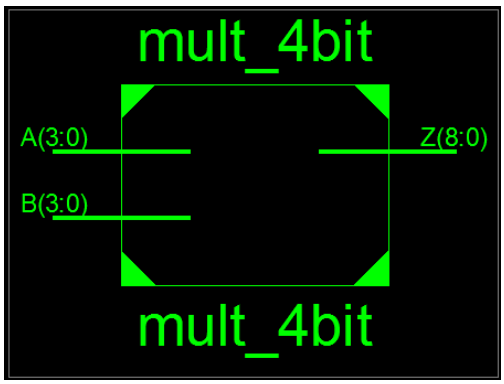


Figure 11: Top View of 4 X 4 UT Multiplier Using Reversible Logic Gates

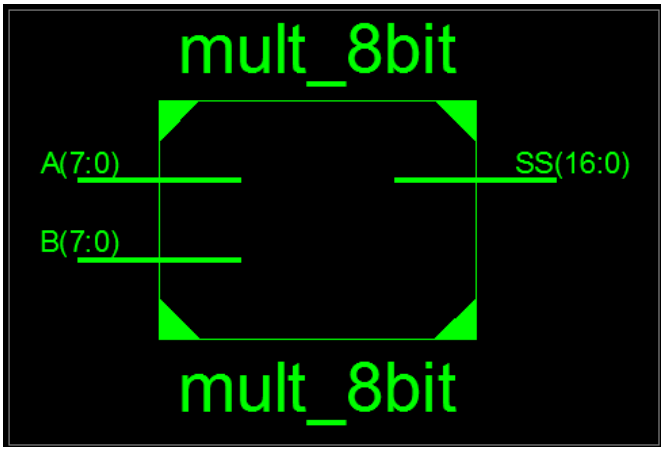


Figure 12: Top View of 8 X 8 UT Multiplier Using Reversible Logic Gates

6.2 RTL Schematic

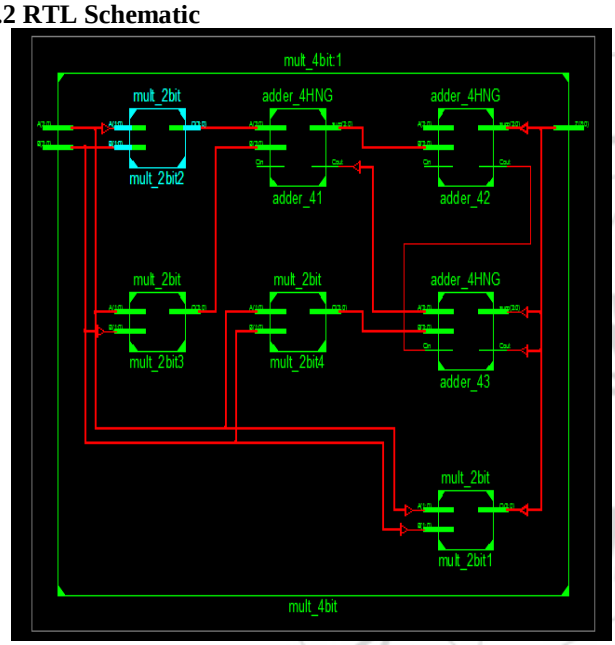


Figure 13: RTL Schematic of 4 X 4 Vedic Multiplier Using Reversible Logic Gates

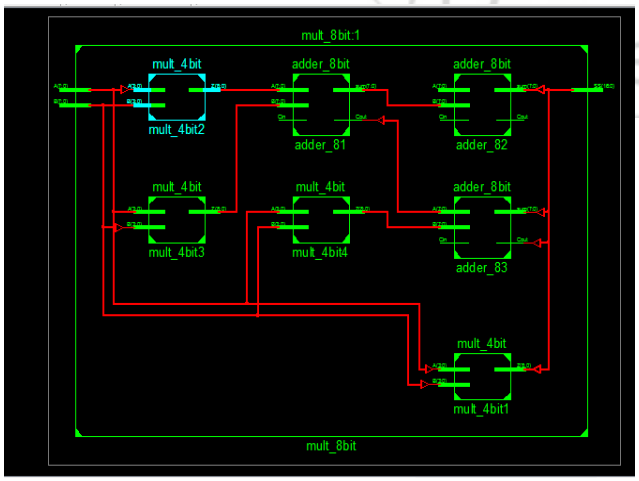


Figure 14: RTL Schematic of 8 X 8 Vedic Multiplier Using Reversible Logic Gates

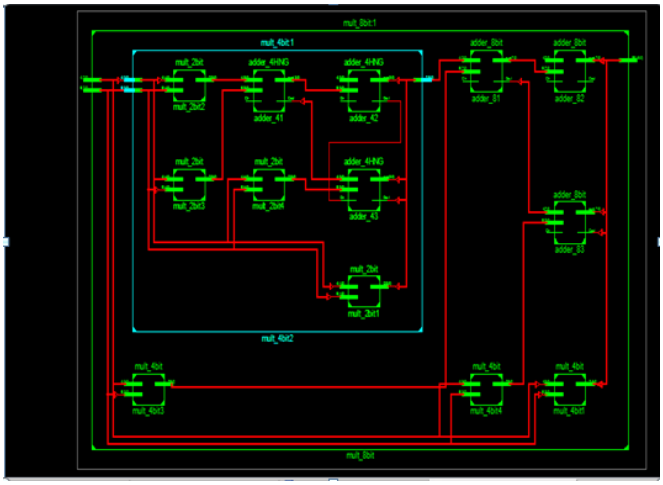


Figure 15: Expanded schematic of 8 X 8 Vedic Multiplier

6.3 Multiplication Output

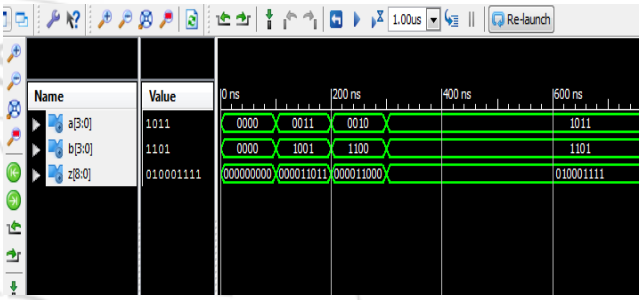


Figure 16: Multiplication Output of 4 X 4 Vedic Multiplier Using Reversible Logic Gates

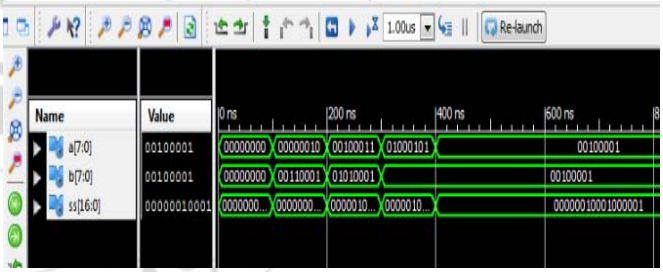


Figure 17: Multiplication Output of 8 X 8 Vedic Multiplier Using Reversible Logic Gates

6.4 Device Utilization Summary

Table 4 : Shows device utilization summary of 4 X 4 Vedic Multiplier Using Reversible Logic Gates

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	2	2448	0%
Number of 4 input LUTs	4	4896	0%
Number of bonded IOBs	8	66	12%

Table 5: Shows device utilization summary of 8 X 8 Vedic Multiplier Using Reversible Logic Gates

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	4	4,896	1%	
Number of occupied Slices	2	2,448	1%	
Number of Slices containing only related logic	2	2	100%	
Number of Slices containing unrelated logic	0	2	0%	
Total Number of 4 input LUTs	4	4,896	1%	
Number of bonded IOBs	8	66	12%	
Average Fanout of Non-Clock Nets	2.25			

7. Result Comparable

Table 6: Result of proposed multiplier

8 Bit Reversible Multiplier

Reversible multiplier	No of gates N	No of Constant inputs CI	No of Garbage outputs GO
Proposed	110	124	264

4 Bit Reversible Multipliers Comparision Table

Reversible multiplier	No of Gates N	No of Constant Inputs	No of Garbage Outputs
Proposed (FG,PG,HNG)	28	28	60
[3]	40	31	56
[4]	29	34	56

8. Conclusions

Reversible multiplier is to be designed with the help of different logical gates purposed in conventional Sequential and combinational logic whose aim is to improve the performance of the system. To improve the performance, the main factors in designing efficient reversible multipliers are: No of gates, No of garbage outputs, total quantum cost and total logical calculations. This Vedic multiplier is designed and implemented using Feynman Gate, Peres Gate and HNG gate. Firstly, 2*2 multiplier is designed using Feynman Gate, Peres Gate. 4*4 multiplier is designed using four 2*2 multiplier and three four bit ripple carry adders which is designed using HNG gate. And eight bit multiplier is designed using four 4*4 multiplier and three eight bit ripple carry adders. This multiplier design has high speed, less garbage output, minimum number of gate and less power.

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