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Effect of Pulse Width Modulation on the Performance of Hybrid Cascaded Five Level Inverter

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Abstract: ***For industrial applications medium power and medium voltage ac drives are more attractive. In order to reduce high dv/dt and to minimize the ripple in torque Multi Level Inverter (MLI)s are proposed. For the realization of Multi Level Inverters, different topologies have been emerging. Among these topologies, hybrid topologies are proven to be better than the conventional topologies. This paper compares the performance of a hybrid cascaded five level inverter with and without using the pulse width modulation technique. The frequency spectrum of the output voltage and currents are compared. For the simulation MATLAB software Simulink is used.***

Keywords: Pulse width modulation**,** Multi level inverters, hybrid topologies, MATLAB-Simulink**.**

1. Introduction

In industrial applications like adjustable speed drives, regulated power supplies, induction heating, inverters are more suitable to provide controlled voltage with desired frequency. However, the basic two level inverter provides an output voltage with more harmonic content and high dv/dt. In order to minimize these values, different harmonic reduction techniques are used. In the majority of inverters, commonly employed harmonic reduction methods are i) control strategies ii) multi level topologies[1] and iii) Pulse Width Modulation (PWM) techniques. The most frequently used topologies are neutral point clamped, capacitor clamped and cascaded H-bridge[2]. To reduce the losses, cost and weight hybrid topologies are introduced. In order to minimize the harmonics further, internal voltage control techniques like pulse width modulation methods are proposed. The modern inverter combines multilevel inverter topologies[3] with different pulse width modulation techniques for harmonic reduction to improve the performance of the inverter. In multi level inverters[4] the input voltage is divided into different levels using a series of static switches and/or capacitors[5].

The basic PWM techniques are classified into two types based on their switching frequency; they are i) fundamental frequency technique ii) High frequency switching technique. The former is used for selective harmonic elimination whereas the latter is carried either by using space vector or carrier based PWM techniques. Out of these, the simplest and cost-effective method is carrier based pulse width modulation technique[6]. In pulse width modulated technique, a sine wave called reference signal of fundamental frequency is compared with high frequency triangular wave form called carrier signal to generate the pulses for the switches in the inverter circuit. To change the output voltage, vary the magnitude of the reference signal called amplitude modulation index and to change the switching frequency vary the frequency of the carrier signal called frequency modulation index.

2. Operation of Hybrid Cascaded MLI

Hybrid topologies are the most modern arrangement of two conventional basic topologies connected in cascade[7] to get the desired levels in the output voltage. The significant characteristic of the projected multilevel inverter topology is the decrease in the number of elements per phase, hence as a result reducing the power loss, cost and size. The arrangement of Hybrid cascaded MLI for five level[8] output is shown in the figure 1. The base inverter is of an ordinary 3-leg inverter with a dc power source is cascaded with a H-bridge[9] [10] standard inverter topology. The H-bridge can use a capacitor or battery or any other dc power source.

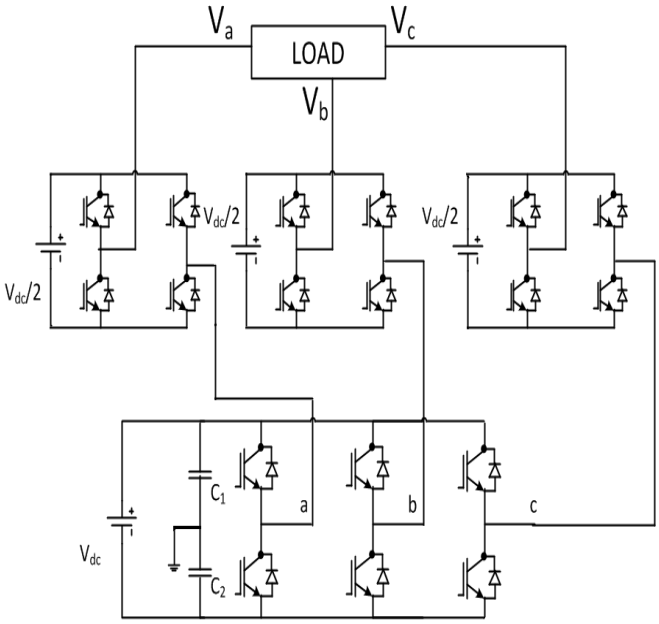

Figure 1: 3-ϕ configuration of hybrid cascaded MLI

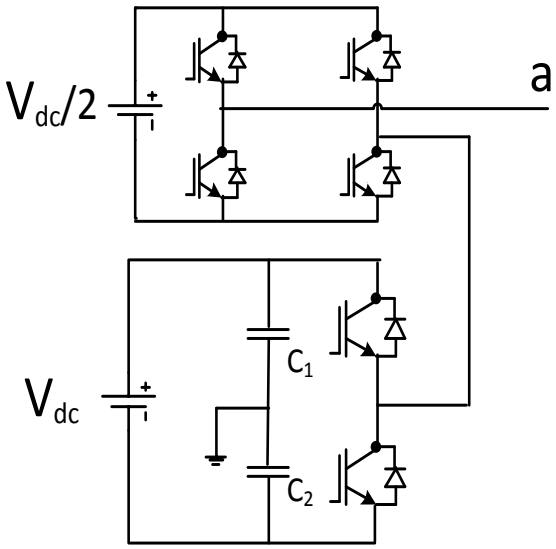

Figure 2: 1-ϕ configuration of hybrid cascaded MLI

The single phase circuit representation of Hybrid cascaded MLI is shown in figure 2. The load is connected between a particular line to the neutral point. There are six switch states to produce different levels in the output voltage across the load. The sequence of the switches operating to provide different voltage levels is clearly mentioned in the table 1. The five voltage levels are V,V/2,0,-V/2 and V.

Table 1: Switching states for Hybrid cascaded MLI

Voltage levels	Switching States					
	T_1	T_4	S_{R1}	S_{R2}	S_{R3}	S_{R4}
$+V_{dc}$	1	0	0	0	1	1
$+V_{dc}/2$	1	0	1	0	1	0
0	1	0	1	1	0	0
	0	1	0	0	1	1
$-V_{dc}/2$	0	1	1	0	1	0
$-V_{dc}$	0	1	1	1	0	0

To provide an output voltage V_{dc} turn ON the switches T_1, S_{R3} and S_{R4}. To obtain output voltage $V_{dc}/2$ turn OFF S_{R4} and turn ON $S_{R1}$by keeping T_1 and S_{R3} in ON state. To make the output voltage zero, turn OFF S_{R3} and turn ON S_{R2} keeping T_1 and S_{R1} in ON state(or use the complement of this combination). To bring the out voltage to $V_{dc}/2$, turn ON T_4, S_{R1} and S_{R3}. To decrease the output to –V, switch OFF S_{R3} and switch ON S_{R2}.

3. MATLAB Simulink model of Hybrid 5-level MLI

The MATLAB-Simulink simulation diagram is shown in figure 3. The design of control circuit for the five level hybrid multi level inverter is given in figure4. The figure 5 depicts the driver circuit output signals to generate a five level output voltage without using pulse width modulation technique, where the switches T_1 and T_4 are complementary to each other. Whereas S_{R1} & S_{R4}, S_{R2} & S_{R3} are complementary to each other.

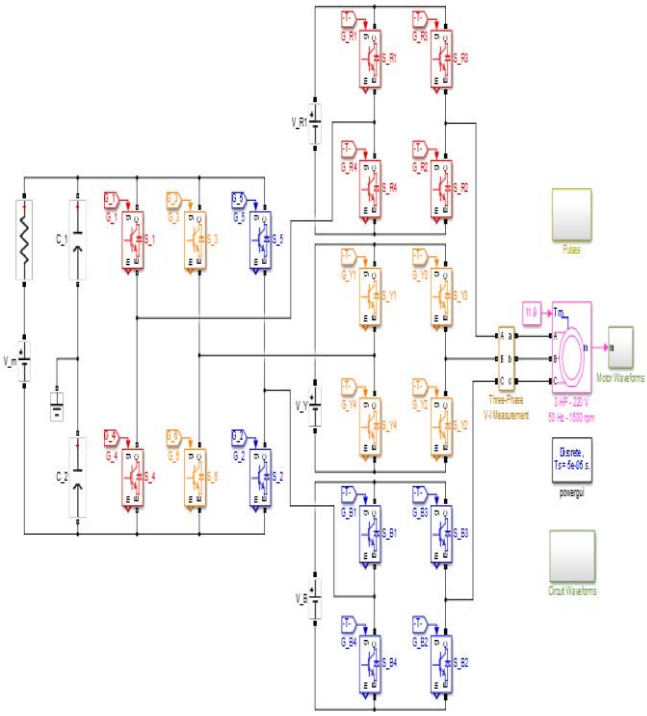

Figure 3: Simulink diagram of Hybrid cascaded MLI

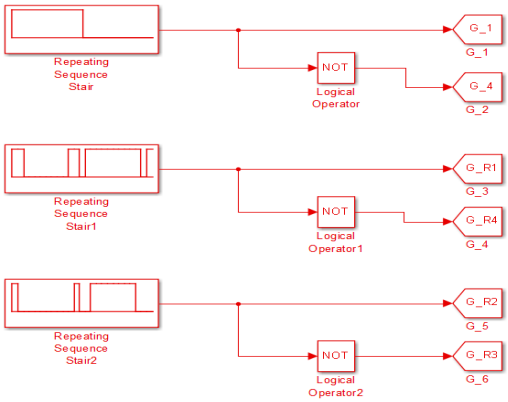

Figure 4: Control circuit without using PWM.

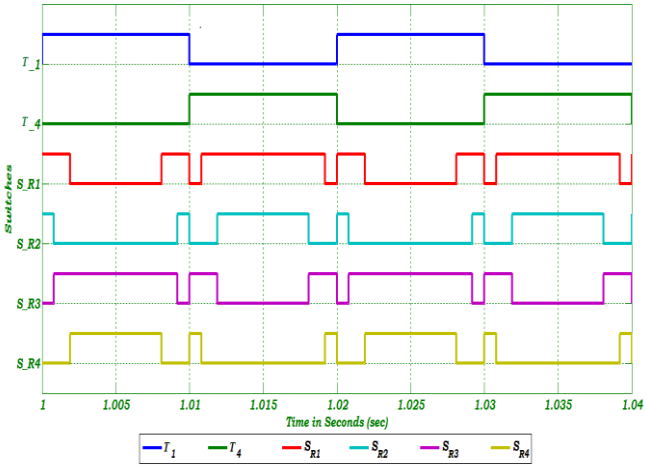

Figure 5: Control circuit output without using PWM.

4. Pulse Width Modulation

The design of pulse width modulated signal for the hybrid cascaded five level inverter is shown in below figure 6, where a sine wave is compared with the triangular carrier signal to generate the desired output. The corresponding pulses are shown in figure 7.

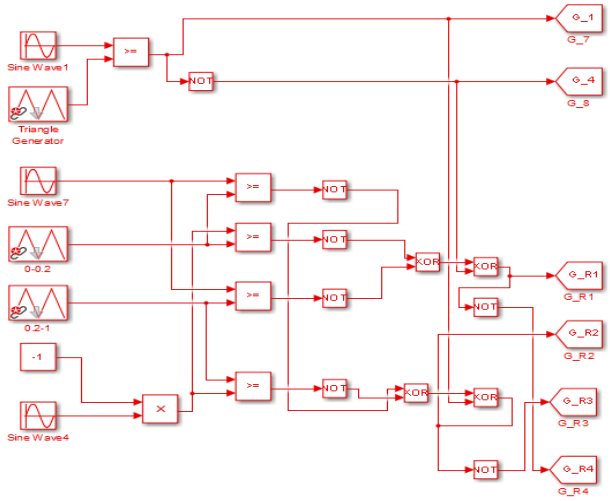

Figure 6: Logic circuit to generate PWM signals

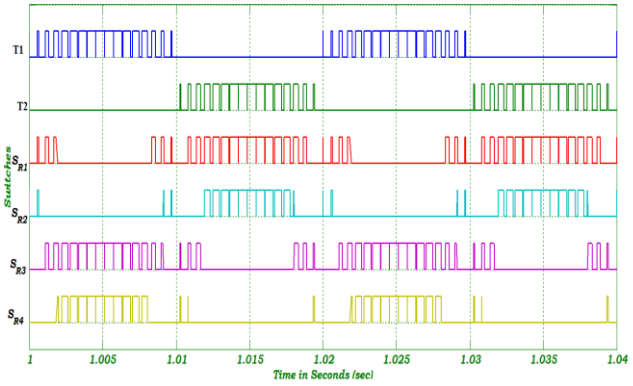

Figure 7: PWM pulses from the driver circuit

5. Results

The Hybrid cascaded multilevel is modeled using MATLAB Simulink environment. IGBTs are taken as switching elements. The frequency modulation index is chosen as 20. A 3 HP, 220V, 50 Hz, 1725 rpm squirrel cage induction motor is considered as load. The input torque applied is 11.9 Nm. The figure 8 and 9 represents the output phase voltage and its frequency spectrum without applying pulse width modulation. The output line voltage and its frequency spectrum are shown in figures 10 and 11 respectively. The corresponding load current and total harmonic distortions are depicted in figures 12 and 13.

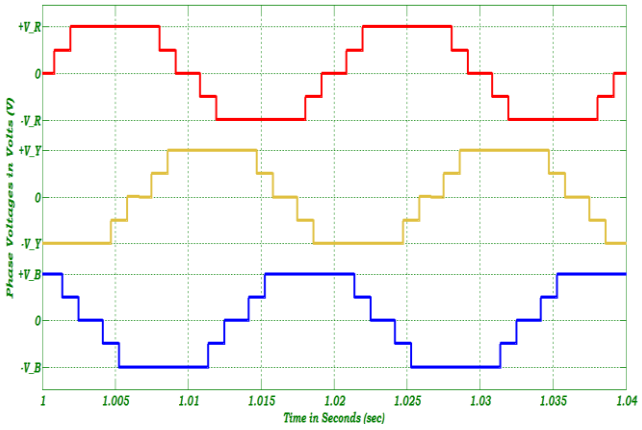

Figure 8: Output phase voltages without PWM

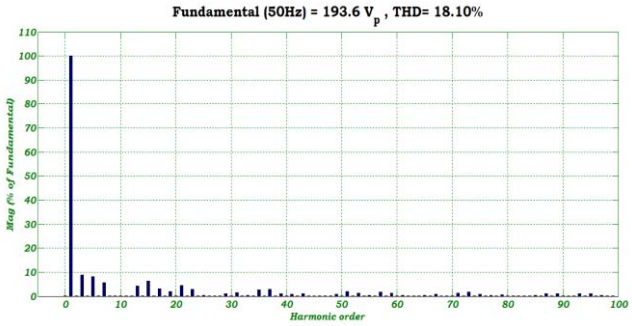

Figure 9: Frequency spectrum of phase voltage without PWM

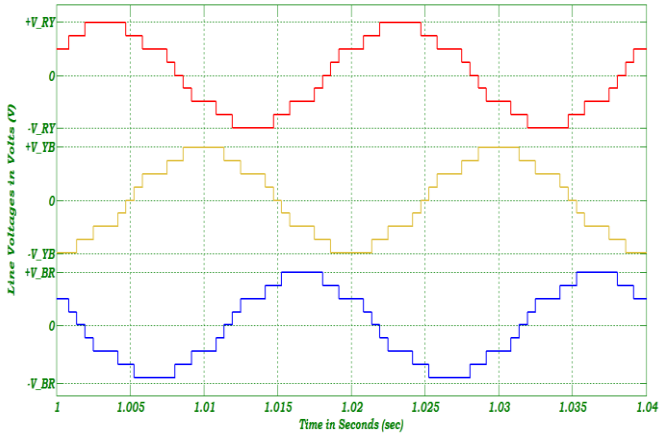

Figure 10: Output line to line voltage without PWM

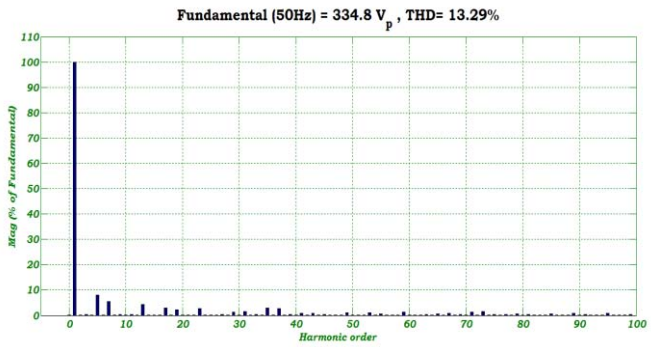

Figure 11: Frequency spectrum of line to line voltage without PWM

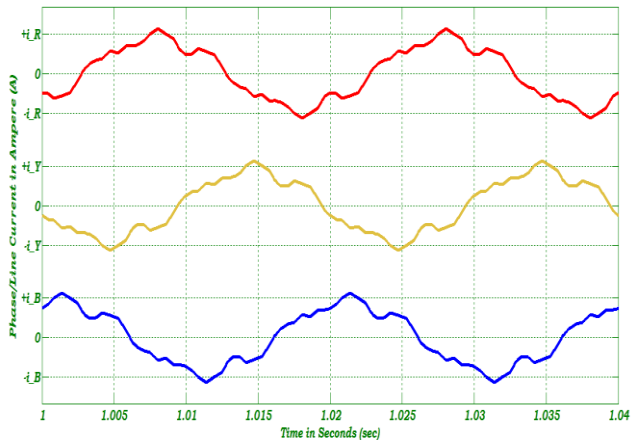

Figure 12: Line currents without PWM

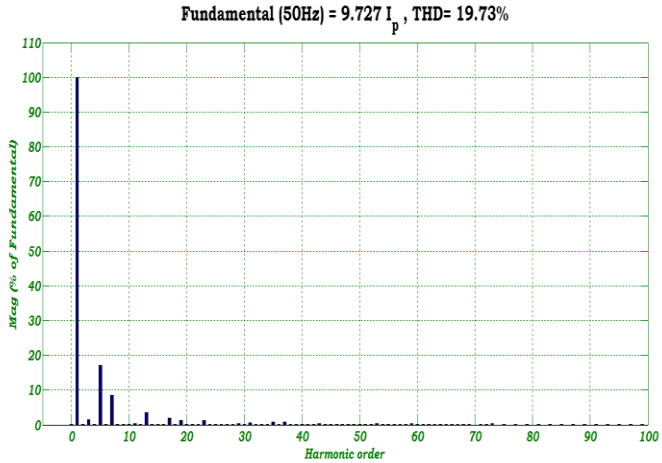

Figure 13: Frequency spectrum of line current without PWM

The output phase voltage and its frequency spectrum are shown in figures 14 and 15 respectively. From these figures it is observed that with pulse width modulation the fundamental component of phase voltage is decreased. The output line to line voltage and its fast Fourier transform is given in figures 16 and 17. It can be observed that the peak value of the fundamental component of line voltage also gets reduced.

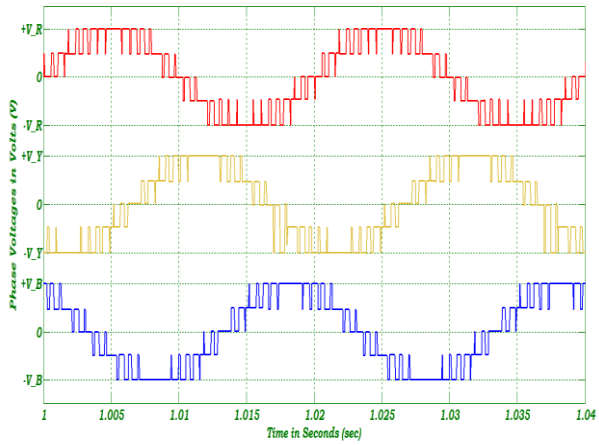

Figure 14: Output phase voltage with PWM

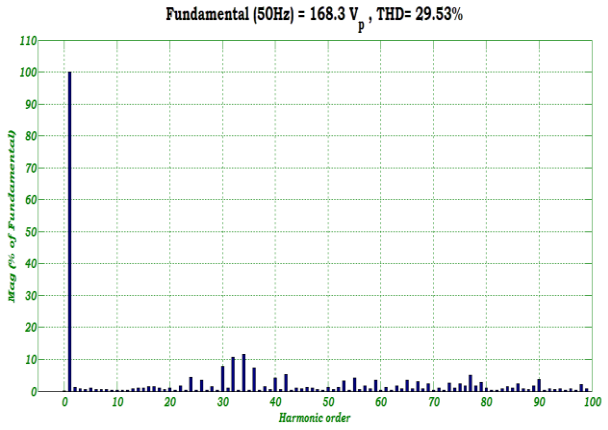

Figure 15: Frequency spectrum of phase voltage with PWM

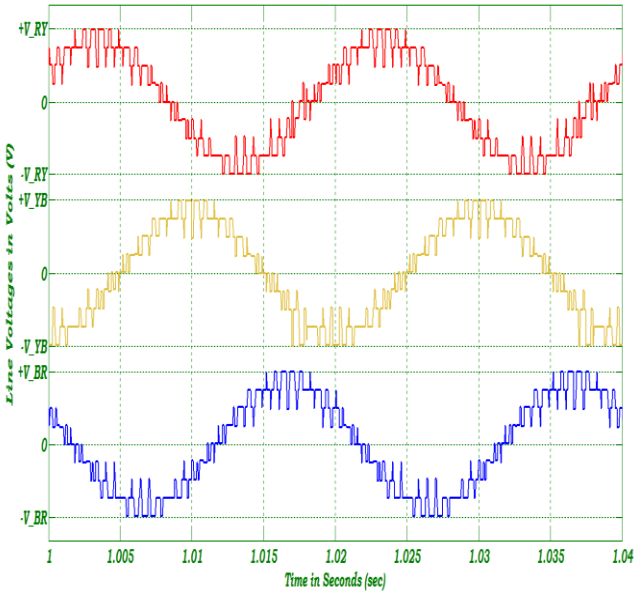

Figure 16: Output line to line voltage with PWM

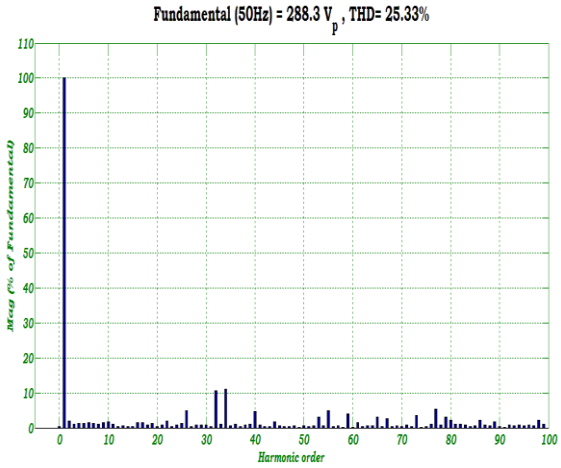

Figure 17: Frequency spectrum of line voltage with PWM

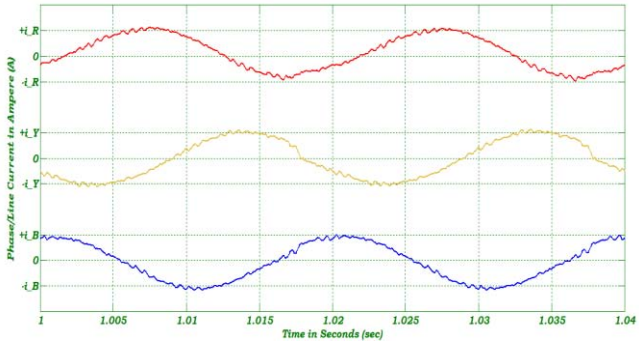

Figure 18: Line currents with PWM

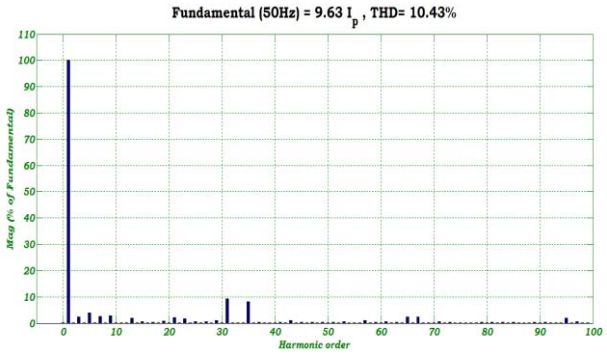

Figure 19: Frequency spectrum of line current with PWM

The line current waveform and its frequency spectrum are shown in figures 19 and 19 respectively. All these observations are tabulated in table2.

Table 2

	Voltage Levels	
	Without PWM	With PWM
Fundamental Peak Phase Voltage	193.6	168.3
THD	18.10%	29.53%
Fundamental Peak Line Voltage	334.8	288.3
THD	13.29%	25.3%
Fundamental Peak Current	9.727	9.63
THD	19.73%	10.43%

6. Conclusion

The topology of Hybrid cascaded inverter utilizes less number of elements per phase for its design. From the above result it can be concluded that the conventional sinusoidal pulse width modulation technique will reduce the fundamental components of phase and line voltages. In the other words it will increases the harmonic content in the phase and line voltages. But the harmonic components in the line currents are reduced. The harmonics in the output phase and line voltages can be minimized with suitable change in the reference signal from conventional sinusoidal to any other reference signal.

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Author Profile

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