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Harmonics Elimination in Cascaded Multilevel Inverter Using PWM Method

Vaisakh .T

Post Graduate, Power Electronics and Drives

Abstract: ***In this project, a multilevel inverter was designed and implemented to operate a stand-alone solar photovoltaic system. The proposed system uses selective harmonics elimination pulse-width modulation (PWM) in the multilevel inverter to convert DC voltage from battery storage to supply AC loads. In the PWM method, the effectiveness of eliminating low-order harmonics in the inverter output voltage is studied and compared to that of the sinusoidal PWM method. This work also uses SHEPWM to predict the optimum modulation index and switching angels required for a nine-level cascaded H-bridge inverter with improved inverter output voltage. The proposed predictive method is more convincing than other techniques in providing all possible solutions with any random initial guess and for any number of levels of a multilevel inverter. The simulation results prove that the lower-order harmonics are eliminated using the optimum modulation index and switching angels. An experimental system was implemented to demonstrate the effectiveness of the proposed system.***

Keywords: SHEPWM, Redundant states, Self-balancing

1. Introduction

In recent years, environmental concerns the depletion of fossil fuel reserves have spurred significant interest in renewable energy sources. Interconnecting these intermittent sources to the utility grid on a large scale it affect the voltage/frequency control of the grid and lead to severe power quality issue. Multilevel inverter has been attracting extensive attention from as well as industry in the recent decade [1]. They have emerged as the solution too many problems related to the traditional two-level inverter. The principal advantage is to generate a good waveform quality reducing the voltage stresses on power semiconductor devices. So, they are very useful in high power ac applications. Several multilevel-PWM methods are developed for the two-level inverter and expanded to the multiple levels. The most popular are the multilevel carrier-based PWM derivatives. However, these techniques offer good performances using high switching frequency [2]. The SHEPWM-based method can theoretically provide various performance advantages over all the PWM methods. These advantages include, produced the desired fundamental sinusoidal voltage while at the same time certain order harmonics are eliminated [3]. Otherwise, the use of this kind of inverter poses the dc-link capacitor unbalance problem. Two main approaches have been proposed. 1) The use of additional passive and/or active components. 2) The manipulation of the redundant switching states. The first solution causes an increase of system cost and additional power losses. For the second one, it is generally used in the space vector PWM. In fact, this paper shows that the redundant states can be associated to the selective harmonic elimination PWM in order to improve more and more the performance system in term of quality signal and power losses. In order to reduce energy loss in transmission lines and increase the overall battery capacity, the battery bank is series connected for a high-voltage dc power supply[2]-[8].

2. Selective Harmonic Elimination

This is also termed as the optimized PWM technique. By reversing the phase voltages a few times during each half cycle, it is possible to eliminate lower order harmonics selectively. However, the higher order harmonics may increase in magnitudes, but the current harmonics are not significantly affected due to low pass filter characteristics of the AC system. The voltage reversals are affected at chosen instants such that the notches (caused by the voltage reversals) are placed symmetrically about the centre line of each half cycle. If there are „p" switching (voltage reversals) in a quarter cycle, the rms value of the nth harmonic voltage is given by,

$$E_n = \pm\frac{0.45}{n} V_{dc}[2(cosn\,\propto_1 - cosn\,\propto_2 + cosn\,\propto_3 \ldots..) - 1] \quad (1)$$

Where $\propto_1, \propto_2 \ldots.. \propto_n$ are switching angles within each quarter cycle. There are p degrees of freedom and are used to cancel (p-1) harmonic components in the voltage and control the fundamental voltage. For example, if there are 3 switching at $\propto_1, \propto_2 \; and \; \propto_3$, we can eliminate the fifth and seventh harmonics in addition to control the fundamental voltage. We get 3 transcendental equations is given by,

$$m = 2[cos\alpha_1 - cos\alpha_2 + cos\alpha_3] - 1 \quad (2)$$

$$0 = 2[cos5\,\propto_1 - cos5\,\propto_2 + cos5\alpha_3] - 1 \quad (3)$$

$$0 = 2[cos7\,\propto_1 - cos\propto 7\,\propto_2 + cos7\,\propto_3] - 1 \quad (4)$$

Note that although the phase voltage contains triple harmonics, the line to line voltages are free from them [7]-[8].

3. Simulation Circuit Diagram

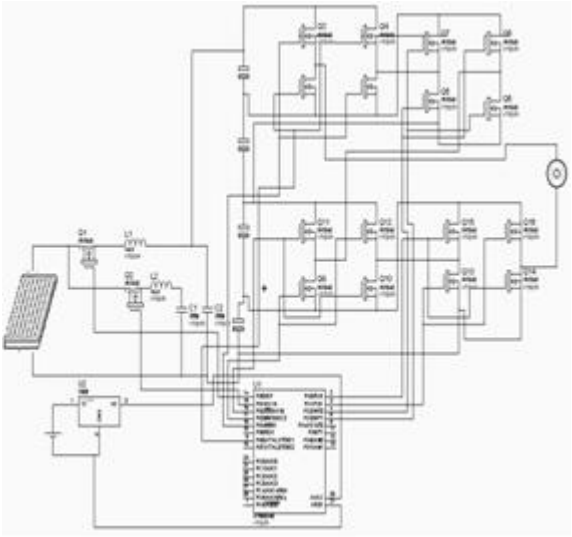

Figure 1: Circuit Diagram

Operation of Circuit Diagram

In order to keep the four voltages equal, we will make use of the switch states of the 9-level inverter. Three groups are distinguished from 125 switch states. The first one is formed by 24 vectors which do not connect any of the phases to the common capacitors potential and so the capacitor voltages remains unaffected. The second group has 36 vectors with multiple switch states. The last one is the vector zero with five different switch states. They have any effect on the DC-link voltages. So, only the second group will be used to ensure the capacitor voltages balance. Different switch states force load current to flow through different paths. Thus the direction of current through the DC-link capacitors is different and variation of capacitor voltages is minimizing the difference between the voltages of the four capacitors by selecting the suitable redundancy among the different. We express the capacitor currents by the two *ac* load current i_a and i_b .

According to their sign, we can know the effect of each state on the capacitor behavior (charge or discharge). voltage vectors of group 2. The switch state selected has to unload the most loaded capacitor voltage and load the unloaded one. Therefore, capacitor voltage derivations have to be considered. Substitute the modulation 1 1 4 by the first redundancy (0 0 3) which allows charging C_1 and discharging C_4. In the contrariwise, we let the initial state. The same operation is done using the PWM signal given by the SHE technique at the end; we obtain another leg voltage waveform which provides the same modulation voltage waveform and the same harmonics spectrum. The proposed capacitor balancing method has been assessed by simulation.

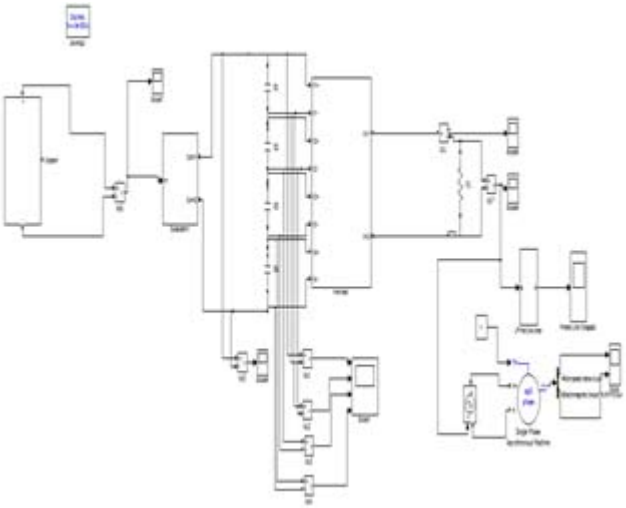

Figure 2: Simulation circuit for 9-level Cascaded Inverter

4. Simulation Results

The proposed nine-level inverter circuit has been tested on a 230V, 50Hz, induction motor drive with *V/f* control scheme at a switching frequency of 1 kHz. This simulation diagram is drawn in MATLAB Software package. In this diagram, MOSFET Switches are connected in structure of cascaded with H-bridge. SHEPWM technique is used in this project for controlling the inverter by giving gate pulse to MOSFET Switches. The inverter dc-link voltage is set to 230 V. The hysteresis limit for the capacitor is set at 5% of the respective capacitor voltage. The capacitors are sized suitably so that the voltage of the capacitors would not cross the hysteresis limit in two switching cycles at full load current. Simulation circuit for nine-level in switching angles is calculated by give the firing pulses to the nine level inverter, the staircase voltage waveform is obtained. The FFT analysis is done in both the cases. The THD calculated in case of resistive load is 14.49% while in case of RL load is further reduced to 3.08%. The calculation revealed that 3rd, 5th and 7th harmonics is significantly reduced up to four decimal places and thus overall THD% is reduced. A full-bridge inverter or so-called H-bridge cell is introduced. Basically, an H bridge cell can generate up to three output voltage levels. The appropriate gate control signal and blinking time are presented. Multilevel inverter using cascaded-inverter with SDCSs is introduced in both single-phase and three-phase structure. The output voltage is the sum of the output voltage of each H-bridge cell. In three-phase system, the voltage THD can be improved in line voltage. Finally, the reason to use SDCSs is explained the concept of the optimized harmonic stepped-waveform technique will be presented.

4.1 Output Voltage Waveform

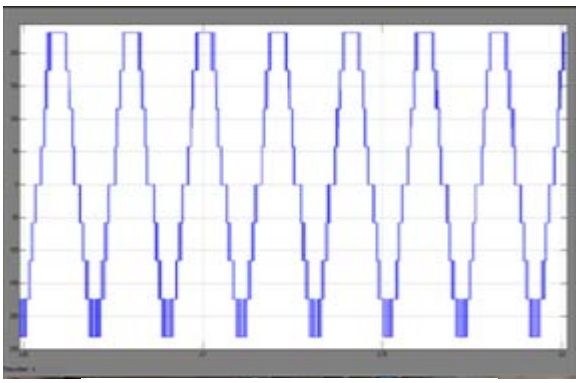

Figure 4.1: Output Voltage Waveform

4.2 Output Current Waveform

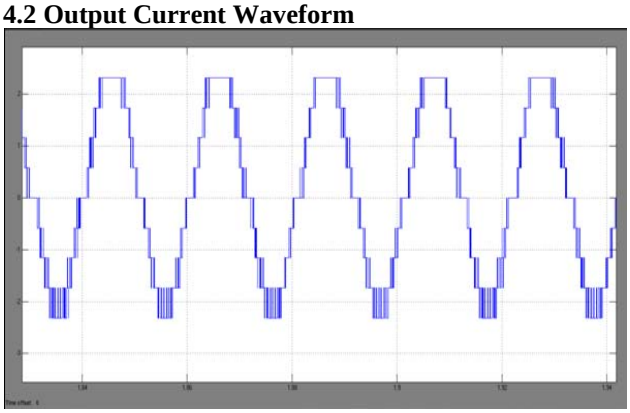

Figure 4.2: Output Current Waveform

4.3 Filtered Output Voltage

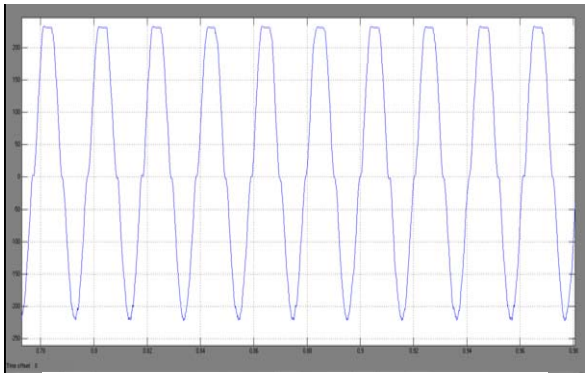

Figure 4.3: Filtered Output Voltage Waveform

4.4 THD Analysis of Output Voltage

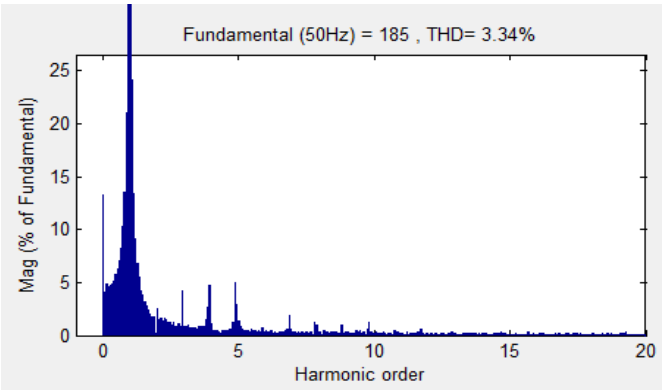

Figure 4.4: THD Analysis of Output Voltage

In this project, modulation index is 0.8 is used in pulse generator. The gate pulses are given to inverter through the subsystem. From subsystem the pulses are given to Goto and then Goto are linked with from blocks then pulses given to switches. Then output current and output voltage is determined from the simulation results.

5. Conclusion

Both optimization of switching angles of nine-level output waveform using SHEPWM and DC-link voltages balance are investigated in this study. The programmed PWM allows eliminating harmonics row 5, 7 and 9th orders with a good control of the fundamental voltage. In order to keep as well as possible the four capacitor voltages equal, we have made use the 61 switch states of the nine-level inverter. Its matrix representation simplify the redundant states analyse.

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