Comparison of DPC methods Using Two-Level and Three-Level Rectifiers

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Abstract: *This paper contains the evaluation and comparison between DPC methods for two-level (2-L) and three-level (3-L) AC/DC converters, in order to demonstrate de great advantages of using a three level rectifier type NPC. The theoretical principal of this methods as well as the synthesis of the active and reactive power are discussed. The regulation of DC-bus voltage is achieved using PI controller. The effectiveness of this approach is shown by simulation results using Power System Bloc set (PSB) of Matlab/Simulink.*

Keywords: Direct Power Control, two-level rectifier, three-level rectifier, instantaneous active and reactive power, switching table, corrector PI.

1. Introduction

In recent years, the trend of positively using PWM rectifier, as the dc power supplies for voltage-source inverters has been increasing [1,3]. The voltage-source PWM rectifier-inverter has the following advantages: harmonics in input-output waveforms are fewer, input power factor can be controlled to be unity, generation is possible and the capacity of dc capacitor can be reduced etc.., the PWM rectifiers have more and more application such as active power filter (APF), unified power flow control (UPFC) and so on [1,2]. In the recent years, the research interest in three-phase PWM rectifiers is mainly influenced by the update of the control technology with the aim to: [3]

1) Ensure that the ac terminal current THD is less than 5% of the total fluctuation load to reduce the adverse effect on the grid.
2) Guarantee the power factor close to one and regard the rectifier as a „pure resistive load" in terms of the grid;
3) Improve the dynamic characteristic for dc-bus voltage regulation, and reduce the dynamic response time, etc. [4, 5].

The high-performance control strategies of PWM rectifiers are mainly the voltage oriented control (VOC) [6] and direct power control (DPC) [7], which are similar to the vector control (VC) and direct torque control (DTC) [8] for AC machines. The VOC control scheme guarantees high dynamic and static performance via internal current control loops. However, the final configuration and performance of the VOC system largely depends on the quality of the applied current control strategy. With DPC there are not internal current control loops and no PWM modulator bloc, because the converter switching states are selected by a switching table based on the instantaneous errors between the commanded and estimated values of the active and reactive power, and voltage position vector. Therefore, the key point of the DPC implementation is a correct and fast estimation of the active and the reactive line power.

On the other hand, multi-level inverters have become a very attractive solution for high power application areas [9-10].

The three-level Neutral Point Clamped (NPC) inverter is one of the most commonly used multi-level inverter topologies in high power ac drives. By comparing to the standard two-level inverter, the three-level inverter presents its superiority in terms of lower stress across the semiconductors, lower voltage distortion, less harmonic content and lower switching frequency [11].

The three level inverters present a big interest in the field of the high voltages and the high powers of the fact that they introduce less distortion and weak losses with relatively low switching frequency [12]. This paper presents a brief description and comparison of DPC methods of vector control using two and three-level AC/DC converters, and to demonstrate the great advantages of using three level converters type NPC. The regulation dc-bus output is realized by corrector PI.

2. DPC with Two Level Rectifier

DPC block for PWM converter essentially comprises of active and reactive power comparators, power estimators and switching pattern generator. The DPC application in PWM converter is analogous to direct torque control (DTC) in inverter fed three-phase motor drives. Initially, DTC and DPC strategies had been implemented with look-up table based switching pattern generator.

### 2.1 The principle and modeling of the two level rectifier

The topology of three phase bidirectional voltage-source PWM rectifier (VSR) is shown in fig. 1. The VSR is connected to the three phase as source via smoothing L and internal resistance R. The inductance act as a line filter for smoothing the line currents with minimum ripples. Insulated gate bipolar transistors (IGBTs) are used as the VSR power switches since IGBTs have features of high power rating, simple gate drives requirement and suitable for high frequency switching applications. It is assumed that a pure resistive load R_L is connected at the dc-link capacitor C. [13] By assuming a balance three-phase and three wires system, the voltage equations of the PWM rectifier can be described by equation (1)-(3).

$$\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} = R \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \qquad (1)$$

$$C \frac{dV_{dc}}{dt} = S_a i_a + S_b i_b + S_c i_c - i_{dc} \qquad (2)$$

Where $S_{a,b,c}$ is switching state of the converter. The phase voltages at the poles of the converter are equal to:

$$v_a = (2S_a - (S_b + S_c)/3).V_{dc}$$
$$v_b = (2S_b - (S_a + S_c)/3).V_{dc} \qquad (3)$$
$$v_c = (2S_c - (S_b + S_a)/3).V_{dc}$$
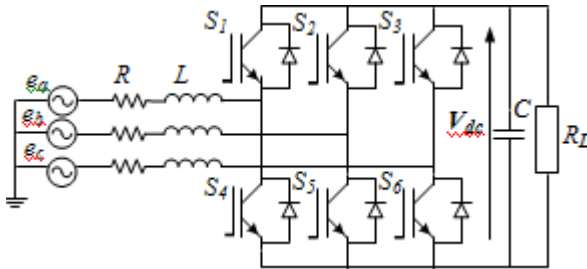
Figure 1: Configuration of three phase VSR

## 2.2 Direct Power Control Strategy (2-Level)

In this configuration, the dc-bus voltage is regulated by controlling the active power, and unity power factor operation is achieved by controlled the reactive power to be zero [13]. As shown in fig. 2, the active power command is provided from a dc-bus voltage control block, while the reactive power command is directly given from the outside of the controller. Errors between the commands and the estimated feedback power are input to the hysteresis comparators and digitized to the signals Sp and Sq. Also, the phase of the power-source voltage vector is converted to the digitized signal θ_n. For this purpose, the stationary coordinates are divided into 12 sectors, as shown in Fig. 3, and the sectors can be numerically expressed as:

$$(n-2)\frac{\pi}{6} \leq \theta_n \leq (n-1)\frac{\pi}{6} \quad n = 1, 2, ..., 12 \qquad (4)$$

By using several comparators, it is possible to specify the sector where the voltage vector exists.
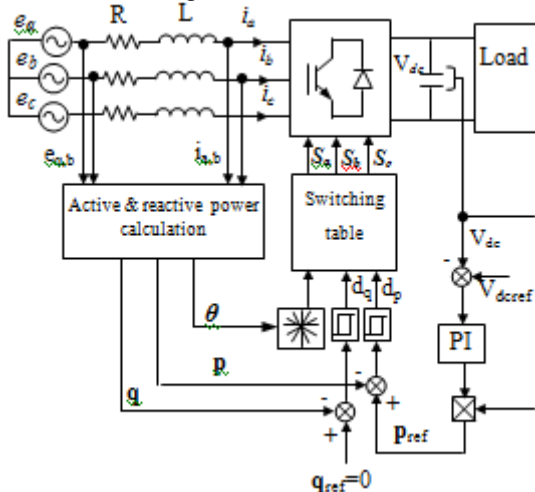
Figure 2: Configuration of direct instantaneous active and reactive power controller
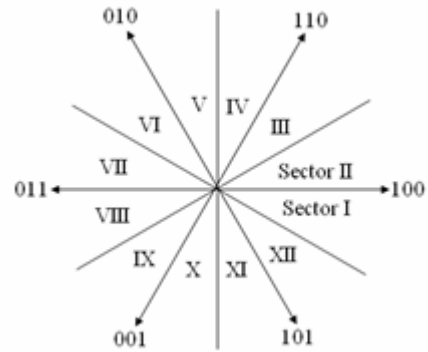
Figure 3: Twelve sector on stationary coordinates to specify voltage vector phase

It is known that the calculation of the active power P is a scalar product between the voltages and the currents, whereas the reactive power q can be calculated by a vector product between them [11]-[13].

$$p = v_a i_a + v_b i_b + v_c i_c \qquad (5)$$

$$q = \frac{1}{\sqrt{3}}\left[(v_b - v_c)i_a + (v_c - v_a)i_b + (v_a - v_b)i_c\right] \qquad (6)$$

In terms of the switching states of the converter, the three phase line currents, the dc-bus voltage, and the inductance of the reactors, the estimated values of p and q and can be derived as:

$$\hat{p} = L\left(\frac{di_a}{dt}i_a + \frac{di_b}{dt}i_b + \frac{di_c}{dt}i_c\right) + V_{dc}(S_a i_a + S_b i_b + S_c i_c) \qquad (7)$$

$$\hat{q} = \sqrt{3}L\left(\frac{di_a}{dt}i_c - \frac{di_c}{dt}i_a\right)$$
$$- \frac{1}{\sqrt{3}}V_{dc}\left[(S_a(i_b - i_c) + S_b(i_b - i_a) + S_c(i_a - i_b)\right] \qquad (8)$$

The digitized error signals and digitized voltage phase are input to the switching table in which every switching state dp and dq of the converter is stored, as shown in Table I.

By using this switching table, the optimum switching state of the converter can be selected uniquely in every specific moment according to the combination of the digitized input signals. The selection of the optimum switching state is performed so that the power errors can be restricted within the hysteresis bands.

Table 1: Conventional Switching Table For Direct Instantaneous Power Control

| d_p	d_q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
1	1	7	7	0	0	7	7	0	0	7	7	0	0
1	0	6	7	1	0	2	7	0	3	7	4	0	5
0	1	1	2	2	3	3	4	4	5	5	6	6	1
0	0	6	1	1	2	2	3	3	4	4	5	5	6

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3. DPC with Three Level Rectifier

3.1 Three-Level NPC Rectifier

In the Neutral-Point Clamped inverter presented in fig. 4, the converter is built around twelve switching cells (based on IGBT, or others) and six clamp diodes; each phase can produce three distinct levels by connecting the output either to the positive ($V_{dc}/2$), negative (-$V_{dc}/2$) or null (0) potential. In a three system it results in $3^3=27$ output voltage vectors, related to 19 possible voltage vectors at the output of the converter (fig. 5, and Table II).
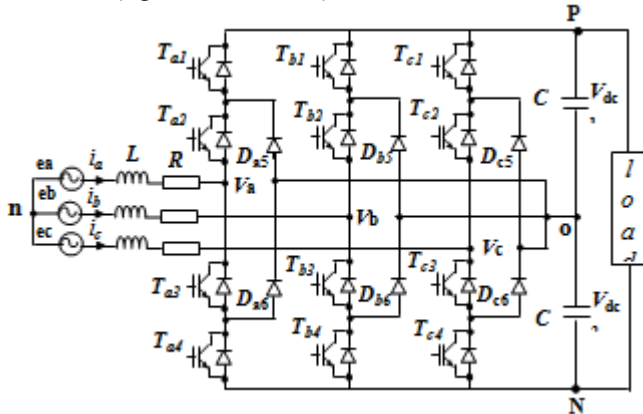
Figure 4: Schematic diagram of a three-level NPC rectifier

The output voltage space vector V_i corresponding to the 19 different vectors can be classified into four categories according to its magnitude; it can be summarized in the Table II.
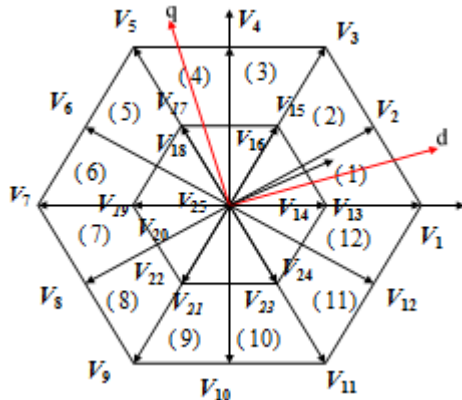
igure 5: Space vector diagram of three-level inverter.

Table 2: Voltage Space Vectors Generated By The Three-Level Npc Inverter

Zeros Voltages	V_{25} (0,0,0)	V_{26} (1,1,1)	V_{27} (-1,-1,-1)			
Half Voltages	V_{13} (1,0,0)	V_{15} (1,1,0)	V_{17} (0,1,0)	V_{19} (0,1,1)	V_{21} (0,0,1)	V_{23} (1,0,1)
	V_{14} (0,-1,-1)	V_{16} (0,0,-1)	V_{18} (-1,0,-1)	V_{20} (-1,0,0)	V_{22} (-1,-1,0)	V_{24} (0,-1,0)
Full Voltages	V_1 (1,-1,-1)	V_3 (1,1,-1)	V_5 (-1,1,-1)	V_7 (-1,1,1)	V_9 (-1,-1,1)	V_{11} (1,-1,1)
Medium Voltage	V_2 (1,0,-1)	V_4 (0,1,-1)	V_6 (-1,1,0)	V_8 (-1,0,1)	V_{10} (0,-1,1)	V_{12} (1,-1,0)

According to the defined switching functions, the state space equations can be developed in the three phase abc stationary coordinate system. In addition of the line currents, the dynamic of the capacitors is taken in to account and are selected as state variables. However, the phase voltage of the grid and the load current are considered as disturbances.

$$L\frac{di_a}{dt} = e_a - Ri_a - S_{a1}.V_{dc1} + S_{a2}.V_{c2} - u_{on}$$

$$L\frac{di_b}{dt} = e_b - Ri_b - S_{b1}.V_{dc1} + S_{b2}.V_{dc2} - u_{on} \qquad (9)$$

$$L\frac{di_c}{dt} = e_c - Ri_c - S_{c1}.V_{dc1} + S_{c2}.V_{dc2} - u_{on}$$

$$C_{dc1}\frac{dv_{dc1}}{dt} = S_{a1}.i_a + S_{b1}.i_b + S_{c1}.i_c - i_L$$

$$(10)$$

$$C_{dc2}\frac{dv_{dc2}}{dt} = -S_{a2}.i_a - S_{b2}.i_b - S_{c2}.i_c - i_L$$

Where u_x and i_x is the phase voltage and current of the grid (x = a,b,c). L and R are the grid filter inductor and resistance, V_{dc} is the dc voltage, and I_L is the load current. [16][17] Considering the three-phase three-line grid system balanced.
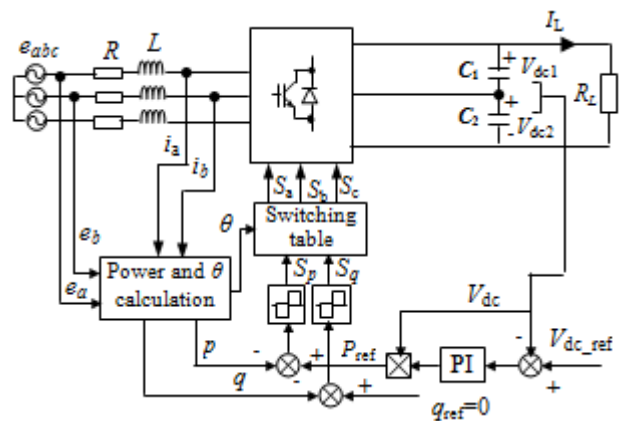
$$e_a + e_b + e_c = 0$$
$$i_a + i_b + i_c = 0 \qquad (11)$$

The voltage U_{on} can be done by:

$$u_{on} = -\frac{1}{3}(S_{a1} + S_{b1} + S_{c1})V_{dc1} + \frac{1}{3}(S_{a2} + S_{b2} + S_{c2})V_{dc2}$$

3.2 Direct Power Control Strategy (3-Level)

Figure 6 is the block scheme of DPC for three-level PWM rectifier.

Figure 6: Block diagram of direct power control DPC

It is know that the mathematical model of three-level PWM rectifier in three-phase static abc coordinates as shown in (13):

$$e_j = L\frac{di_j}{dt} + Ri_j + v_j \quad (j = a,b,c) (13)$$

Where as:
e_j, i_j: phase voltage and phase current of j-phase source.
v_j: the j-phase neutral point voltage of rectifier in AC side.

According to coordinates transformation, and neglecting internal resistance of inductance, the mathematical model of three-level PWM rectifier in dq rotational coordinates is as:

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$$L \frac{di_d}{dt} = e_d - v_d$$
$$L \frac{di_q}{dt} = -v_q \qquad (14)$$

Where as:
e_d, e_q: the d-axis and q-axis projections of source voltage, here e_d.
i_d, i_q: the d-axis and q-axis projections of source current.
v_d, v_q: the d-axis and q-axis projections of rectifier neutral point voltage in AC side.

According the instantaneous power theory:

$$p = e_d i_d + e_q i_q$$
$$q = e_q i_d - e_d i_q \qquad (15)$$

Where as:
p, q: active and reactive power of source.

Equation (14) is multiplied by e_d, and equation (15) is substituted in to it. Then the mathematical model of three-level PWM rectifier based on DPC in *dq* rotational coordinates is described as:

$$\frac{dp}{dt} = \frac{e_d}{L}(e_d - v_d)$$
$$\frac{dq}{dt} = \frac{1}{L} e_d v_q \qquad (16)$$

It is evident that the active power and passive power could be controlled by the neutral point voltage of rectifier in AC side.

For example if the reference voltage vector was located in θ_1, the influences of all space voltage vectors on active power and passive power were listed in Table. I. In Table.I, "+++"represents that the increment of active power or passive power is positive and the largest, "++" is the second, and "+" is less; "---"represents that the increment of active power or passive power is negative and its absolute value is the biggest, "--" is the second, and "-" is less; "0"represents that the increment of active power or passive power is zero. there is no influence of voltage vector on active or passive power. "×"represents that the increment of active power or passive power is uncertain. It is evident that there are fewer voltage vectors to make active power decreased. When the reference voltage vector was located in the other sections, the similar result could be deduced. [18]

Table 3: The influence for active and reactive power of each switching vectors (sector 1)

Power	V_0	V_{13}	V_{14}	V_{15}	V_{16}	V_{17}	V_{18}
p	++	+	+	++	++	++	+
q	0	-	+	++	+	-	--
Power	V_2	V_4	V_6	V_8	V_{10}	V_{12}	
p	--	+	++	++	++	X	
q	+	++	++	-	--	--	
Power	V_1	V_3	V_5	V_7	V_9	V_{11}	
p	---	X	+	+++	++	+	
q	-	++	+++	+	--	---	

3.3 Switching table for three-Level rectifier

From Table. 3, some conclusions can be carried out [19]. In each sector, there are only two switching vectors have the ability of decreasing the present active power. So it"s not necessary to set two hysteresis comparators during the negative region of active power. Some switching vectors, such as V_3 and V_{12}, are indefinite influence to the active power. It"s advisable to avoid selecting these vectors for fear uncontrollable states of the inverter. Then, the novel switching table is given in Table.4. Sp and Sq represent the demand of increment of active power and reactive power compared with reference value, which were decided by equation (17) and (18).

$$\begin{cases} \Delta p > H_{p2} \rightarrow S_p = 2 \\ H_{p2} > \Delta p > H_{p1} \rightarrow S_P = 1 \\ H_{p1} > \Delta p > -H_{p1} \rightarrow S_P = 0 \\ \Delta p < -H_{p1} \rightarrow S_p = -1 \end{cases} \qquad (17)$$

$$\begin{cases} \Delta q > H_q \rightarrow S_q = 1 \\ H_q > \Delta q > -H_q \rightarrow S_q = 0 \\ \Delta q < -H_q \rightarrow S_q = -1 \end{cases} \qquad (18)$$

Where, H_{p1}, H_{p2} and H_q are hysteresis bands of active and reactive power comparators; Δp and Δq is the error between the commands and the estimated feedback power.

Table 4: Switching table of DPC for three-level PWM rectifier

| S_p	S_q	θ_1	θ_2	θ_3	θ_4	θ_5	θ_6	θ_7	θ_8	θ_9	θ_{10}	θ_{11}	θ_{12}
2	1	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_1	V_2	V_3	V_4
	0	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_1	V_2	V_3	V_4	V_5	V_6
	-1	V_8	V_9	V_{10}	V_{11}	V_{12}	V_1	V_2	V_3	V_4	V_5	V_6	V_7
1	1	V_{17}	V_{17}	V_{19}	V_{19}	V_{21}	V_{21}	V_{23}	V_{23}	V_{13}	V_{13}	V_{15}	V_{15}
	0	V_{25}	V_{25}	V_{26}	V_{26}	V_{25}	V_{25}	V_{26}	V_{26}	V_{25}	V_{25}	V_{26}	V_{26}
	-1	V_{21}	V_{21}	V_{23}	V_{23}	V_{13}	V_{13}	V_{15}	V_{15}	V_{17}	V_{17}	V_{19}	V_{19}
0	1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}	V_{11}	V_{12}	V_1
	0	V_{13}	V_{13}	V_{15}	V_{15}	V_{17}	V_{17}	V_{19}	V_{19}	V_{21}	V_{21}	V_{23}	V_{23}
	-1	V_{11}	V_{12}	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}
-1	1	V_1	V_1	V_3	V_3	V_5	V_5	V_7	V_7	V_9	V_9	V_{11}	V_{11}
	0	V_1	V_1	V_3	V_3	V_5	V_5	V_7	V_7	V_9	V_9	V_{11}	V_{11}
	-1	V_{12}	V_{12}	V_2	V_2	V_4	V_4	V_6	V_6	V_8	V_8	V_{10}	V_{10}

4. Simulation result

To study the effectiveness of the DPC with three-level PWM rectifier, it is implemented in Matlab/Simulink environment using power system bloc-set (PSB). The simulation results obtained for different condition show that:

- The dc link voltage variation, when step change applied to V_{dcref} (from 600 to 700 volt) figure.7(a) for a DPC two-level rectifier and figure.7(a") for a DPC three-level rectifier.
- Figure. 7(b) show the active and reactive power in AC line side with the DPC two-level rectifier scheme when the

step is applied, from this response it is observed that the ripple in the active power response is around 4.5 and 6.2kw. Figure. 8(b‟) show the active power with the DPC three-level rectifier, here the ripple is around 4.6 and 6.25kw. This results show that the active power in three-level scheme has been reduced significantly. To obtain a unity power factor in AC line side the input reference of reactive power is set to zero and active power change, so the dc voltage is regulated at set point value.

- Line current obtained by DPC three-level (figure. 8(c‟)) is quasi-sinusoidal. However, there are lower ripple in line current thane hose in DPC two-level. Moreover , as shown in FFT analysis diagrams, the THD of line current in DPC three-level is 3.48% (figure.8 (d)), which is much lower than that 4.90% in DPC two-level (figure.7 (d)).

- Line current and voltage is shown in (figure7. (e) for a DPC two-level and figure.8 (e‟) for a DPC three-level rectifier). As shown in this figures the line current has some phase respect to line voltage.

The performances of the DPC two-level and the DPC three-level against the load disturbance under unit power factor operation. At 0.5s, the load power of each system has been increased 100%. It can be observed that both methods maintain UPF successfully and keep DC-bus voltage close to the reference value (figure.7 (f) for a DPC two-level and figure.8 (f‟) for a three-level rectifier). In these figures the change in the load don‟t affect DC link voltage and only change the amplitude of the line current (figure.7 (g) for a DPC two-level and figure.8 (g‟) for a three-level rectifier) and the line active side active power (figure.7 (h) for a DPC two-level and figure.8 (h‟) for a three-level rectifier).

(a)   (a‟)

(b)   (b‟)

(c)   (c‟)

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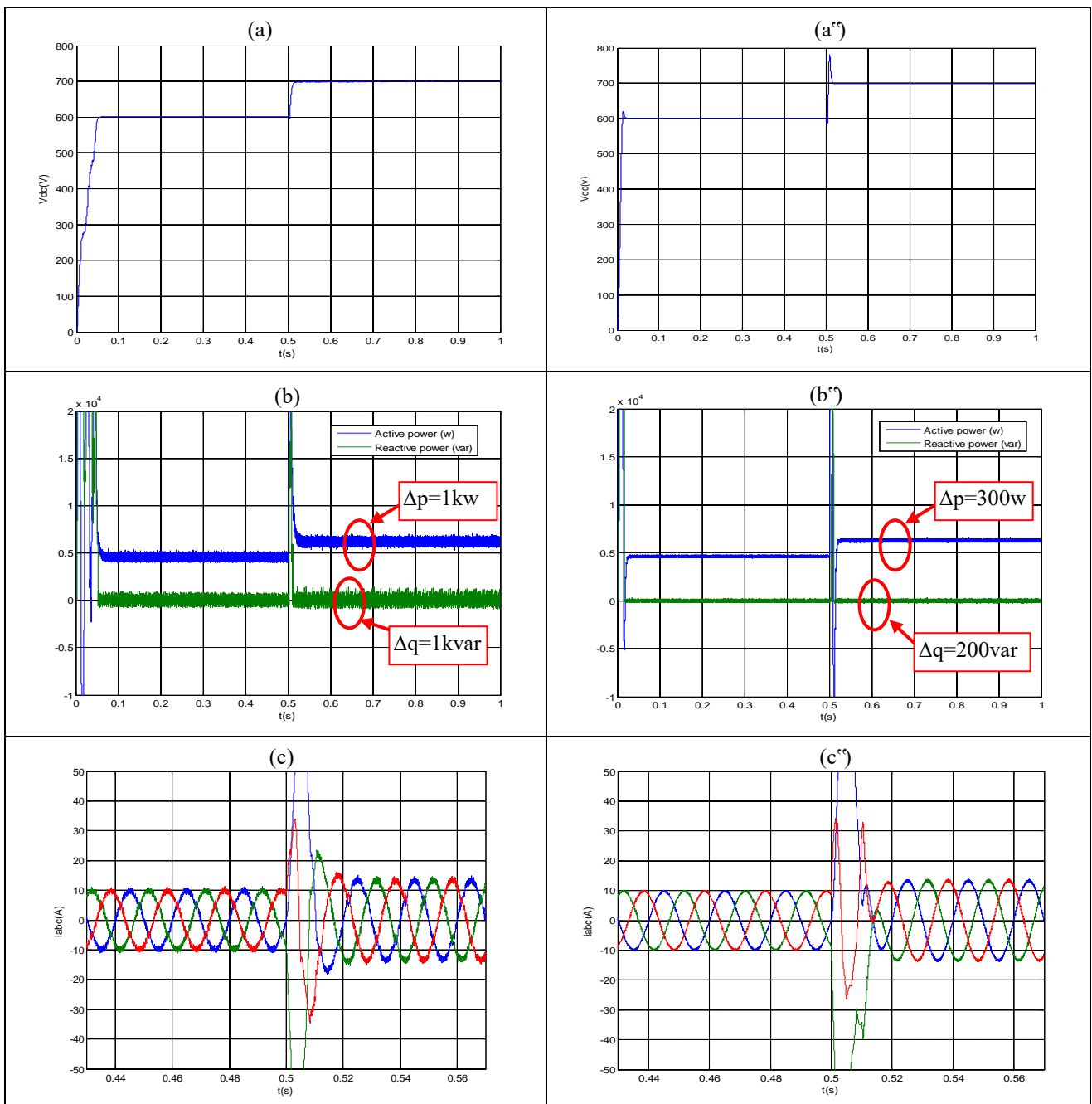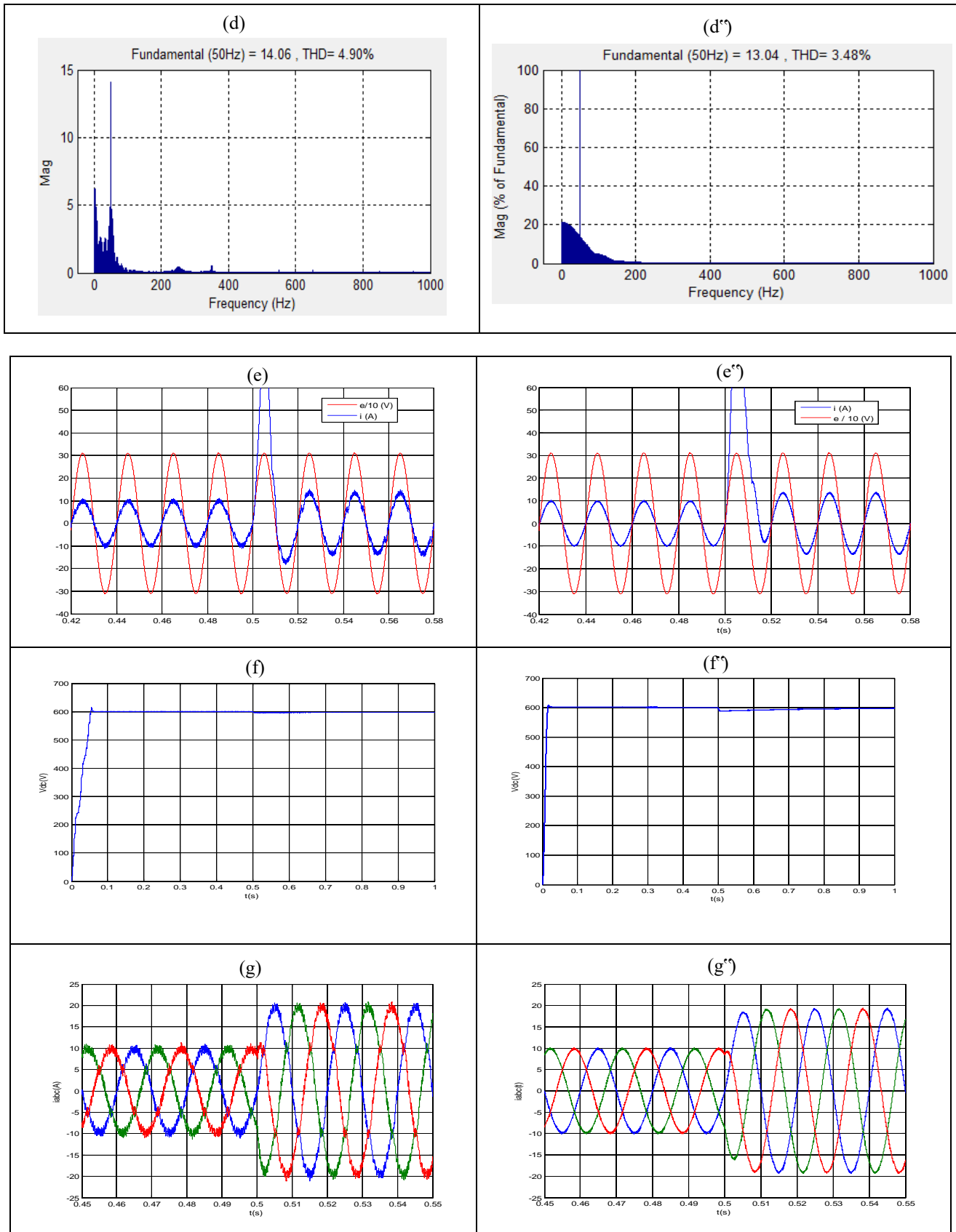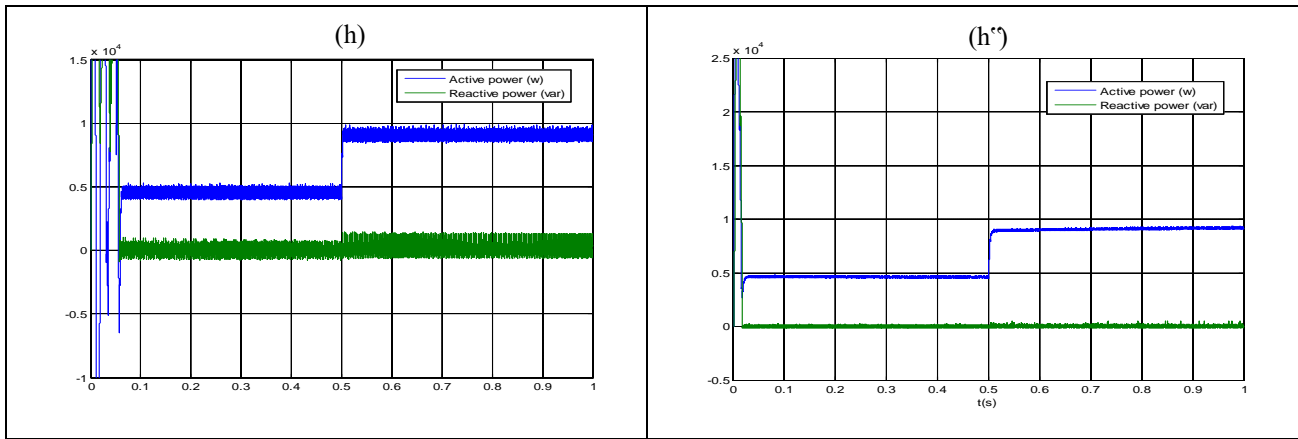
Table 5 : Parameters of circuit

Parameters	Value
Line voltage (e)	220V
Line frequency (f)	50Hz
DC bus voltage (V_{dcref})	600V
Line resistance (R)	0.25Ω
Line Inductance (L)	10mH
DC link capacitor (C)	2000μF
Sampling time (T_s)	5μs

5. Conclusion

In this article we present a DPC control strategy for two-level and three-level PWM rectifier. To predict behavior of DPC of three phase PWM rectifier in different load and supply conditions, dynamic model is implemented in SIMULINK/MATLAB.

The main goal of the control system is to maintain the DC-bus voltage at the required value and achieve UPF operation. The DPC using three-level PWM rectifiers presents good performance and ripples reductions, compared with conventional DPC. In this case, some techniques were developed in order to replace the DPC using two-level rectifiers switching table adapted for NPC rectifier.

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