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Analysis of Design of Schmitt Trigger Based SRAM Cell Using a Novel Power Reduction Technique

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Abstract: ***In low power SRAM memory cell design Power dissipation through standby leakage and dynamic loss is a major problem. this paper is mainly based on low power cell operation and delay of SRAM designing this paper presents a novel technique to reduce short circuit power. The differential SRAM for ultra low voltage design for Schmitt trigger (ST) is analyzed using 180nm CMOS technology. Schmitt trigger based differential SRAM cell design helps to sort the issues related to design problems in read and write operation of basic SRAM cell. Feed back is built in mechanism in proposed Schmitt trigger SRAM design. There is always trade-off among area, power and delay in any SRAM cell designing. In comparison to standard 6TSRAM cell the ST SRAM cell provides better read stability and having a high probability of read failure. Short circuit power dissipation is one of the considerable parameter in achieving low power. This paper mainly proposes a novel technique for achieving the low power consumption. Delay of an SRAM cell is maintained as it was without affecting the delay with the reduction of power. By using novel power reduction technique to reduce the short circuit power compared to the proposed design is reduced by 21%.The aim of this project is to develop a circuit level technique that takes advantage of program behavior to reduce power consumption with no performance degradation. These simulations are implemented by the H-spice and synopsis tool.***

Keywords: SRAM, Power Reduction, Schmitt Trigger, Static, Leakage

1. Introduction

To attain higher density performance and lower power consumption, CMOS devices have been scaled for more than 30 years. Transistor delay times decrease by more than 30% per technology Generation, resulting in doubling of microprocessor performance every two years. The main intention of this work focuses on the reduction of power consumption in SRAM cells. This paper presents a low power consumption SRAM cell and array architecture targeting high performance, low power embedded memory. For reducing the power consumption at the circuit, architectural and system level we are introducing various techniques at the different levels in the designing process.

In the designing of the system we are using SRAM or DRAM memories. SRAM or Static Random Access Memory is a form of semiconductor memory widely used in electronics, Microprocessor and general computing applications. This form of semiconductor memory gains its name from the fact that data is held in there in a static fashion, The main reasons are its design tradeoffs include density, speed, volatility, cost and custom features. SRAMs are mostly used in the circuit designs for its efficiency and cost is overhead. Since SRAM cells are high power consuming elements so we introducing the Schmitt Trigger based designs to remove the unwanted power consumption. In the transactions of SRAM cell requires minimum voltage for its operation [2], then it will search for Vmin. This will leads to delay in the circuit operation and gives the power leakage from the design. To reduce this type of power leakage and delays in the circuit we are introducing the new design. If the operating voltage of the design is reduces, it leads to reduction in the power dissipation, then stability of the SRAM cell is disturbed. So the SRAM cell will not operates the read and write operations properly. For getting better stability we are introducing 8T/10T SRAM cells [7].

This paper demonstrates the power consumption of various models of SRAM cell with feedback mechanism circuit technique. All the circuit simulations have been done using mentor graphics tool. Finally, the analysis of the power consumption of various SRAM designs with the proposed design is shown. To increase the read stability extra peripheral circuitry can be added to 6T SRAM bit cell at the cost of increased area overhead and power consumption. Several SRAM bit cell topologies have been proposed in the recent past to improve read stability.

2. Standard 6T SRAM Cell

The CMOS 6T SRAM bit cell design is shown in figure 1. 6T cell is most widely used in embedded memory because of its fast access time and comparatively small area [1]. The standard 6T SRAM cell forms two cross-coupled inverters. Which are controlled by the word line (WL) signal, This storage cell has two stable states which are used to denote 0 and 1.during the read operation the „0" storing node voltage is disturbed which might flip the stored data. For reliable read operation the design requirement is such that the data should not be flipped

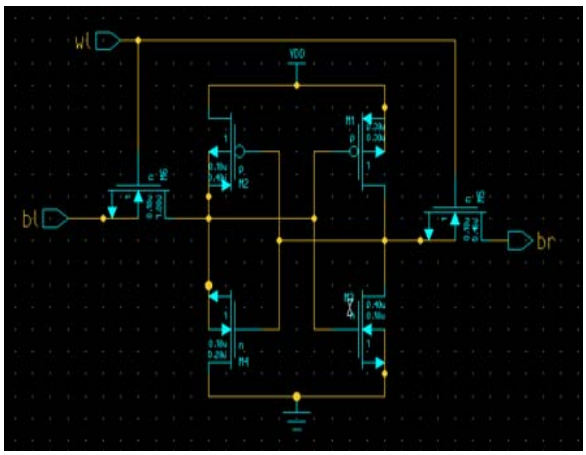

Figure 1: Standard 6T SRAM CELL

During write operation the design recruitment is such that the data should be flipped as easily as possible. In order to tenacity the read versus write operation in the 6T cell, we apply Schmitt trigger principle for the cross -coupled inverter pair. A Schmitt trigger principle is used to vary the switching threshold of an inverter depending on the direction of input transition

3. Schmitt Trigger Principle:

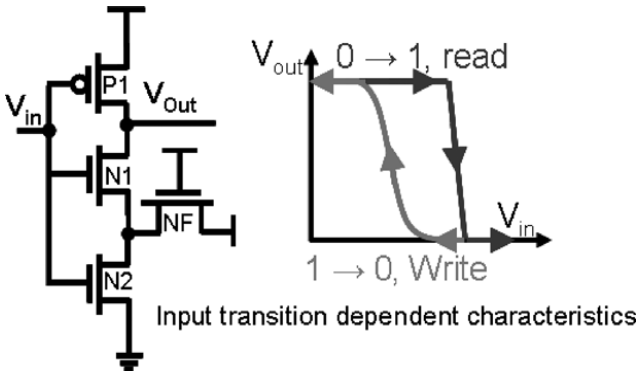

Figure2: Basic Schmitt trigger

In order to resolve the read versus write conundrum in the 6T cell, we apply Schmitt trigger principle for the cross coupled inverter pair. A Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. In the proposed Schmitt trigger SRAM cell, the feedback mechanism is used only in the pull down path as Shown in Fig. 2. During 0 to 1 input transition, the feedback transistor tries to preserve the logic „1" at output (Vout) node by raising the source voltage of pull down NMOS (N1). These Consequences in higher switching threshold of the inverter with very sharp transfer characteristics. For the 1 to 0 input transition the feedback mechanism is not present. This results in smooth transfer characteristics essential for easy write operation. Thus input dependent transfer characteristics of the Schmitt trigger improves both read-stability as well as write–ability of the SRAM cell. the Schmitt Trigger (ST) cell is in termed as "ST-1" bit cell while the other Schmitt Trigger bit cell is termed as „ST-2" bit cell.

4. Existing Techniques

ST-1 Bit cell:

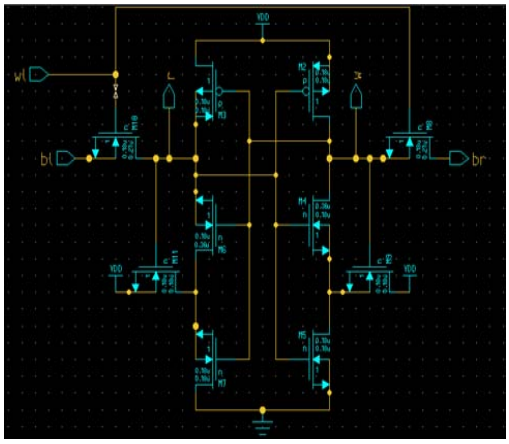

Figure3: Schmitt trigger-1 Bit cell

Fig. 3 shows the schematics of the ST-1 bit cell. The ST-1 bit cell utilizes differential sensing with ten transistors, one word-line (WL), and two bit lines (BL/BR). Transistors M2-M5-M6-M10 forms one ST inverter while M1-M3-M4-M8 forms another ST inverter. Feedback transistors M8/M10 raise the switching threshold of the inverter during the input transition giving the ST action. Detailed operation of the ST-1 bit cell can be found in [3].

ST-2 Bit cell:

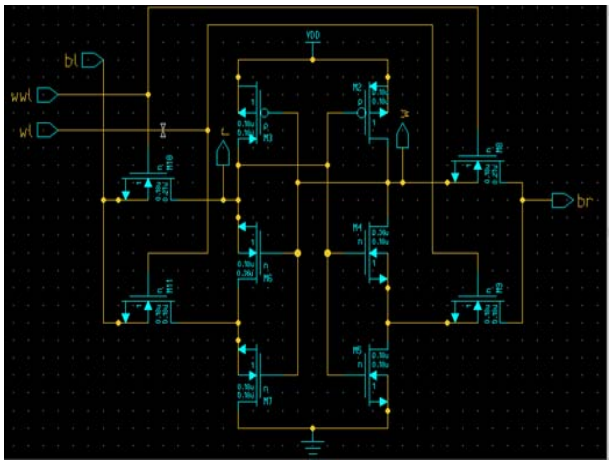

Figure 4: Schmitt trigger-2 Bit cell

	WL	WWL
WRITE	1	0
READ	1	1
HOLD	0	0

Fig. 4 shows the schematics of the ST-2 bit cell utilizing differential sensing with ten transistors, two word-lines (WL/WWL), and two bit lines (BL/BR). The WL signal is asserted during read as well as the write operation, while WWL signal is asserted during the write operation. During The hold-mode, both WL and WWL are OFF. In the ST-2 bit cell, feedback is provided by separate control signal (WL)

unlike the ST-1 bit cell, where in feedback is provided by the Internal nodes.

During the read operation **r** is storing logic „0"and **w** is storing logic „1". When WL is turned ON, (WWL is OFF for the duration of read) For the inverter storing „1" the feedback mechanism is provided by the WL access transistor (M8) compared to the 6T cell the results are better by read stability.

During the write operation, assume **r=0** and **w=1**. In write mode both WL and WWL are turned on while BR is pulled to GND and BL is charged to VDD. For the left-side inverter, both access transistors M9 and M10 might current through the pull down transistor M6.increased current through M6 increases the voltage at the node **r** to be higher than the read mode voltage.

In the ST-1 bit cell, the feedback mechanism is effective as long as the storage node voltages are maintained. Once the storage nodes start transitioning from one state to another state, the feedback mechanism is lost [6]. To improve the feedback mechanism, separate control signal WL is employed for achieving stronger feedback. Exhaustive operation of the ST-2 bit cell is explained in our earlier work [4].

5. Modified Design

Figure. 5 show the schematic of Read error reduction technique with the eight transistor count. As the Schmitt trigger based designs are having high number of transistor to construct the read stability that is 10T SRAM cell. which are very high, when compared to the existing 6T SRAM Design.

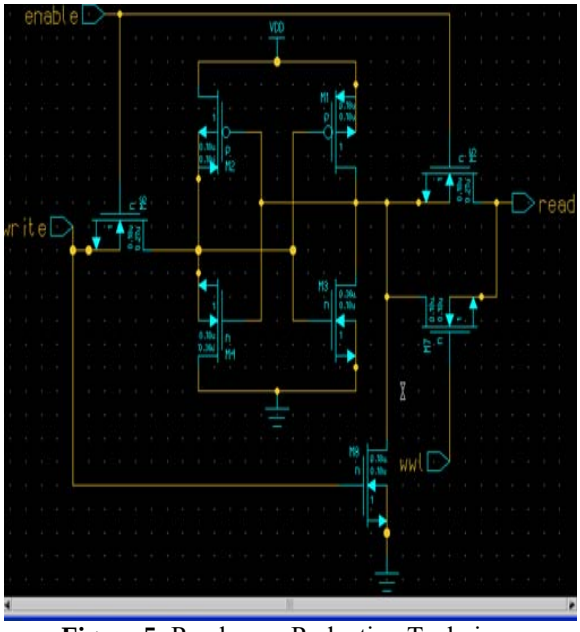

Figure 5: Read error Reduction Technique

We are going to combine the mentioned read stability at the above part to our proposed work to reduce the count than the Schmitt trigger based designs at the same time we are going to achieve reduced power consumption with reduced transistor count without affecting the read stability [5].

6. Proposed Design

Novel power reduction technique

In this novel technique, two pass transistors are inserted at the two end of the SRAM cell. Here the idea is to break any short circuitry in the cell. One PMOS is inserted between VDD and the cell having the logic „0" at the gate of PMOS, similarly NMOS is inserted between the cell and the GND and the cell having the logic „1" at the gate of NMOS.

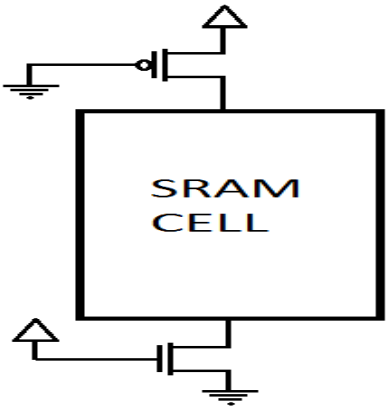

Figure 6: A Novel power reduction technique

7. Proposed Technique Applied On 4t, 6t, 8t And 10t, St1, St2 Architecture

The architecture of basic 4T, 6T, 8T and 10T, ST1, ST2 SRAM are modified using the proposed technique. In the modified architecture the threshold voltages, W/L ratios of all the NMOS and PMOS transistors and the power supply were same as of the parent architectures and two pass transistors are inserted at the two end of the SRAM cell as per the proposed technique. The architectures of modified 4T, 6T, 8T and 10T, ST1, ST2 cells are shown in fig-7, fig-8, fig-9, fig-10, fig-11 and in fig-12 respectively. The simulation result for this SRAM CELL designs has shown in this waveforms. The simulation is carried out of 200MHZ frequency.

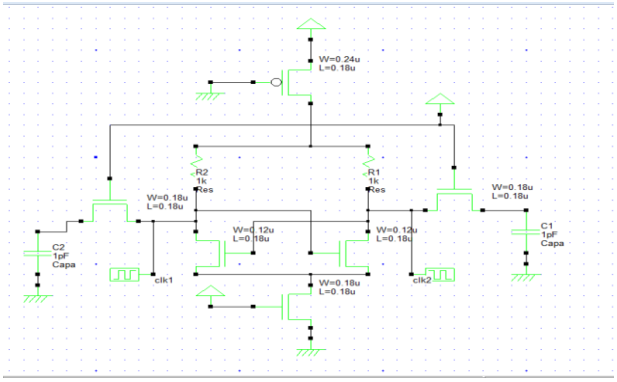

Figure 7: 4T SRAM Cell Design

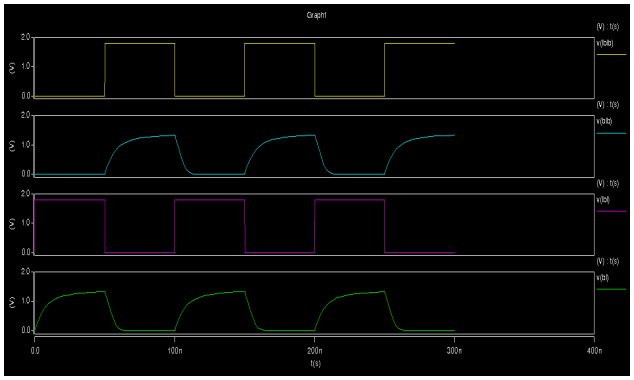

Figure 7.1: Read waveform of 4T SRAM Cell

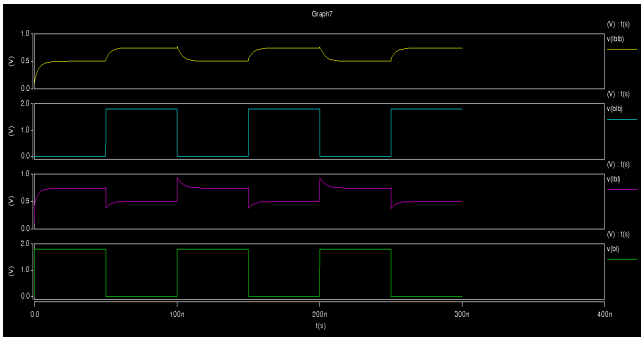

Figure 7.2: Write waveform of 4T SRAM Cell

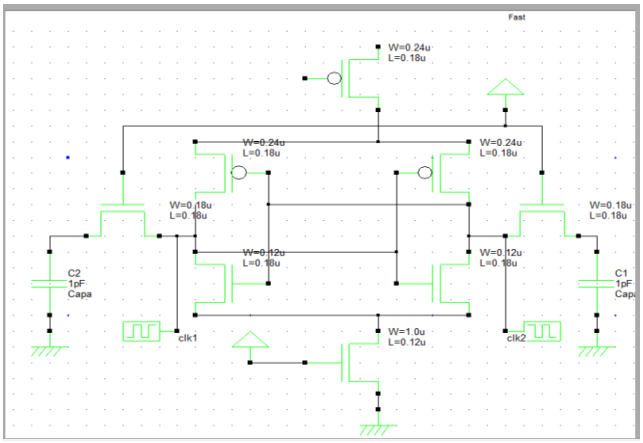

Figure 8: Schematic Of 6T SRAM Cell

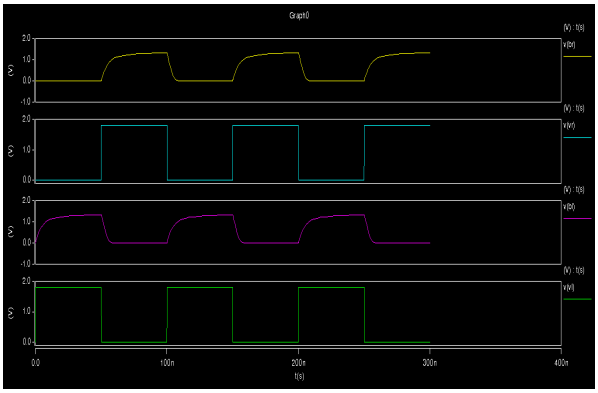

Figure 8.1: Read waveform of 6T SRAM Cell

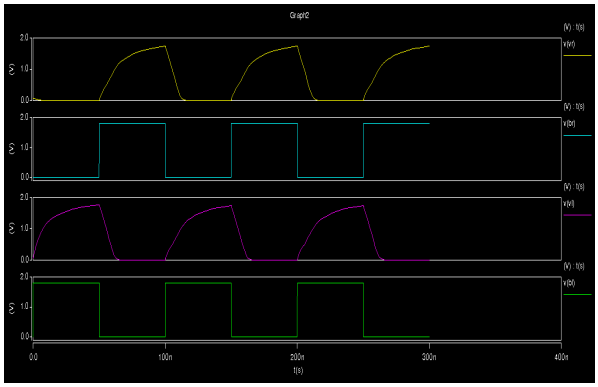

Figure 8.2: Write waveform of 6T SRAM Cell

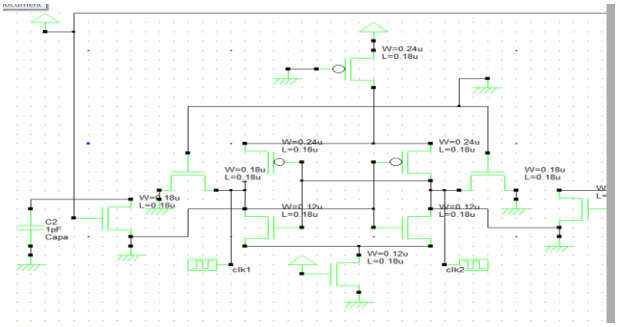

Figure 9: Schematic Of 8T SRAM Cell

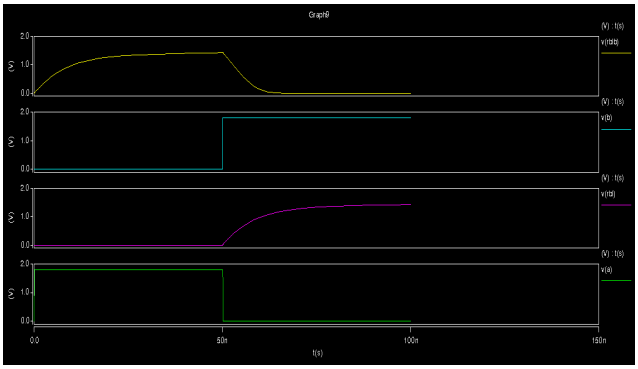

Figure 9.1: Read waveform of 8T SRAM Cell

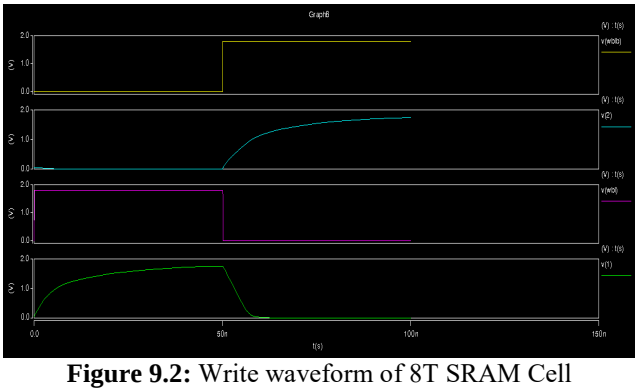

Figure 9.2: Write waveform of 8T SRAM Cell

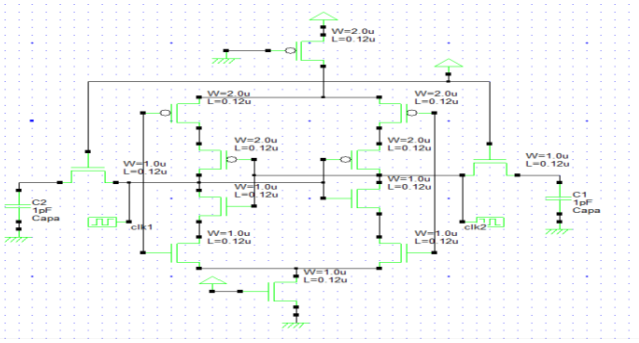

Figure 10: Schematic of 10T SRAM Cell

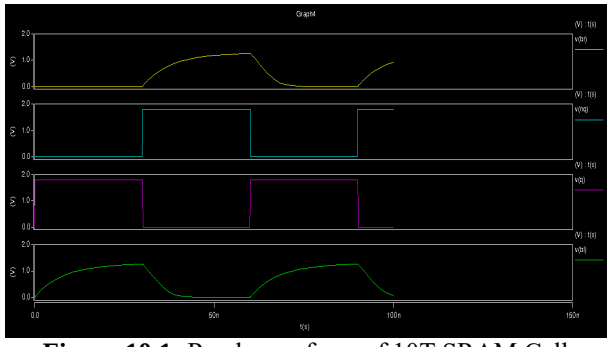

Figure 10.1: Read waveform of 10T SRAM Cell

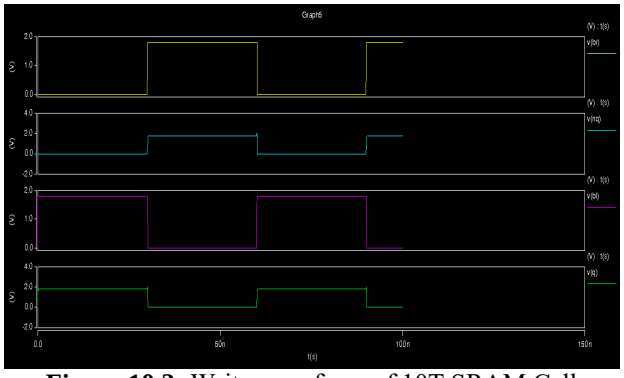

Figure 10.2: Write waveform of 10T SRAM Cell

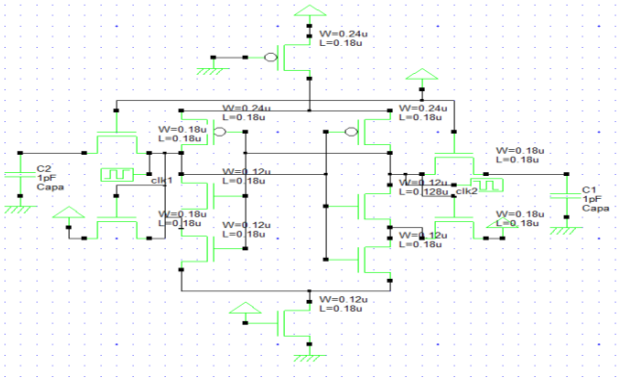

Figure 11: Schematic of ST1 SRAM Cell

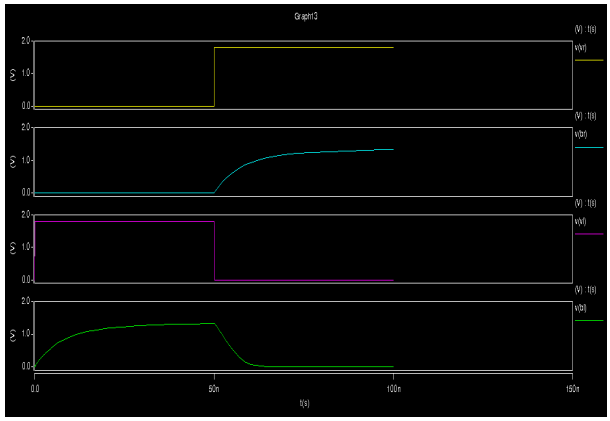

Figure 11.1: Read waveform of ST1 SRAM Cell

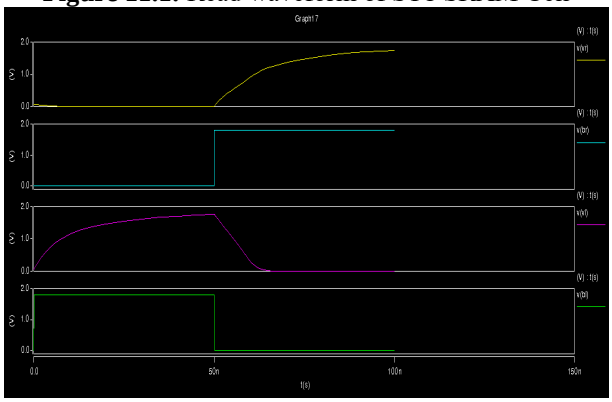

Figure 11.2: Write waveform of ST 1SRAM Cell

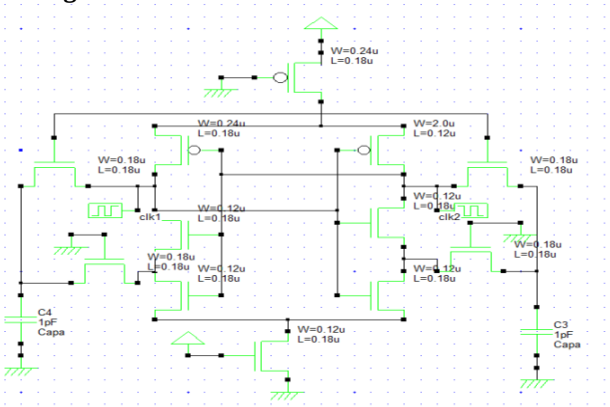

Figure 12: Schematic of ST2 SRAM Cell

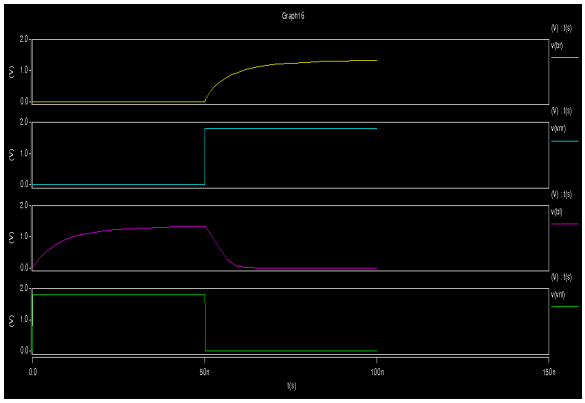

Figure 12.1: Read waveform of ST2 SRAM Cell

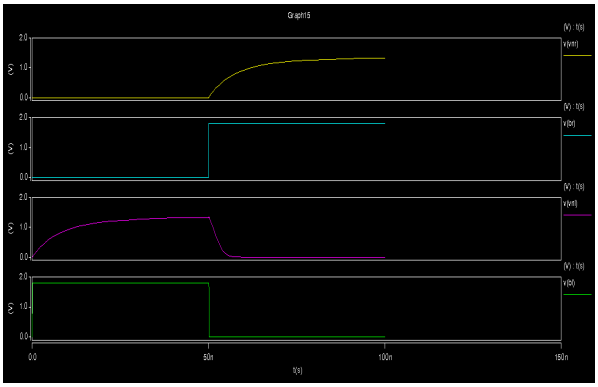

Figure 12.2: Write waveform of ST2 SRAM Cell

Table 1: Comparisons of Total power dissipation

S. No	*Modified SRAM Arch*	*Write Power*	*Read Power*
1	SRAM-4T	2.9511E-04	1.7292E-03
2	SRAM-6T	6.5213E-05	4.5279E-05
3	SRAM-8T	5.5481E-05	4.1217E-05
4	SRAM-10T	5.1972E-07	8.1305E-05
5	SRAM-ST1	9.6079E-05	2.5647E-05
6	SRAM-ST2	3.5620E-05	2.5685E-05

8. Conclusion

The proposed SRAM cell is designed purely to reduce the short circuit power flowing in static path from vdd to gnd. By adding one PMOS and one NMOS one at the top of the SRAM cell and the other one at the bottom of the cell reduces the static path dissipation. The power of the proposed design is reduced in all the SRAM cells

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