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# Design and Analysis of Dynamic Current Mode Full Adder with reduced Power and Delay

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**Abstract:** ***Current mode logic (CML) technology is popular as it offers high performance with very low power dissipation, equal charging and discharging times, equal noise margins and low output logic swing, therefore high-speed performance is achieved . In this paper, MOS current mode logic (MCML) , dynamic current mode logic (DyCML) and cascaded dynamic current mode logic techniques are analyzed and applied to the generation of digital arithmetic circuits. Based on the presented analysis a new current mode full adder is proposed where the circuit of Dynamic Current mode full adder is modified. It is shown that in the proposed full adder circuit both the power consumption and delay time are reduced. The circuits are simulated using TANNER tool with 0.18µm technology and supply voltage 1.5V.***

**Keyword:** MOS current mode logic, Power dissipation ,Output voltage swing Dynamic poer consumption, Self timed buffer.

## 1. Introduction

A digital circuit that seems to be promising in terms of power dissipation and high performance at relatively high frequencies is the current mode logic (CML) circuit. Current mode logic (CML) technology is popular as it offers high performance with very low power dissipation, equal charging and discharging times, equal noise margins and low output logic swing, therefore high-speed performance is achieved. In comparison with CMOS circuits, current mode logic (CML) circuits dissipate constant static power. Also, current mode logic (CML) circuits operate at lower dynamic power to reduce the output swings, which achieves faster switching performance.Therefore,current mode logic (CML) technology offers extreme flexibility in the digital logic design and is suitable for mixed signal applications [1]. Lower cross talk between digital and analog circuitry is achieved by the constant current supplies which makes current mode logic (CML) a promising candidate for mixed-mode systems.

MOS current mode logic circuits are known for its typical high speed and low power consumption. This makes its speed higher and power consumption lower than that of traditional MOS circuit at high frequencies. In this logic circuit the noise of switch is very low; this important property of MCML makes it applicable to the design of hybrid circuits (analog-digital) in order to reduce the Interference (noise) between the digital and analog signals. It brings higher immunity to supply noise and process variation [2]. Other advantageous characteristics of MCML are lower crosstalk owing to the reduced output voltage swing, and lower generated noise level owing to the constant current flowing through the supply rails.

DyCML circuits combine the advantages of MOS current mode logic (MCML) circuits with those of dynamic logic families to achieve high performance at a low-supply voltage with low-power dissipation. Unlike CML circuits, DyCML gates do not have a static current source, which makes DyCML a good candidate for portable devices and battery powered systems. The DyCML circuits show better performance and less dynamic power consumption than other dynamic families or static MCML circuits DyCML circuits have nearly zero dynamic current sources that minimize static power and the other disadvantages of the conventional static current sources [7].

In this paper, MOS current mode logic (MCML) , dynamic current mode logic (DyCML) and cascaded dynamic current mode logic techniques are analyzed and applied to the generation of digital arithmetic circuits. We have proposed a new full adder circuit with reduced power consumption, less delay and less power delay product using TANNER EDA tool with 180nm technology. The thesis contain analysis of existing current mode full adders using same tool and technology and the result of the simulation of MCML, DyCML and Cascaded DyCML adders are compared with the simulation result of the proposed full adder. The comparison shows that the proposed full adder has least power consumption and power delay product and reduced delay with respect to existing current mode adders.

## 2. Methodology

### 2.1 MCML Full Adder [2,4]

The MCML logic circuit consists of generally three main parts: (1) the pull up resistors, (2) the pull down network (PDN) switch and finally (3) the current source. The inputs to the pull down network (PDN) are completely differential in nature. The PDN can implement any logic function but the condition is that must have a definite value for all possible input combinations. The output and its complement are available at the two arms as indicated in the figure. The PDN is grounded through a constant current source I, which is usually an NMOS transistor

The logic equations for a full adder are well known to be an XOR3 for the sum and a 3 input majority vote for the carry.

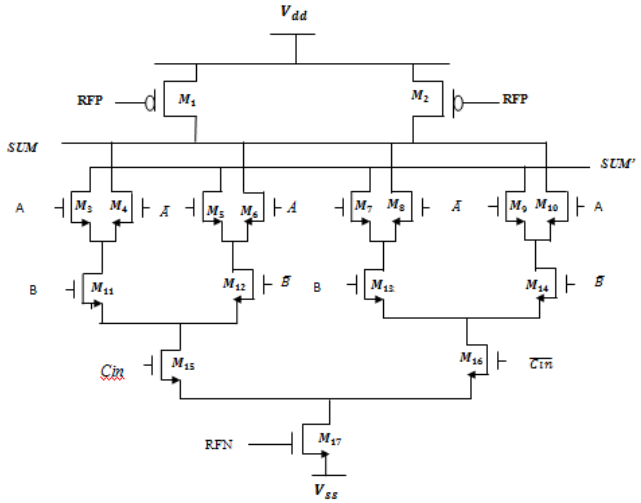


**Figure 1:** MCML Full Adder Sum Circuit

### 2.2 DyCML Full Adder [6,7]

To achieve the high-speed characteristics of MCML, but exclude its drawbacks, the current source and load resistors of the MCML gate should be redesigned. Dynamic Current Mode Logic (DyCML) employs a dynamic current source with a virtual ground to eliminate the static power and other side effects associated with the conventional static current source.The basic architecture of a DyCML logic gate consists of an MCML block for logic function evaluation, precharge circuit ,a dynamic current source and a latch to preserve logic value after evaluation[7].

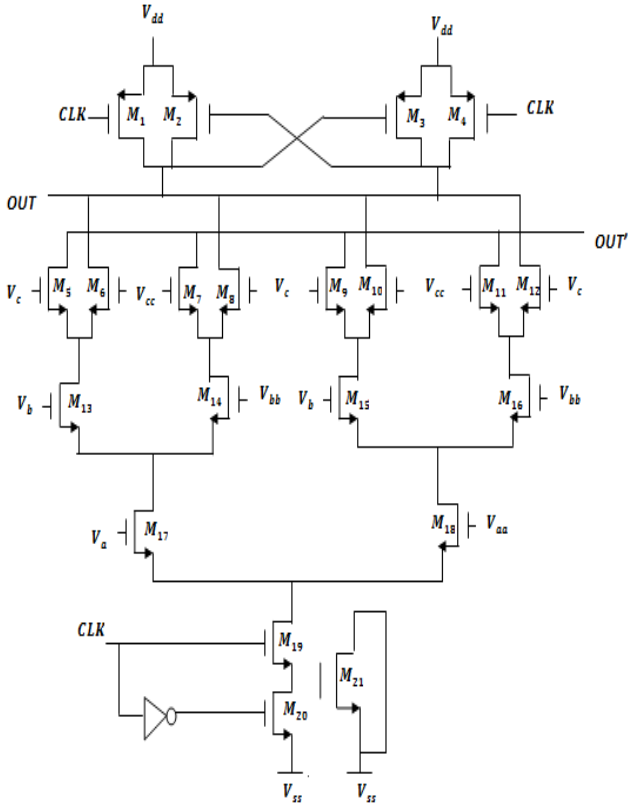


**Figure 2:** DyCML Full Adder Sum Circuit

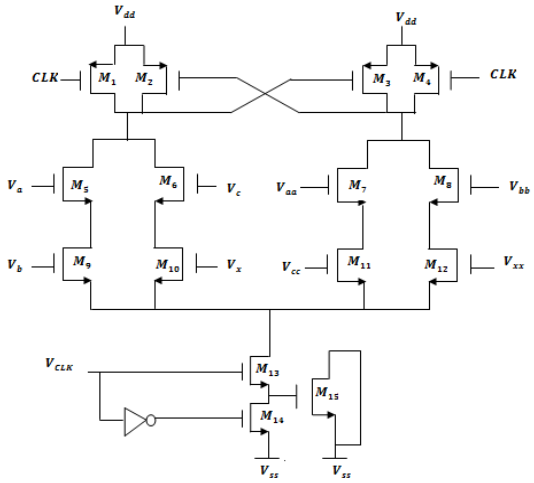


**Figure 3:** DyCML Full Adder Carry Circuit

The Full Adder-Sum and Carry DyCML circuits shown in figure 2 and 3 consist of a precharge circuit that is formed of transistors $M_1, M_4$ and $M_{20}$ ( $M_1, M_4$ and $M_{14}$ in case of the Full Adder-Carry), a dynamic current source that is formed of transistors $M_{19}$ and $M_{21}$ ( $M_{13}$ and $M_{15}$ in case of the Full Adder-Carry) and finally an evaluation which consists of transistors $M_2$ and $M_3$. Transistor $M_{21}$ ( $M_{15}$ in case of the Full Adder-Carry) acts as a capacitor transistor to decrease the amount of charge transferred from the output nodes

### 2.3 Cascaded DyCML Full Adder Circuit using Self-timed Buffer [6,7]

In the self-timed buffering scheme introduced in [7], the voltage signal coming from the capacitor transistor is converted to a full swing voltage signal used as a clock waveform signal for the next DyCML stage [7].

#### 2.3.1 Self-timed Buffer Circuit [6]

Self-timing requires each gate to generate a completion signal for the following logic level as figure 2.13 In DyCML, this signal may be the voltage on the transistor/capacitor $C_1$ (node d in the DyCML gate schematic). A special buffer is used to convert this signal to a full swing signal to be used as the clock signal for the next block [6].

It consists of a cascade of two clocked inverters. The PMOS transistor of the second buffer is removed to reduce the delay of the generated clock signal. The input to the first inverter EOE (the End Of the Evaluation) is the voltage on the transistor $C_1$ from the previous logic level.

When the clock is low, transistor $Q_1$ turns ON, charging node i to $V_{dd}$ which turns transistor $Q_5$ OFF. Transistor turns $Q_3$ ON and discharges the output node to "0." Since the transistor $C_1$'s gate is discharged to "0" and the clock is low, transistor $Q_4$ turns OFF during this clock phase.

When the clock (CLK) is high, transistor $Q_1$ turns OFF while transistor $Q_3$ turns OFF. Until EOE input starts to rise, no current will pass from node i to the ground, keeping transistor $Q_5$ OFF. When the input starts to rise, transistor $Q_4$ switches on, discharging the node to "0." Consequently, transistor $Q_5$ turns ON to charge the output node to $V_{dd}$ .

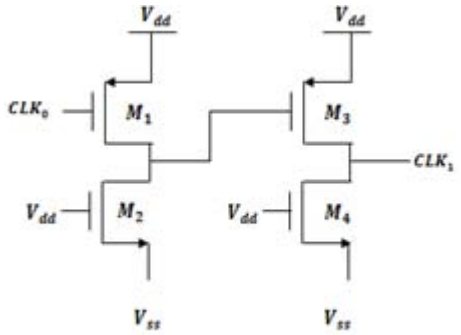


**Figure 4:** Self –timed Buffer Circuit

### 2.3.2 Cascaded DyCML Full Adder [7]

In cascaded DyCML full adder sum circuit, two dynamic full adder sum circuits, one connected to a square wave pulse clock and the other is connected to a Self-timed buffer used to convert the signal coming from transistors $M_{21}$ to clock signal.

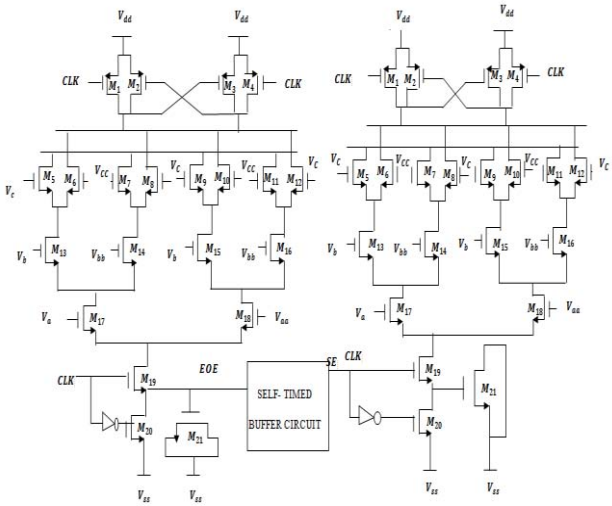


**Figure 5:** Cascaded DyCML Full Adder Sum Circuit

In the same manner in cascaded DyCML full adder carry circuit, two DYCML full adder carry circuits are used ,one of which is connected to square wave clock pulse and other is connected to self timed buffer out.

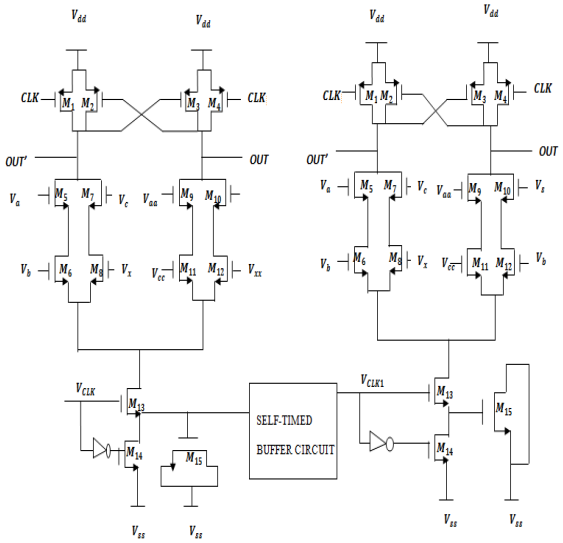


**Figure 6:** Cascaded DyCML Full Adder Carry Circuit

### 2.4 Proposed Full Adder

The proposed circuit is based on DyCML logic with a change in evaluation control logic. The circuit presents better results in terms of power and propagation delay in comparison to DyCML. The reduction in delay and power consumption of circuit is due to removal of NMOS from tail and insertion of NMOS devices just below output nodes respectively.

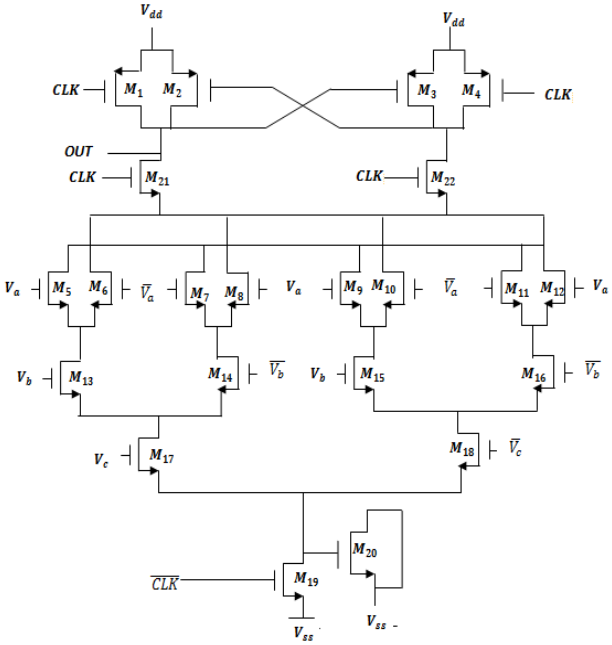


**Figure 7:** Proposed Full Adder Sum Circuit

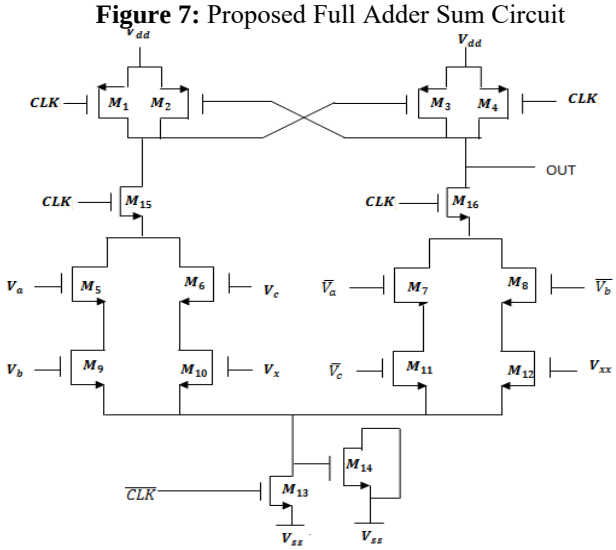


**Figure 8:** Proposed Full Adder Carry Circuit

In pre-charge phase (CLK low) the top PMOS devices are on which charge the output and out_bar nodes to high. At this time the 2 NMOS devices below out and out_bar nodes are off which reduces effective parasitic capacitance at out and out_bar. This helps in reducing power consumption as switching power reduces (due to reduced C).

In evaluation phase the delay is reduced as we have removed the tail NMOS device present in DyCML. This helps in discharging the parasitic capacitances of lower NMOS logic circuit even before the clock goes high. In DyCML discharge of total capacitance (output node and intermediate) is

dependent on lower tail NMOS. In DyCML total capacitance discharge starts when clock starts rising. In proposed technique parasitic capacitance of NMOS logic discharges before clock goes high and remaining capacitance of output node discharges when clock goes high. This speeds up evaluation process.

## 3. Simulation Results

Table 1 shows the comparison of power, delay, speed and Power Delay Product (PDP) of previous current mode full adders and Proposed full adder. The circuits are simulated using the TANNER EDA tool with 180nm technology. The Input specifications of simulated circuits are as follows: supply voltage ($V_{dd}$) is 1.5V, clock rise and fall time 100ns, clock period is 60ns.

**Table 1:** Comparison of previous current mode full adders with Proposed Full adder

| GATE TYPE | | MCML | DyCML | CASCADED DyCML | PROPOSED FULL ADDER |
|---|---|---|---|---|---|
| FULL ADDER SUM | POWER | 0.49712 mW | 0.37666 nW | 0.39774 nW | 0.030097nW |
| | DELAY | 0.20214 us | 0.17005 us | 0.21204 us | 0.19178 us |
| | PDP | 1.0049e-010 | 6.4051e-017 | 8.4336e-017 | 5.7720e-018 |
| FULL ADDER CARRY | POWER | 0.47231 mW | 0.42685nW | 0.47590 nW | 0.02126 nW |
| | DELAY | 0.32306 us | 0.26178 us | 0.32378 us | 0.23966 us |
| | PDP | 1.5258e-010 | 1.1174e-016 | 1.5408e-016 | 5.0952e-018 |

In Transient analysis of MCML full adder plot is drawn for Input Signals ($V_a$, $V_b$ $V_{c,,}$), Output Signal ($V_{out}$) with respect to Time.

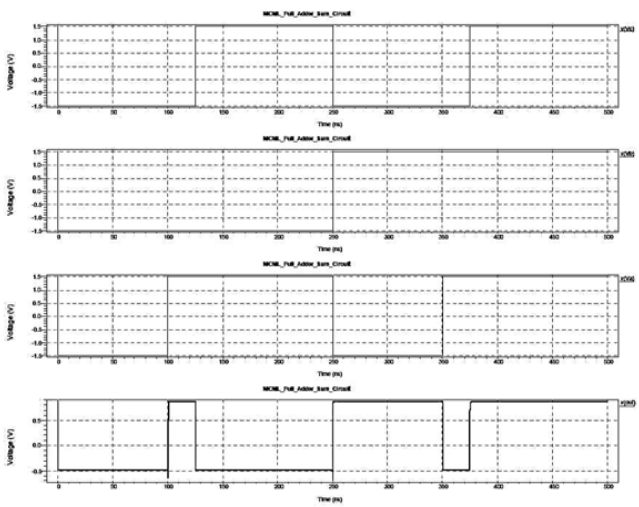

**Figure 9:** Transient analysis of MCML Full adder sum

In Transient analysis of Dynamic current mode logic full adder sum circuit plot is drawn for Input Signals ($V_a$, $V_b$ $V_{c,,}$), clock signals ($V_{clk}$, $V_{clk\_bar}$) Output Signal ($V_{out}$) with respect to time.

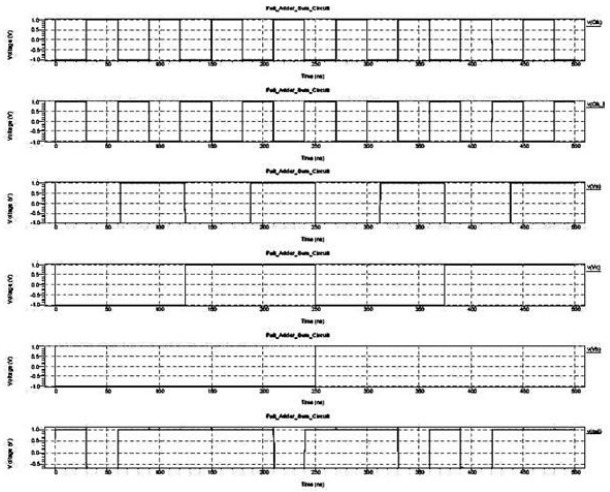

**Figure 10:** Transient analysis of Dynamic current mode logic full adder sum

In Transient analysis of DyCML full adder carry circuit plot is drawn for for Input Signal ($V_a$ ,$V_b$, $V_c$), clock Signal ($V_{clk}$ ,$V_{clk\_bar}$ ), Output Signal ($V_{out}$, $V_{out1}$) with respect to time.

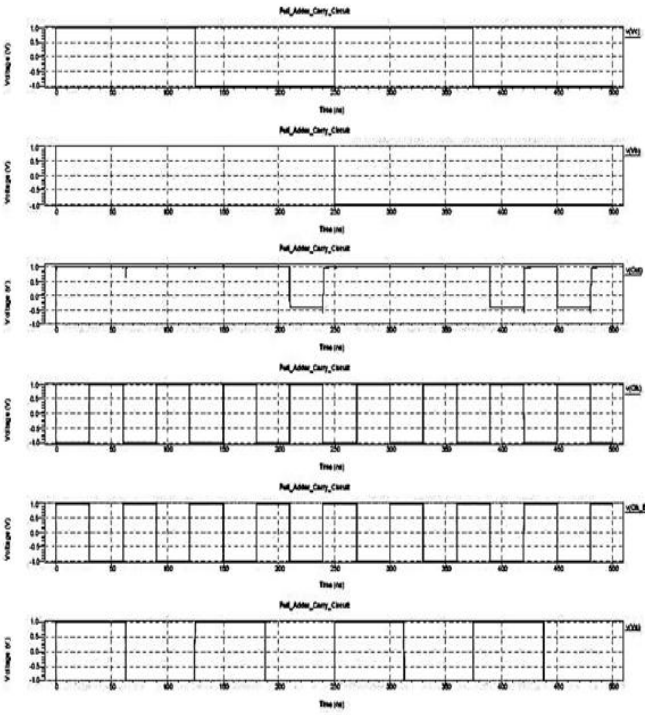

**Figure 11**: Transient analysis of Dynamic current mode logic full adder carry

In Transient analysis of cascaded Dynamic current mode logic full adder sum circuit using self timed buffer plot is drawn for Input Signal ($V_a$ ,$V_b$, $V_c$), clock Signal ($V_{clk}$ ,$V_{clk\_bar}$ ), Output Signal ($V_{out}$, $V_{out1}$) with respect to time.

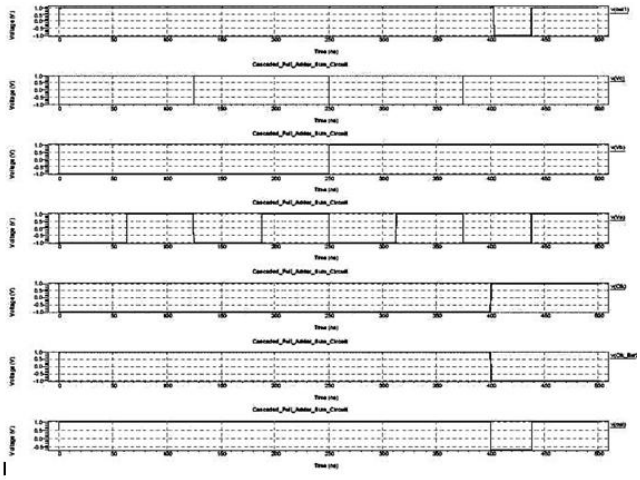

**Figure 12:** Transient analysis of Cascaded Dynamic current mode logic full adder sum

In Transient analysis cascaded dynamic full adder carry circuit using self timed buffer plot is drawn for Input Signal ($V_a$ ,$V_b$, $V_c$), clock Signal ($V_{clk}$ ,$V_{clk\_bar}$ ), Output Signal ($V_{out}$, $V_{out1}$) with respect to time.

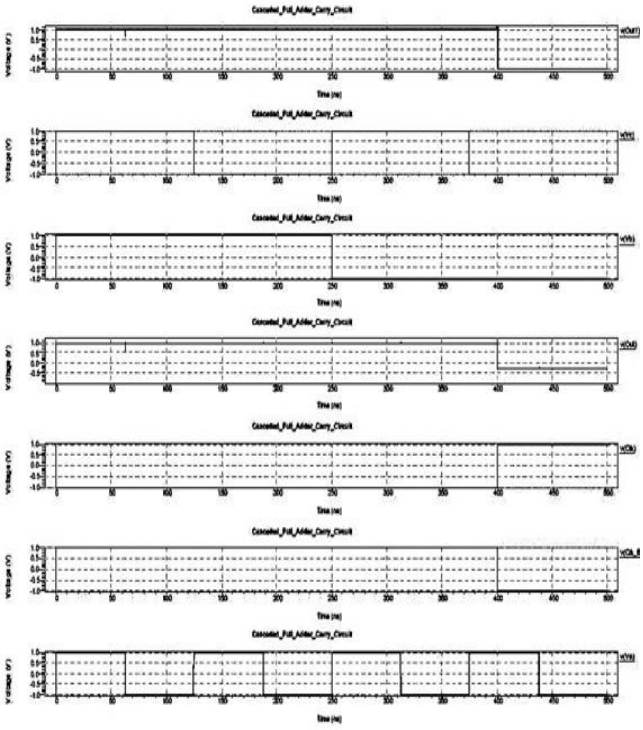

**Figure 13:** Transient analysis cascaded dynamic current mode logic full adder carry

In Transient analysis of proposed full adder sum circuit plot is drawn for Input Signals ($V_a$, $V_b$ $V_{c,,}$), clock signals ($V_{clk}$, $V_{clk\_bar}$) Output Signal ($V_{out}$) with respect to time.

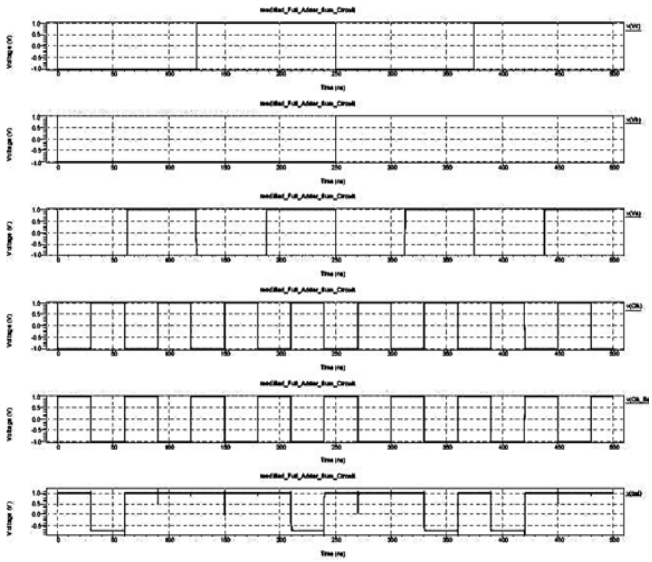

**Figure 14:** Transient analysis proposed full adder sum

In Transient analysis of proposed full adder carry circuit plot is drawn for Input Signals ($V_a$, $V_b$ $V_{c,,}$), clock signals ($V_{clk}$, $V_{clk\_bar}$) Output Signal ($V_{out}$) with respect to time.

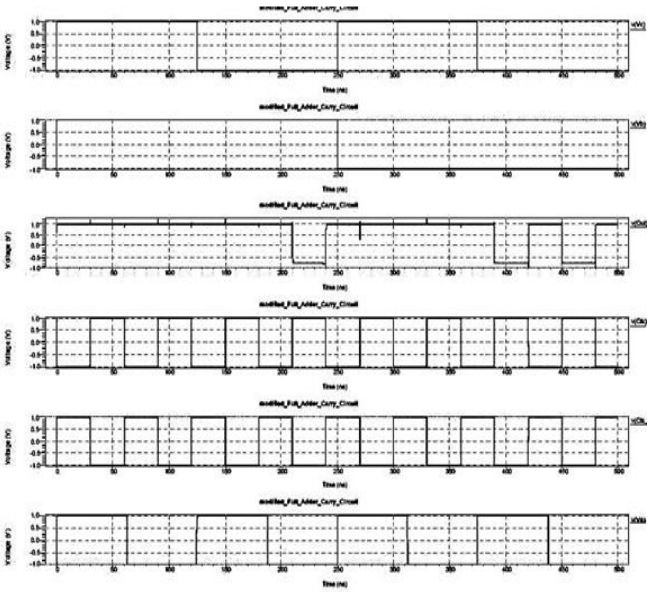

**Figure 15:** Transient analysis proposed full adder carry

## 4. Conclusion

In this paper, we have first discussed various current mode logic techniques. We have analyzed and simulated the present Current mode logic adders with the help of MCML, DyCML and Cascaded DyCML technologies with TANNER EDA tool with 180nm technology.

Secondly a new A new full adder is designed, analyzed and simulate with the same technology. Thirdly, a comparison is made between the simulation results of the various current mode adders and with the simulated result of proposed adder circuit. The comparison result shows that proposed full adder has less power consumption and power delay product as compared to present adders with better speed. So the

proposed adder can be used in large arithmetic circuits with reduced power consumption and high speed.

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