

# 8 Bit Instructional Processor using FPGA

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**Abstract:** Processor is the logic circuitry that responds to and processes instructions, whereas FPGA contains an array of programmable logic blocks which can be configured to perform various functions. The main purpose of this paper is to realize functions of 8 bit processor using Spartan 6 and Opcodes are optimized in such a manner to reduce its complexity and later on can be used to reduce power consumption. Functions of processor in different modules are programmed using VHDL programming. Xilinx ISE 12.4 is used and results are verified using Isim simulator. Regarding hardware results are verified using Spartan-6 XC6LX16-CS324 board along with additional inputs and outputs by interfacing it with laptop. 8085 processor was taken as reference. Instructions from Arithmetic, logical, data transfer, machine control and branching group were tested.

**Keywords:** FPGA, Instructions, Opcodes, Processor, Spartan 6.

## 1. Introduction

A field programmable gate array (FPGA) is programmable logic device that supports implementation of relatively large logic circuits. The standard logic elements are available for the designer and these elements need to be interconnected to achieve the desired functional performance. The Spartan-6 family provides leading system integration capabilities with the lowest total cost for high-volume applications. It delivers expanded densities ranging from 3,840 to 147,443 logic cells, with half the power consumption of previous Spartan families with faster and more comprehensive connectivity.

Microprocessors are essential to many of the products we use in day-to-day life such as TVs, cars, radios, home appliances and of course computer. Microprocessor computing expressions with more than two terms requires a sequence of arithmetic and/or logical operations, and in many cases, there is a need for assigning a temporary variable. FPGAs can increase the performance of such systems by performing such computations in parallel with a reasonable amount of combinational logic. This paper includes implementation of various functions of Microprocessor using Spartan-6 FPGA. Various instructions of microprocessor from data transfer group, arithmetic group, logical group, machine control and branching group have been programmed and tested. Xilinx ISE 12.4 is used to program. Performance of codes is verified using Isim simulator. After which they are tested on Spartan-6 FPGA board with additional inputs and outputs.

## 2. Existing work

- Design and FPGA implementation of a 16-bit microprocessor was done using VHDL. It was able to execute 16 instructions such as add, subtract, multiply, divide, load and store. Design was realized and verified on Xilinx Spartan-3[1].
- Later on 16 bit and 32 bit pipelined RISC processors were implemented using Spartan-3AN and Spartan-3E respectively [2], [3].
- The 64-bit RISC Processor with 33 instructions was designed and implemented on Spartan-3E. The design was verified on Xilinx ISE 10.1i simulator [4].

- Control unit of a 16-bit processor was implemented in Spartan-2 FPGA [5] and Spartan-3E [5], [6], [7].
- 8 bit RISC processor using FPGA Spartan 3E was later implemented using Verilog. Design of Control unit, ALU, shift registers and accumulator register were highly focused [8].
- Recently 16 bit Processor was designed using VHDL. The CPU, shifter, comparator, control unit and memory were integrated in proposed processor. Spartan-6 FPGA was used [9].

## 3. Processor Design

This paper actually describes an instructional processor. Group of instructions are programmed and tested experimentally as separate modules. Group include data transfer instruction group, arithmetic instruction group, logical instruction group, machine control and branching instruction group. All types of instructions are programmed using Xilinx ISE 12.4 and are tested using Spartan-6 with additional set of inputs and outputs. Opcodes are optimized which make them meaningful and reduce complexity. Later on this technique can also be used to reduce consumption of power when actual processor will be fabricated.

### 3.1 Opcode Optimization

Opcode length is of 8 bit as the processor designed is 8 bit processor. So the total number of possible Opcodes is 256. General format of 8 bit instruction is as follows

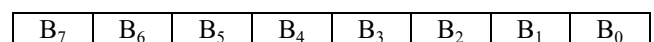


Figure 1: 8-bit Instruction Format

B<sub>n</sub> represents n<sup>th</sup> bit where n represents bit number (0 to 7). Opcodes are optimized as follows

Table 1: Optimization using B<sub>7</sub> & B<sub>6</sub> bits

B <sub>7</sub>	B <sub>6</sub>	Type of Group
0	0	Data transfer instruction group
0	1	Arithmetic instruction group
1	0	Logical instruction group
1	1	Machine control instruction group

Further optimization is done on basis on groups. It is as follows:

**3.1.1 Data transfer instruction group:**

In data transfer group Bits  $B_7$  and  $B_6$  will be "00". Further optimization is done using  $B_5$ ,  $B_4$ , and  $B_3$  bits.

**Table 2:** Data transfer group

$B_5$	$B_4$	$B_3$	Type of instruction / register
0	0	0	Register A
0	0	1	Register B
0	1	0	Register C
0	1	1	Register D
1	0	0	Register E
1	0	1	Immediate data transfer instructions
1	1	0	Swap instructions
1	1	1	Push / Pop instructions

**3.1.2 Arithmetic instruction group:**

In Arithmetic instruction group Bits  $B_7$  and  $B_6$  will be "01". Further optimization is done using  $B_5$ ,  $B_4$ , and  $B_3$  bits.

**Table 3:** Arithmetic group

$B_5$	$B_4$	$B_3$	Type of instruction
0	0	0	Addition
0	0	1	Addition with carry
0	1	0	Subtraction
0	1	1	Subtraction with borrow
1	0	0	Increment
1	0	1	Decrement
1	1	0	Add / Sub immediate data
1	1	1	Multiplication & division

**3.1.3 Logical Instruction Group**

In Logical instruction group Bits  $B_7$  and  $B_6$  will be "10". Further optimization is done using  $B_5$ ,  $B_4$ , and  $B_3$  bits.

**Table 4:** Logical group

$B_5$	$B_4$	$B_3$	Type of instruction
0	0	0	AND
0	0	1	OR
0	1	0	XOR
0	1	1	Compare
1	0	0	Rotate left
1	0	1	Rotate right
1	1	0	Rotate left with carry
1	1	1	Rotate right with carry

**3.1.4 Machine control & Branching Instruction Group**

In Machine control instruction group Bits  $B_7$  and  $B_6$  will be "11". Further optimization is done using  $B_5$ ,  $B_4$ , and  $B_3$  bits.

**Table 5:** Machine control group

$B_5$	$B_4$	$B_3$	Type of instruction
0	0	0	IN
0	0	1	OUT
0	1	0	HLT
0	1	1	NOP
1	0	0	Branch

In such manner 101 Opcodes are optimized out of 256 possible opcodes.

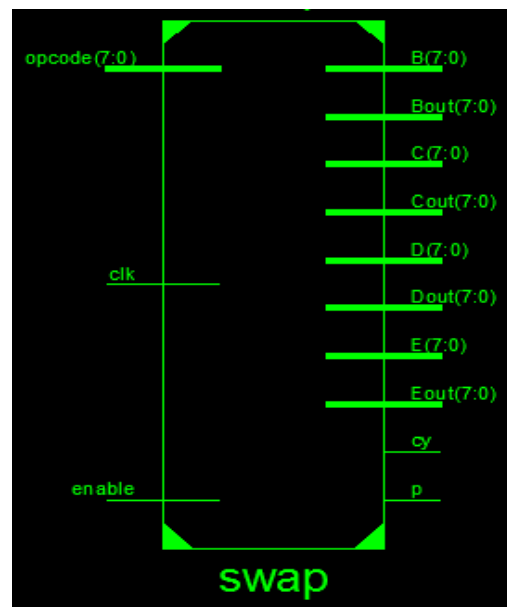
**3.2 Experimentation**

Instructions of processor are tested in different modules. RTL schematic along with the obtained simulation of one instruction from each group is given below

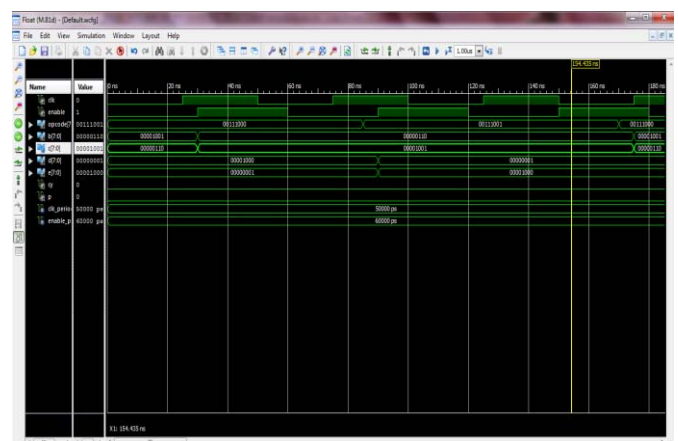
**3.2.1 Data transfer instruction group:**

Instructions of this group include data transfer from register to register data transfer of immediate data to register, swap instructions, Push instruction and Pop instruction.

From the above instructions, RTL Schematic and Simulation for Swap instruction is shown below. Swap includes instructions such as SWAP B, C and SWAP D, E. These instructions perform swapping of data from register B to register C and vice versa. Similarly, swapping of data from register D to register E and vice versa. Simulation shows the result of swap instructions.



**Figure 2 (a):** RTL Schematic for Swap instruction



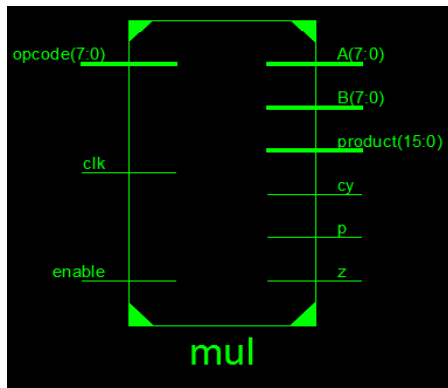
**Figure 2 (b):** Simulation of Swap instruction

Both SWAP B, C and SWAP D, E are executed in simulation for their respective opcodes.

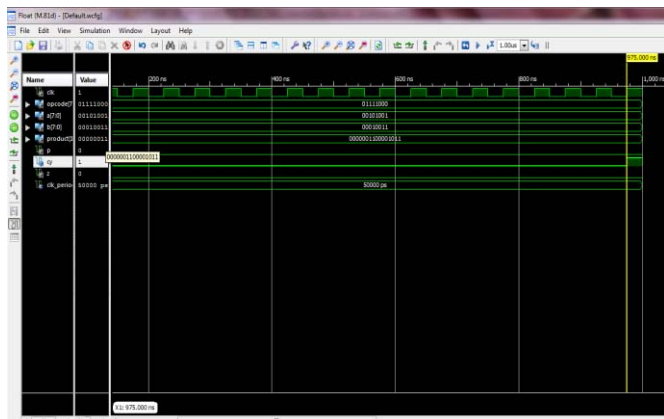
**3.2.2 Arithmetic instruction group:**

This group includes instructions such as Addition of data from two registers with or without carry; Subtraction of data from two registers with or without borrow; Increment or decrement data of registers; Addition and subtraction of immediate data; Multiplication and division of data from two registers.

From the above instructions, RTL Schematic and Simulation for multiplication instruction is shown below. Multiplication includes instructions such as MUL A, B. This instruction performs multiplication of data from register A and register B.



**Figure 3 (a):** RTL Schematic for Multiplication instruction

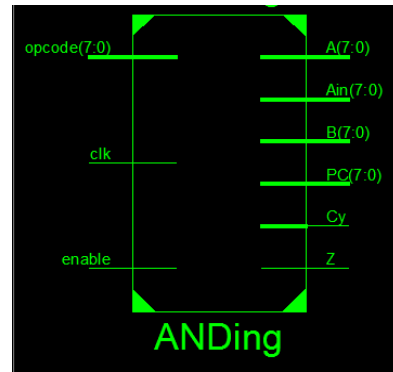


**Figure 3 (b):** Simulation of Multiplication instruction

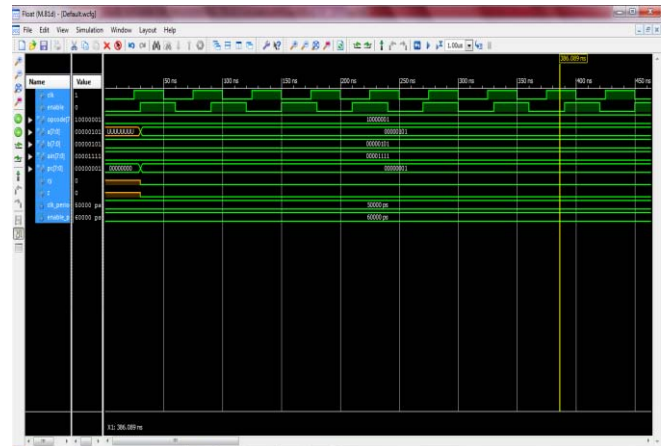
Simulation for instruction MUL A, B for its respective opcode is shown above.

**3.2.3 Logical instruction group:**

This group of instructions perform logical operations such as AND, OR, XOR, compare, Rotate with and without carry. Any 8 bit direct data or contents of register can be logically operated.



**Figure 4 (a):** RTL Schematic for AND instruction

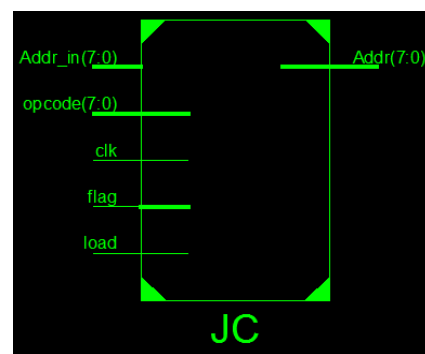


**Figure 4 (a):** Simulation for AND instruction

**3.2.4 Machine Control Branching group :**

This group of instructions performs machine control functions such as No operation, Halt, etc. Branching group of instruction changes the path of program execution or sequence of program execution.

RTL Schematic and simulation of JUMP instruction is shown below. JUMP instruction transfers the program control to specified address.



**Figure 5 (a):** RTL Schematic for Jump instruction

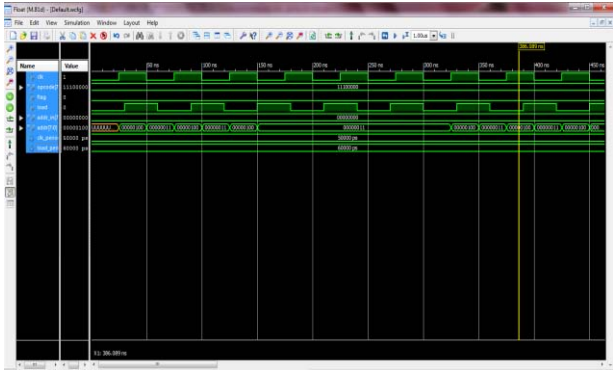


Figure 5 (b): Simulation of Jump instruction

#### 4. Experimental Setup

Experimental setup include Spartan-6 FPGA (XC6LX16-CS324) board, additional switches and LEDs as inputs and outputs respectively, laptop with Xilinx ISE 12.4 and USB cable for interfacing FPGA board with laptop.

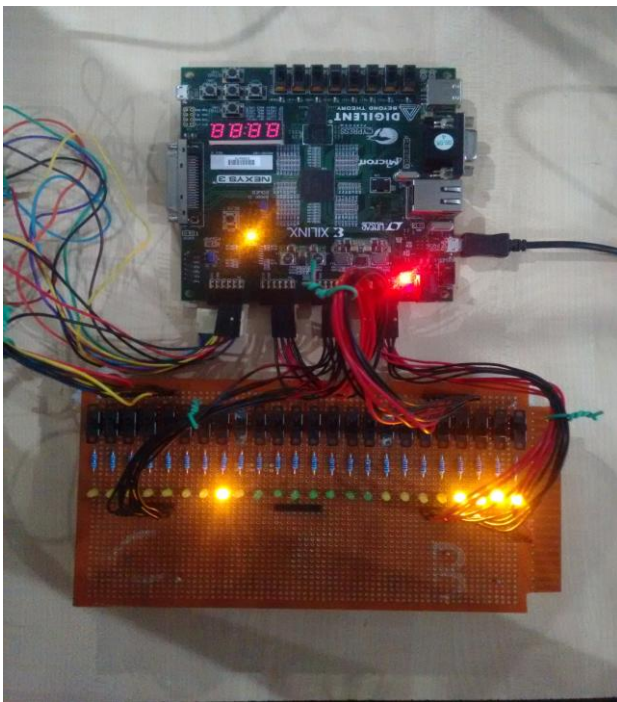


Figure 6: Experimental setup

#### 5. Conclusion and Future Scope

In such manner Instructions of processor were programmed. Following the simulation work, the entire model was synthesized using Xilinx ISE 12.4 and dumped on to a Spartan-6 FPGA board for functional verification, which was carried out successfully. Opcode optimization was done in order to increase simplicity of Opcodes and will further reduce power consumption. Future scope includes consideration of more bits i.e. 16, 32, etc. and also to increase number of operations performed by processor.

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